NP50P04SLG

MOS FIELD EFFECT TRANSISTOR

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Description

The NP50P04SLG is P-channel MOS Field Effect Transistor designed for high current switching applications.

Features

- Super low on-state resistance
  - $R_{DS(on)1}$ = 9.6 mΩ MAX. (V_{GS} = –10 V, I_D = –25 A)
  - $R_{DS(on)2}$ = 15 mΩ MAX. (V_{GS} = –4.5 V, I_D = –25 A)
- Low input capacitance
- Gate to Source ESD protection diode built-in

Ordering Information

Part No.	LEAD PLATING	PACKING	Package
NP50P04SLG-E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	TO-252 (MP-3ZK)
NP50P04SLG-E2-AY *1			

Note: *1. Pb-free (This product does not contain Pb in external electrode.)

Absolute Maximum Ratings (T_A = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	–40	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	∓20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	∓50	A
Drain Current (pulse) *1	$I_{D(pulse)}$	∓150	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	84	W
Total Power Dissipation (T_A = 25°C)	P_{T2}	1.2	W
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	–55 to +175	°C
Single Avalanche Current *2	I_{AS}	37	A
Single Avalanche Energy *2	E_{AS}	136	mJ

Thermal Resistance

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	1.78	°C/W
Channel to Ambient Thermal Resistance *2	$R_{th(ch-A)}$	125	°C/W

Notes: *1. PW ≤ 10 μs, Duty Cycle ≤ 1%

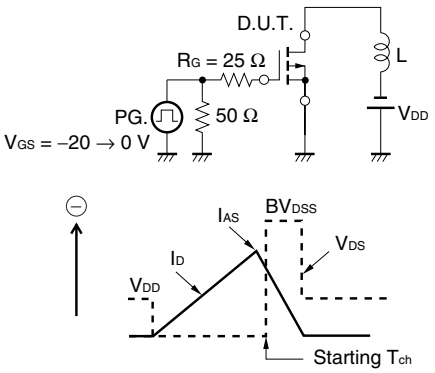
*2. Starting T_{ch} = 25°C, V_{DD} = –20 V, R_G = 25 Ω, V_{GS} = –20 → 0 V

Electrical Characteristics (T_A = 25°C)

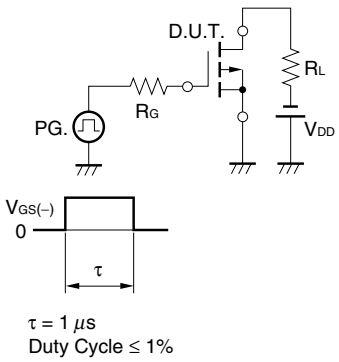
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}			–1	μA	V_{DS} = –40 V, V_{GS} = 0 V
Gate Leakage Current	I_{GSS}			∓10	μA	V_{GS} = ∓20 V, V_{DS} = 0 V
Gate to Source Threshold Voltage	$V_{GS(th)}$	–1.0	–1.4	–2.5	V	V_{DS} = V_{GS}, I_D = –250 μA
Forward Transfer Admittance *1	$\|y_{fs}\|$	12	44		S	V_{DS} = –10 V, I_D = –25 A
Drain to Source On-state Resistance *1	$R_{DS(on)1}$		8.2	9.6	mΩ	V_{GS} = –10 V, I_D = –25 A
	$R_{DS(on)2}$		9.8	15	mΩ	V_{GS} = –4.5 V, I_D = –25 A
Input Capacitance	C_{iss}		3800	5700	pF	V_{DS} = –10 V,
Output Capacitance	C_{oss}		740	1120	pF	V_{GS} = 0 V,
Reverse Transfer Capacitance	C_{rss}		500	905	pF	f = 1 MHz
Turn-on Delay Time	$t_{d(on)}$		11	24	ns	V_{DD} = –20 V, I_D = –25 A,
Rise Time	t_r		15	39	ns	V_{GS} = –10 V,
Turn-off Delay Time	$t_{d(off)}$		250	505	ns	R_G = 0 Ω
Fall Time	t_f		150	380	ns	
Total Gate Charge	Q_G		100	150	nC	V_{DD} = –32 V,
Gate to Source Charge	Q_{GS}		13		nC	V_{GS} = –10 V,
Gate to Drain Charge	Q_{GD}		30		nC	I_D = –50 A
Body Diode Forward Voltage *1	$V_{F(S-D)}$		0.96	1.5	V	I_F = –50 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}		50		ns	I_F = –50 A, V_{GS} = 0 V,
Reverse Recovery Charge	Q_{rr}		63		nC	di/dt = –100 A/μs

Note: *1. Pulsed test PW ≤ 350 μs, Duty Cycle ≤ 2%

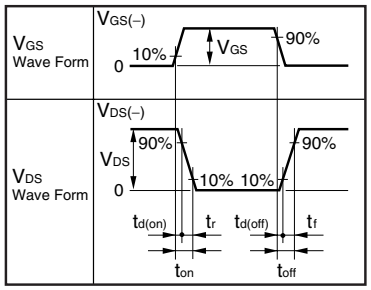
TEST CIRCUIT 1 AVALANCHE CAPABILITY



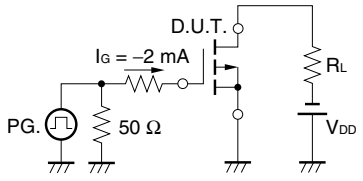
TEST CIRCUIT 2 SWITCHING TIME



τ = 1 μs
Duty Cycle ≤ 1%

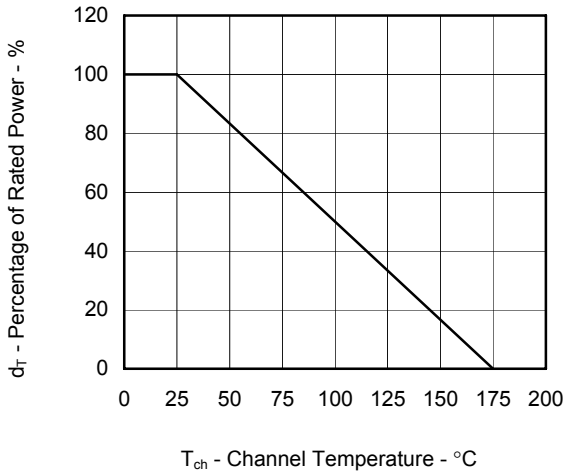


TEST CIRCUIT 3 GATE CHARGE

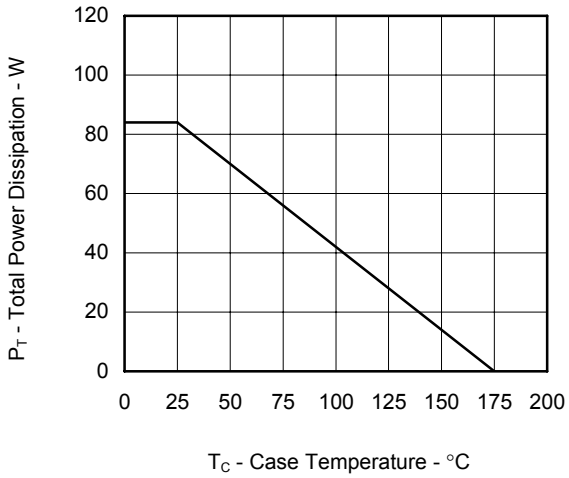


Typical Characteristics (T_A = 25°C)

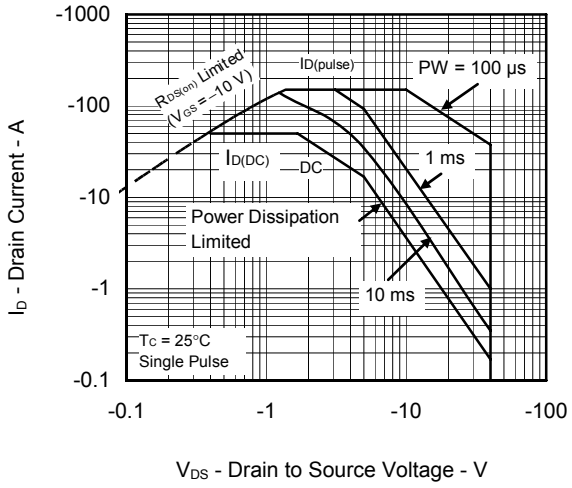
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



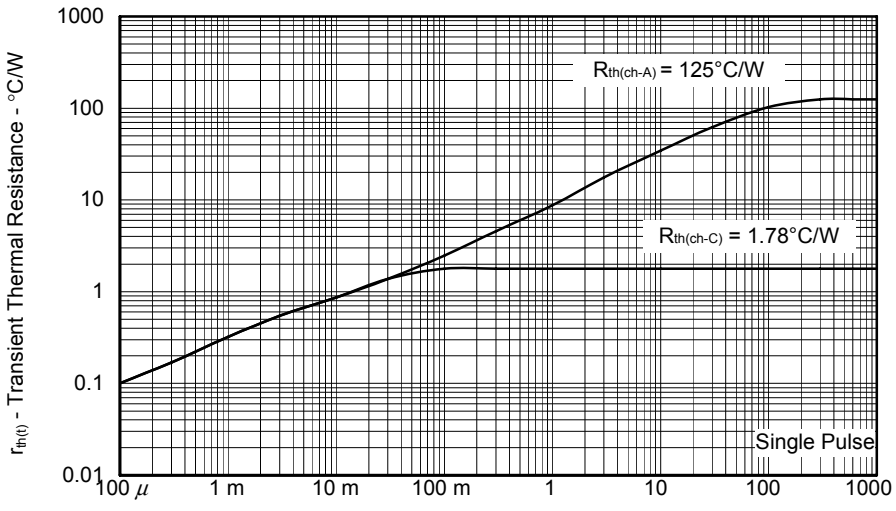
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



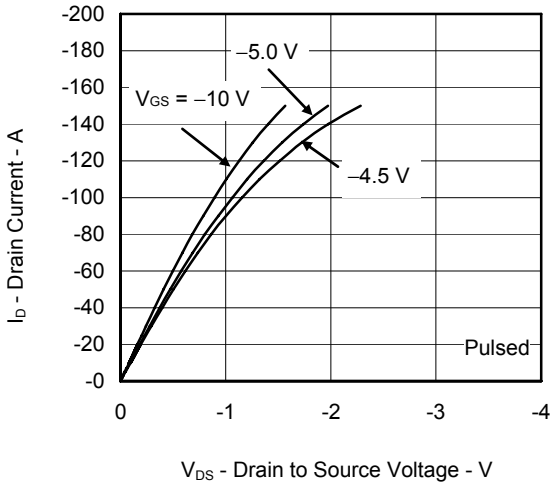
FORWARD BIAS SAFE OPERATING AREA



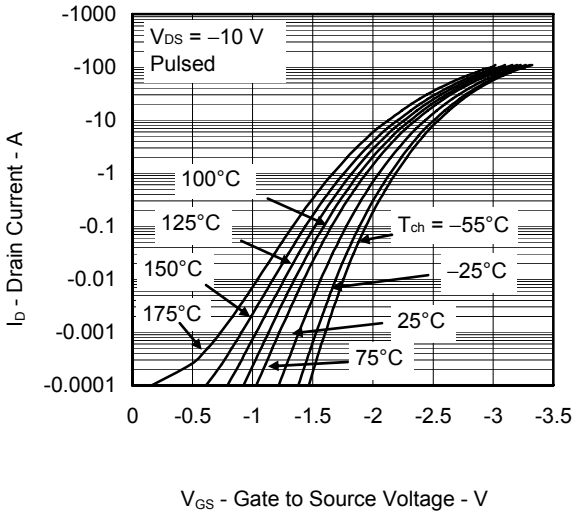
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



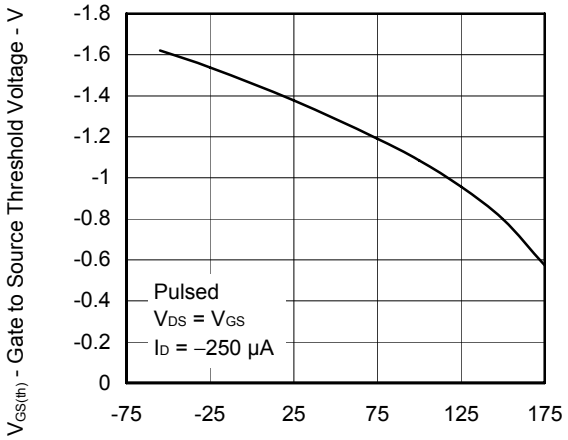
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



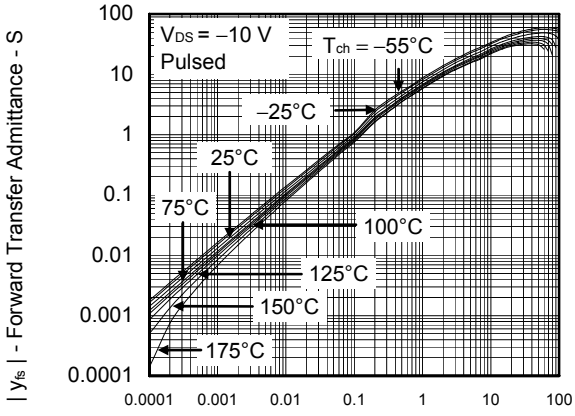
FORWARD TRANSFER CHARACTERISTICS



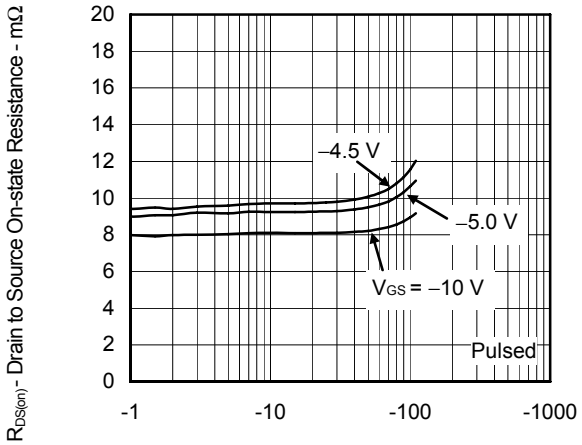
GATE TO SOURCE THRESHOLD VOLTAGE vs.
CHANNEL TEMPERATURE



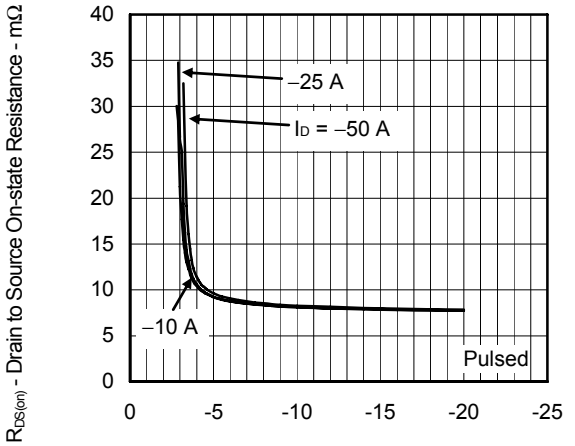
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



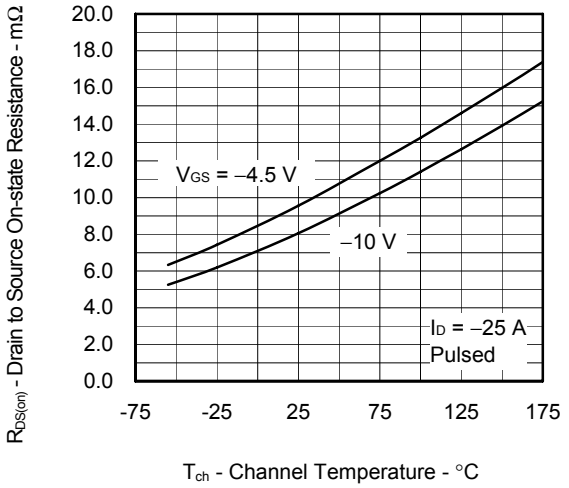
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



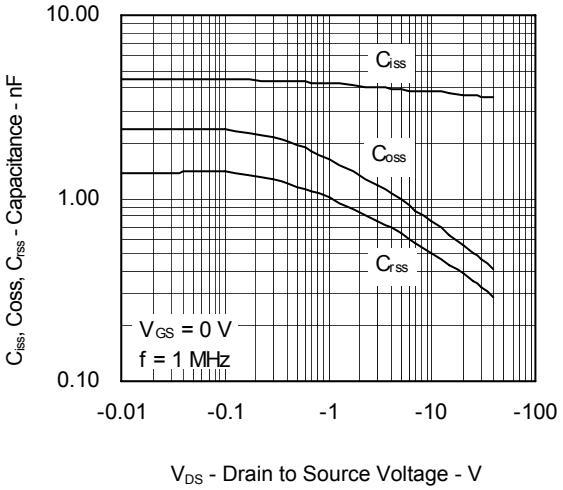
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



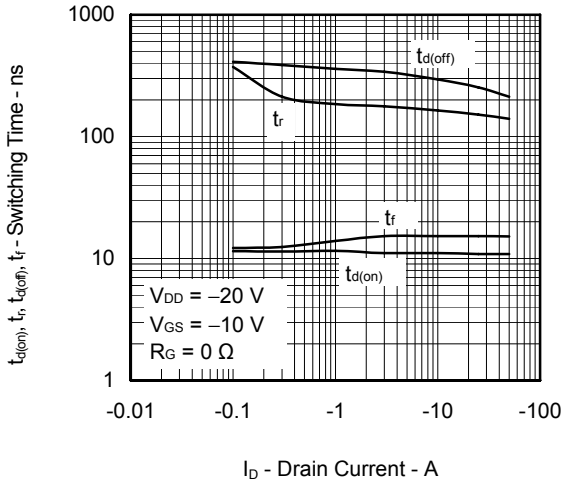
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



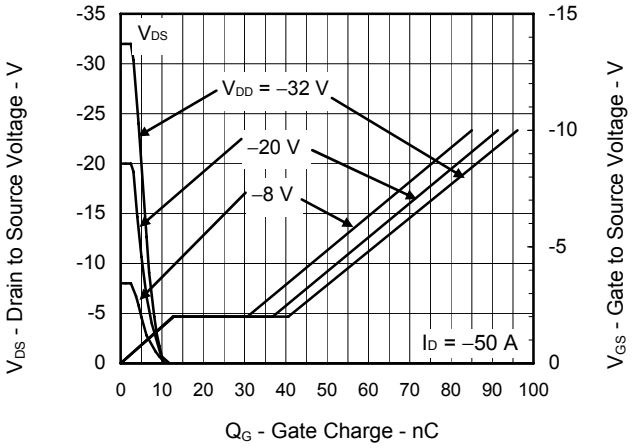
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



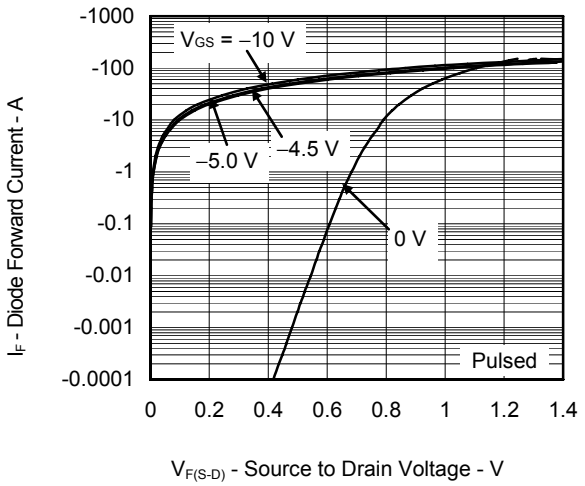
SWITCHING CHARACTERISTICS



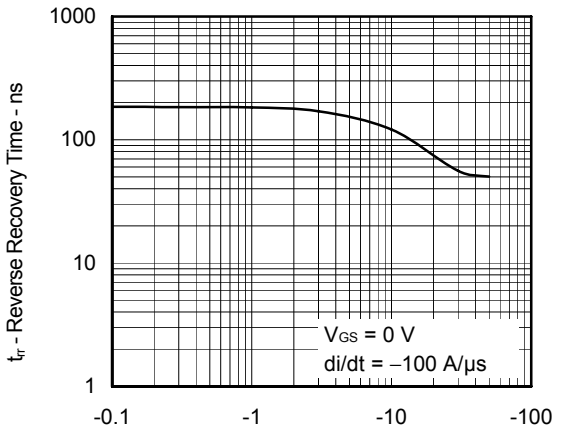
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

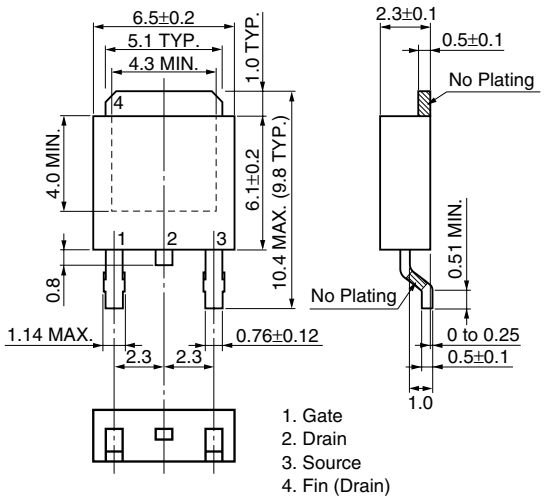


REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

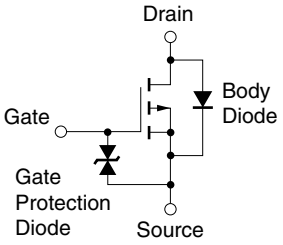


Package Drawings (Unit: mm)

TO-252 (MP-3ZK)



Equivalent Circuit



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

Revision History	NP50P04SLG Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Feb 09, 2011	–	First Edition Issued

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