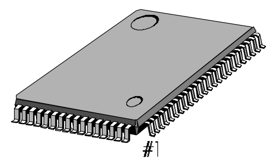
INTRODUCTION

80-QFP-1420C

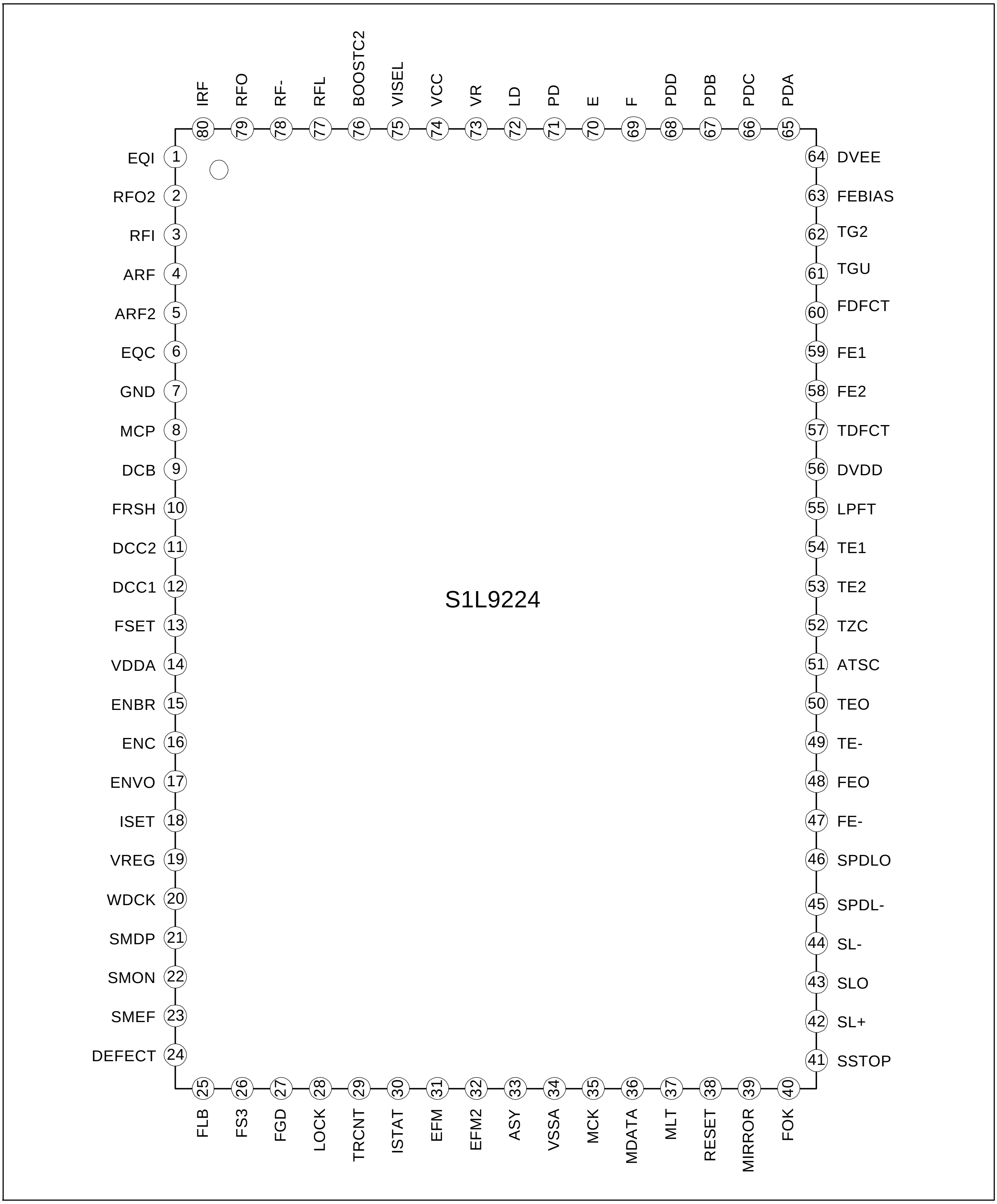


The S1L9224 is a servo signal processor designed specifically for the samsung video-CD designed using the BICMOS process. RF block and picture quality enhancing Items are built-in. The processor is a hard-wired free-adjustment servo with the pre-signal parts adjustment point automatically adjusted.

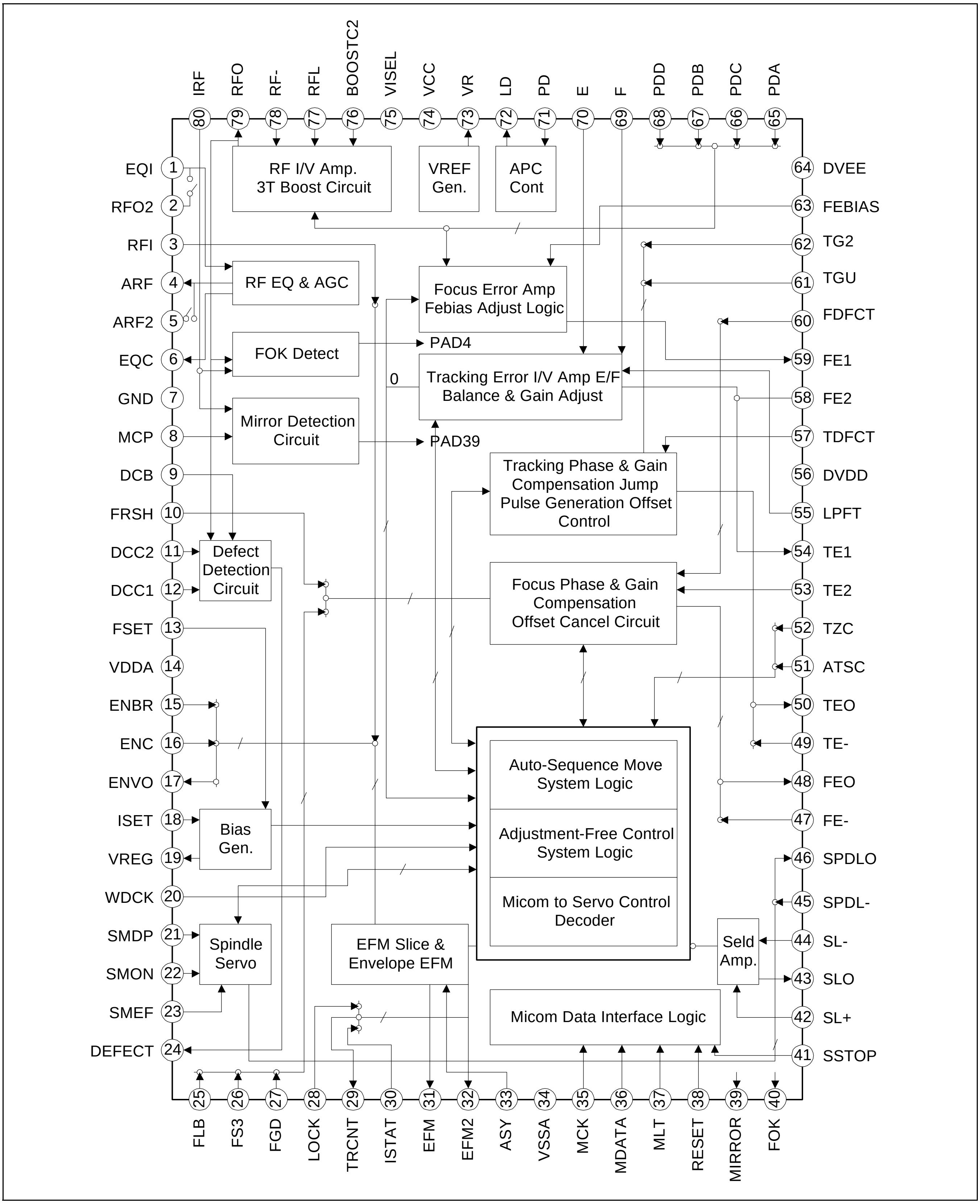
FEATURES

- Focus error amplifier & servo control
- Tracking error amplifier & servo control
- Sled amplifier
- Embedded CLV control LPF
- Mirror, FOK, and defect detector circuit
- APC (Auto Laser Power Control) circuit for constant laser power
- Double speed play available
- Circuit for interruption countermeasure
- FE bias & focus servo offset free adjustment
- EF balance & tracking loop gain free adjustment
- Tracking servo offset free adjustment
- Enhanced auto-sequence algorithm (fast-search)
- Tracking muting by window mirror
- Current, voltage pick-up interaction available
- Embedded RF 3T boost circuit
- Enhanced RF equalize AGC circuit
- Built-in focus, tracking 2x filter adjust
- Single power supply: +5 V
- Related products
  - KS9287 data processor
  - KS9284 data processor
  - KA9258D/KA9259D motor driver

PIN CONFIGURATION



BLOCK DIAGRAM



PIN DESCRIPTION

Table 1. Pin Description

No.	Pin Name	I/O	Description
1	EQI	I	RF AGC & eqaualize input pin
2	RFO2	I	RFO buffer output and RFOB output for capacity merge with RFO (by MICOM)
3	RFI	I	EFM comparator input pin
4	ARF	O	RF AGC & EQ output pin.
5	ARF2	O	RF AGC & EQ output pin (output enable controlled by C1FLAG)
6	EQC	I	AGC_equalize level control pin, VCA input pin & noise eliminating CAP pin
7	GND	G	Ground (RF block)
8	MCP	I	Half-wave rectifier CAP pin for MIRROR output
9	DCB	I	Defect max duty limiting CAP pin
10	FRSH	I	Focus search generating & charge/discharge CAP pin
11	DCC2	I	Defect min duty generating DC eliminating CAP pin. (connected DCC1)
12	DCC1	O	Defect min duty generating DC eliminating CAP pin (connected DCC2)
13	FSET	I	Focus, tracking, spindle peaking frequency compensation bias pin
14	VDDA	P	5V power pin for servo
15	ENBR	I	Bias pin for envelope EFM-slice
16	ENC	I	RF envelope DC bias extract voltage input pin
17	ENVO	O	RF envelope output pin
18	ISET	I	Focus search, tracking jump, sled kick voltage generating bias pin
19	VREG	O	3.4V regulator output pin
20	WDCK	I	88.2kHz input pin from DSP
21	SMDP	I	SMDP input pin of DSP
22	SMON	I	SMON input pin of DSP
23	SMEF	I	External LPF time constant connection pin of CLV servo error signal
24	DEFECT	O	Defect output pin.
25	FLB	I	CAP pin for focus loop rising low band
26	FS3	I	Focus loop’s high frequency gain adjustment pin
27	FGD	I	Focus loop’s high frequency gain adjustment pin
28	LOCK	I	Sled run away preventing pin (L: sled off and tracking gain up)
29	TRCNT	O	Track count output pin
30	ISTAT	O	Internal status output pin
31	EFM	O	RFO slice EFM output pin (to DSP)
32	EFM2	O	EFM comparator integrating output pin

Table 1. Pin Description(Continued)

No.	Pin Name	I/O	Description
33	ASY	I	Auto asymmetry control input pin
34	VSSA	G	Servo part analog VSSA power supply pin
35	MCK	I	Micom clock pin
36	MDATA	I	Data input pin
37	MLT	I	Data latch input pin
38	RESET	I	Reset input pin
39	MIRROR	O	MIRROR detect output pin
40	FOK	O	Focus ok output pin
41	SSTOP	I	Pick up's maximum lead-in diameter position check pin
42	SL+	I	Sled servo non-inverting input
43	SLO	O	Sled servo output
44	SL-	I	Sled servo inverting input
45	SPDL-	I	Spindle AMP inverting input pin
46	SPDLO	O	Spindle AMP output pin
47	FE-	I	Focus servo AMP inverting input pin
48	FEO	O	Focus servo AMP output pin
49	TE-	I	Tracking servo AMP inverting input pin
50	TEO	O	Tracking servo AMP output pin
51	ATSC	I	Anti-shock input pin
52	TZC	I	Tracking zero crossing input pin
53	TE2	I	Tracking servo input pin
54	TE1	O	Tracking error AMP output pin
55	LPFT	I	Tracking error integrating input pin (auto adjust)
56	DVDD	P	Logic DVDD power supply pin
57	TDFCT	I	Defect tracking error integrating CAP connection pin
58	FE2	I	Focus servo input pin
59	FE1	O	Focus error AMP output pin
60	FDFCT	I	When defect, focus error integrating CAP connection pin
61	TGU	I	High frequency tracking gain switching CAP connection pin
62	TG2	I	Time constant controlling tracking loop's high frequency gain control pin
63	FEBIAS	I	Focus error bias control connect pin
64	DVEE	G	Logic DVEE power supply pin
65	PDA	I	Poto-diode A & RF I/V AMP1 inverting input pin

Table 1. Pin Description(Continued)

No.	Pin Name	I/O	Description
66	PDC	I	Poto-diode C & RF I/V AMP1 inverting input pin
67	PDB	I	Poto-diode B & RF I/V AMP2 inverting input pin
68	PDD	I	Poto-diode D & RF I/V AMP2 inverting input pin
69	F	I	Poto-diode F & tracking (F) I/V AMP inverting input pin
70	E	I	Poto-diode f & tracking (E) I/V AMP inverting input pin
71	PD	I	APC AMP input pin
72	LD	O	APC AMP output pin
73	VR	O	(VCC+GND)/2 voltage reference output pin
74	VCC	P	RF part VCC power supply pin
75	VISEL	I	Current, voltage pick-up select command inverting control pin (pull → down) ex) Voltage type pick-up + command pull up → current type pick-up composition Current type pick-up + command pull up → voltage type pick-up composition
76	BOOSTC2	I	RF summing AMP 3T boost's CAP connection pin (connected GND)
77	RFL	I	RF summing AMP noise eliminating CAP connection pin (connected RFO)
78	RF-	I	RF summing AMP inverting input pin
79	RFO	O	RF summing AMP output pin
80	IRF	I	RFO DC eliminating input pin (used in MIRROR, FOK pin)

MICOM COMMAND

($0X, $1X)

Item	Address	Data				ISTAT Output
	Symbol	D3	D2	D1	D0	
Focus control	0 0 0 0	FS4 Focus on	FS3 Gain down	FS2 Search on	FS1 Search up	FZC
Tracking control	0 0 0 1	Anti-shock	Brake on	TG2 Gain set	TG1 Gain set	ATSC

Tracking Gain Setting for Anti-Shock

D7	D6	D5	D4	D3		D2		D1		D0		ISTAT Output
				Anti-Shock		Lens. Brake		TG2 (D3 = 1)		TG1		
0	0	0	1	0	1	0	1	0	1	0	1	ATSC
				Anti-shock off	Anti-shock on	Lens brake off	Lens brake on	High freq. gain down	High freq. normal gain	Nor-mal gain	Gain up	

Item	Hex	AS = 0		AS = 1	
		TG2	TG1	TG2	TG1
Tracking gain control TG1, TG2 = 1 gain up	$10	0	0	0	0
	$11	0	1	0	1
	$12	1	0	1	0
	$13	1	1	1	1
	$14	0	0	0	0
	$15	0	1	0	1
	$16	1	0	1	0
	$17	1	1	1	1
$13, $17, $1B, $1F (AS0) $13, $17, $18, $1C (AS1) Tracking gain up at this time, MIRROR muting is off	$18	0	0	1	1
	$19	0	1	1	0
	$1A	1	0	0	1
	$1B	1	1	0	0
	$1C	0	0	1	1
	$1D	0	1	1	0
	$1E	1	0	0	1
	$1F	1	1	0	0

$2X

D7	D6	D5	D4	D3		D2		D1		D0		ISTAT Output
				Tracking Servo Mode				Sled Servo Mode				
0	0	1	0	Mode	TM7	TM6	TM5	TM4	TM3	TM2	TM1	TZC
TM1				$20	1	0	1	0	1	1	0	
0	Track. servo off			$21	1	0	1	0	1	0	0	
1	Track. servo on			$22	1	0	0	0	1	1	0	
TM2				$23	1	1	1	0	1	1	0	
0	Sled. servo on			$24	1	0	1	0	1	1	1	
1	Sled. servo off			$25	1	0	1	0	1	0	1	
TM4	TM3	Track.kick		$26	1	0	0	0	1	1	1	
0	0	FWD. jump		$27	1	1	1	0	1	1	1	
0	0	Jump off		$28	1	0	1	0	0	1	0	
0	0	REV. jump		$29	1	0	1	0	0	0	0	
TM4	TM3	Sled. kick		$2A	1	0	0	0	0	1	0	
0	0	FWD. kick		$2B	1	1	1	0	0	1	0	
0	0	Kick off		$2C	1	0	1	1	1	1	0	
0	0	REV. kick		$2D	1	0	1	1	1	0	0	
TM7 (Jump)				$2E	1	0	0	1	1	1	0	
1	Lens brake on			$2F	1	0	0	1	1	1	0	

Tracking Condition for DIRC (Direct 1 Track Jump)

Item	Hex	DIRC = 1	DIRC = 0	DIRC = 1
		TM 654321	TM 654321	TM 654321
Tracking mode	$20	000000	001000	000011
	$21	000010	001010	000011
	$22	010000	011000	100001
	$23	100000	101000	100001
	$24	000001	000100	000011
	$25	000011	000110	000011
	$26	010001	010100	100001
	$27	100001	100100	100001
	$28	000100	001000	000011
	$29	000110	001010	000011
	$2A	010100	011000	100001
	$2B	100100	101000	100001
	$2C	001000	000100	000011
	$2D	001010	000100	000011
	$2E	011000	000100	100001
	$2F	101000	100100	100001

Register $3X

Address	Focus Search		Sled Kick		C1 Flag Output Defect Duty			3TEQ	Speak
	D11	D10	D9	D8	D7	D6		D5	D4
D15-D12 0011	PS4 Search+2	PS3 Search+1	PS2 Kick+2	PS1 Kick+1	DSPMC2	DSPMC	State	Equalize 3T boost SW 0: Off 1: On	Peaking prevent standard freq. 0: 88kHz 1: 44kHz
					0	0	0.45ms		
					0	1	0.54ms		
					1	0	0.63ms		
					1	1	0.73ms		
Initial					0	1		0	0

Address	MODEC	ONOFF	TOCD	INT3	D3: Envelope EFM-slice or normal EFM-slice select ELOCK H → LOCK H: envelope converse
	D3	D2	D1	D0	
D15-D12 0011	EFM slice 0: Envel 1: Normal	Peaking prevent 0: Off 1: On	Tracking offset adjust 0: Off 1: On	Focus servo cpeak mute 0: Off 1: On	D1: Tracking servo offset adjust select - TOCD: Tracking balance, gain offset adjust select
Initial	1	0	1	0	Register reset command (0: reset, 1: reset cancel) Tracking servo offset a adjust. (0: no used, 1: used)

Select (Upper 8 bits out of 16 bits)

D7	D6	D5	D4	D3	D2	D1	D0	ISTAT
0	0	1	1	Focus servo search level control		Sled servo kick level control		SSTOP
				PS4	PS3	PS2	PS1	
				Search + 2	Search + 1	Kick + 2	Kick + 1	
Data mode (level)				Search X1	$30 - $33	Kick X1	$30, $34, $38, $3C	
				Search X2	$34 - $37	Kick X2	$31, $35, $39, $3D	
				Search X3	$38 - $3B	Kick X3	$32, $36, $3A, $3E	
				Search X4	$3C - $3F	Kick X4	$33, $37, $3B, $3F	
Data				S.X1, K.X1	S.X2, K.X2	S.X3, K.X3	S.X4, K.X4	
				$30	$35	$3A	$3F	

Auto Sequence Mode

Address				Data			
0	**1**	**0**	**0**	**D3**	**D2**	**D1**	**D0**
Auto-sequence cancel				0	0	0	0
Auto-focus				0	1	1	1
1-track jump				1	0	0	0: FWD 1: REV
10-track jump				1	0	1	
2N-track jump				1	1	0	
M-track jump				1	1	1	
Fast search				0	1	0	

Speed Related Command ($FX)

Address				Data			
1	**1**	**1**	**1**	**D3**	**D2**	**D1**	**D0**
x 1 speed				0	0	0	0
x 2 speed				0	0	1	1

RAM Register Set

Item		Data											
Address		D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Blind A, E overflow. C	$5XX	0.18 ms	0.09 ms	0.04 ms	0.02 ms								
Brake. B		0.36 ms	0.18 ms	0.09 ms	0.04 ms					I/V → 0: Voltage, 1: Current type T.RST → 0: Reset cancel, 1: Reset Tracking servo offset			
Fast F		23.2 ms	11.6 ms	5.80 ms	2.90 ms								
Fast K						0.72 ms	0.36 ms	0.18 ms	0.09 ms	I/V SEL	T.RST adjust	EFMB C	FJTS
	INI.	1	0	1	0	1	0	0	0	0	0	0	0
Kick D	$6XXX	11.6 ms	5.80 ms	2.90 ms	1.45 ms					EFMBC: Double compensation of EFM ASY 1: Single (no used), 0: (used) FJTS: Fast search tracking mute 0: No used, 1: Used			
FAST R		23.2 ms	11.6 ms	5.80 ms	2.90 ms								
PWM duty PD						8	4	2	1				
PWM width PW										5.8 ms	2.9 ms	1.45 ms	0.75 ms
	INI.	0	1	1	1	1	0	1	0	0	0	1	0
2N TRA N M TRA. M	$7XXX	4096	2048	1024	512	256	128	64	32	16	8	4	2
Fast search T	$7XXX	16384	8192	4096	2048	1024	512	256	128	64	32	16	8
	INI.	0	0	0	0	0	0	1	1	1	1	1	1
Brake point P	$BXXX	16384	8192	4096	2048	1024	512	256	128	64	32	16	8
	INI.	0	0	0	0	0	0	1	1	1	0	0	0

NOTES:

Actually count value can be a little error in fixed value.
A fixed value + 4-5 WDCK
B, D, E, fixed value + 3 WDCK
C fixed value + 5 WDCK
N, M, T, P fixed value + 3 TRCNT

Warning

1. Out of the 16 settings, PWM width (PW) can select only one of 1, 2, 4, or 8 (not a 4-bit mixture)
2. When using a 2N track or an M track, more than 512 tracks is not recommended (potential for error within the algorithm)
3. There can be a 1-2 error in the WPM duty (PD), so set to fixed value + 2
4. $5XXXs I/V SEL command (0: pick-up configuration using voltage 1: current-type only)
5. T.RST: 0: Tracking servo offset DAC value RESET cancel
   1: Tracking servo offset DAC value RESET
6. EFMBC: 0: Double ASY compen sation EFM slicer
   1: Single ASY compen sation EFM slicer

7: FJTS: When fast search, tracking servo off mode

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{max}		5		V
Operating temperature	T_{OPR}	- 20	25	70	°C
Storage temperature	T_{STG}	- 55	25	150	°C
Permissible loss	Pd		150		mW

ELECTRICAL CHARACTERISTICS

Table 2. Electrical Characteristics

No	Item	Symbol	Block	Min	Typ	Max	Unit
1	Supply current 6V	ICCHI	Supply current	15	40	60	mA
2	Supply current 5V	ICCTY		12	32	50	mA
3	Supply current 4V	ICCLO		10	25	40	mA
4	RF AMP offset voltage	Vrfo	RF AMP	-85	0	+85	mV
5	RF AMP oscillation voltage	Vrfosc		0	50	100	mV
6	RF AMP voltage gain	Grf		16.2	19.2	23.0	dB
7	EQ12 on flag	FLON		0.85	1.00	1.15	dB
7-1	EQ12 off flag	FLOFF		-	-	-15	dB
8	RF RHD charac.	RFTHD		-	-	5	%
9	RF AMP maximum output voltage	Vrfpp1		3.8	-	-	V
10	RF AMP minimum output voltage	Vrfpp2		-	-	2.0	V
11	1X RF AC charac.	RFAC1		0.00	1.50	2.0	-
12	2X RF AC charac.	RFAC2		0.00	1.25	4.0	-
13	Visel control register 1	RVISEL1		35	55	85	kohm
14	Visel control register 2	RVISEL2		35	55	85	kohm
15	RF IVSEL connection charac. AC	RFSELAC		35	55	85	kohm
16	RF IVSEL connection charac. BD	RFSELBD		35	55	85	kohm
17	RF IVSEL connection charac. AC2	RFSELAC2		70	110	160	kohm
18	RF IVSEL connection charac. BD2	RFSELBD2		70	110	160	kohm
19	Focus ERROR offset voltage	VFEO1	Focus error AMP	-525	-250	-50	mV
20	Focus ERROR auto voltage	VFEO2		-70	0	+70	mV
21	Istat after febias adjust	VISTAT1		4.3	-	-	V
22	Focus ERROR voltage gain 1	GFEAC		18	21	24	dB

Table 2. Electrical Characteristics(Continued)

No	Item	Symbol	Block	Min	Typ	Max	Unit
23	Focus ERROR voltage gain 2	GFEBD	Focus error AMP	18	21	24	dB
24	Focus ERROR voltage gain difference	CFE		-3	0	+3	dB
25	Focus ERROR AC difference	VFEACP		0	50	100	mV
26	FERR maximum output voltage H	VFEPPH		4.4	-	-	V
27	FERR minimum output voltage L	VFEPPL		-	-	0.6	V
28	AGC max. gain	GAGC	RF AGC & equalizer	16	19	22.5	dB
29	AGC EQ gain	GEQ		-1	1	2	dB
30	AGC normal gain	GAGC2		3	6	9.8	dB
31	AGC compress ratio	CAGC		0	2.5	5	dB
32	AGC frequency	FAGC		-1.5	0	2.5	dB
33	AGC level control 1	AGCL1		1.03	1.15	3	-
34	AGC level control 2	AGCL2		1.0	1.15	1.3	-
35	AGC level control 3	AGCL3		1.0	1.15	1.25	-
35-1	ARF2 on flag AFLON	RAGCF1		-0.1	0	0.1	-
36	TERR gain voltage gain 1	GTEF1	Tracking error gain & balance	-2	0.5	2	dB
37	TERR gain voltage gain 2	GTEF2		1	1.7	2.4	-
38	TERR gain voltage gain 3	GTEF3		1	1.3	1.6	-
39	TERR gain voltage gain 4	GTEF4		1	1.45	1.9	-
40	TERR gain voltage gain 5	GTEF5		1	1.55	2.1	-
41	TERR gain voltage gain 6	GTEF6		1	1.45	1.9	-
42	TERR gain voltage gain 7	GTEF7		1	1.45	1.9	-
43	TERR balance gain	GTEE		10.5	13.5	16.5	dB
44	TERR balance mode 1	TBE1		0.98	1.05	1.1	-
44-1	TERR balance mode 11	TBE11		0.98	1.05	1.1	-
45	TERR balance mode 2	TBE2		1.0	1.05	1.1	-
46	TERR balance mode 3	TBE3		1.0	1.05	1.1	-
47	TERR balance mode 4	TBE4		1.0	1.10	1.5	-
48	TERR balance mode 5	TBE5		1.0	1.20	1.4	-
49	TERR balance mode 6	TBE6		1.0	1.3	1.75	-
50	TERR EF voltage gain difference	GTEF		10.0	13.0	16.0	dB
51	TERR maximum output voltage H	VTPPH		3.5	-	-	V
52	TERR minimum output voltage L	VTPPL		-	-	1.5	V

Table 2. Electrical Characteristics(Continued)

No	Item	Symbol	Block	Min	Typ	Max	Unit
53	APC PSUB voltage L	APSL	Automatic power control (APC)	-	-	1.2	V
54	APC PSUB voltage H	APSH		3.8	-	-	V
55	APC NSUB voltage L	ANSL		-	-	1.2	V
56	APC NSUB voltage H	ANSH		3.8	-	-	V
57	APC PSUB voltage LDOFF	APSLOF		4.0	-	-	V
58	APC NSUB voltage LDOFF	ANSLOF		-	-	1.0	V
59	APC current drive H	ACDH		2.5	-	-	V
60	APC current drive L	ACDL		-	-	2.5	V
61	MIRROR minimum operting freq.	FMIRB	MIRROR	-	550	900	HZ
62	MIRROR maximum operting freq.	FMIRP		30	75	-	Khz
63	MIRROR AM charac.	FMIRA		-	400	600	HZ
64	MIRROR minimum input voltage	VMIRL		-	0.1	0.2	V
65	MIRROR maximum input voltage	VMIRH		1.8	-	-	V
66	FOK threshold voltage	VFOKT	FOK	-420	-350	-300	mV
67	FOK output voltage H	VFOHH		4.3	-	-	V
68	FOK output voltage L	VFOKL		-	-	0.7	V
69	FOK freq. charac.	FFOK		40	-	-	KHZ
70	Defect bottom voltage	FDFCTB	DEFECT	-	670	1000	HZ
71	Defect cutoff voltage	FDFCTC		2.0	4.7	-	KHZ
72	Defect minimum input voltage	VDFCTL		-	0.3	0.5	V
73	Defect maximum input voltage	VDFCTH		1.8	-	-	V
74	Normal EFM duty voltage 1	NDEFMN	Normal EFM slice	-50	0	+50	mV
75	Normal EFM duty symmetry	NDEFMA		0	5	10	%
76	Normal EFM duty voltage 3	NDEFMH		0	+50	+100	mV
77	Normal EFM duty voltage 4	NDEFML		-100	-50	0	mV
78	Normal EFM minimum input voltage	NDEFMV		-	-	0.12	V
79	Normal EFM duty difference 1	NDEFM1		30	50	70	mV
80	Normal EFM duty difference 2	NDEFM2		30	50	70	mV

Table 2. Electrical Characteristics(Continued)

No	Item	Symbol	Block	Min	Typ	Max	Unit
81	ENV EFM duty voltage 1	EDEFMN1	Envelope EFM slice	-50	0	+50	mV
82	ENV EFM duty voltage 2	EDEFMN2		-50	0	+50	mV
83	ENV EFM duty symmetry	EDEFMA		0	5	10	%
84	ENV EFM duty voltage 3	EDEFMH1		0	+50	+100	mV
85	ENV EFM duty voltage 4	EDEFMH2		+160	+250	+340	mV
86	ENV EFM duty voltage 5	EDEFML1		-100	-50	0	mV
87	ENV EFM duty voltage 6	EDEFML2	Envelope	-340	-250	-160	mV
88	ENV EFM minimum input voltage	EDEFMV		-	-	0.12	V
88-1	Double ASY method 1	DAM1	Double ASY method	-350	-250	-150	mV
88-2	Double ASY method 2	DAM2		150	250	350	mV
88-3	Double ASY method 3	DAM3		-650	-500	-350	mV
88-4	Double ASY method 4	DAM4		350	500	650	mV
89	FZC threshold voltage	VFZC	Interface logic	35	69	100	mV
90	Anti-shock detect H	VATSCH		7	32	67	mV
91	Anti-shock detect L	VATSCL		-67	-32	-7	mV
92	TZC threshold voltage	VTZC		-30	0	+30	mV
93	SSTOP threshold voltage	VSSTOP		-150	-65	-30	mV
94	Tracking gain win T1	VTGWT1		200	250	300	mV
95	Tracking gain win T2	VTGWT2		100	150	200	mV
96	Tracking gain win I1	VTGWI1		250	300	350	mV
97	Tracking gain win I2	VTGWI2		150	200	250	mV
98	Tracking BAL win T1	VTGW11		-50	0	+50	mV
99	Tracking BAL win T2	VTGW12		-40	0	+40	mV
100	VREG voltage	VREG	Reference voltage	3.20	3.45	3.65	V
101	Reference voltage	VREF		-100	0	+100	mV
102	Reference current H	IREFH		-100	0	+100	mV
103	Reference current L	IREFL		-100	0	+100	mV

Table 2. Electrical Characteristics (Continued)

No	Item	Symbol	Block	Min	Typ	Max	Unit
104	F.Servo off offset	VOSF1	Focus servo	-100	0	+100	mV
105	F.Servo DAC on offset	VOSF2		0	+250	+500	mV
106	F.Servo auto offset	VAOF		-75	0	+75	mV
107	F.Servo auto istat	VISTAT2		4.3	-	-	V
108	FERR febias status	VFEBIAS		-50	0	+50	mV
109	F.Servo loop gain	GF		19	21.5	24	dB
110	F.Servo output voltage H	VFOH		4.4	-	-	V
111	F.Servo output voltage L	VFOL		-	-	0.75	V
112	F.Servo maximum output voltage H	VFOMH		3.68	-	-	V
113	F.Servo maximum output voltage L	VFOML		-	-	1.32	V
114	F.Servo osillation voltage	VFOSC		0	+100	+185	mV
115	F.Servo feed through	GFF		-	-	-35	dB
116	F.Servo search voltage H	VFSH		+0.35	+0.50	+0.65	V
117	F.Servo voltage L	VFSL		-0.65	-0.50	-0.35	V
118	Focus full gain	GFSFG		40.0	42.5	45.0	dB
119	F.Servo AC gain 1	GFA1		19.0	23.0	27.0	dB
120	F.Servo AC phase 1	PFA1		30	65	90	deg
121	F.Servo AC gain 2	GFA2		14.0	18.5	23.0	dB
122	F.Servo AC phase 2	PFA2		30	65	90	deg
123	F.Servo mutting	GMUTT		-	-	-15	dB
124	F.Servo AC charac. 1	GFAC1		0.75	0.85	0.95	-
125	F.Servo AC charac. 2	GFAC2		0.68	0.78	0.88	-
126	F.Servo AC charac. 3	GFAC3		0.60	0.70	0.80	-
127	F.Servo AC charac. 4	GFAC4		0.68	0.78	0.88	-
128	F.Servo AC charac. 5	GFAC5		0.94	1.04	1.14	-
129	F.Servo AC charac. 6	GFAC6		0.73	0.83	0.93	-
130	T.Servo DC gain	GTO	Tracking servo	12.5	15.0	17.5	dB
131	T.Servo off offset	VOST1		-100	0	+100	mV
132	T.Servo DAC offset	VTDAC		150	320	550	mV
133	T.Servo on offset	VOST2		-350	0	+350	mV
134	T.Servo auto offset	VTAOF		-50	0	+50	mV
135	T.Servo oscillation	VTOSC		0	+100	+185	mV

Table 2. Electrical Characteristics(Continued)

No	Item	Symbol	Block	Min	Typ	Max	Unit
136	T.Servo ATSC gain	GATSC	Tracking servo	17.5	20.5	23.5	dB
137	T.Servo lock gain	GLOCK		17.5	20.5	23.5	dB
138	T.Servo gain up	GTUP		17.5	20.5	23.5	dB
139	T.Servo output voltage H	VTSH		4.48	-	-	V
140	T.Servo output voltage L	VTSL		-	-	0.52	V
141	T.Servo maximum output voltage H	VTSMH		3.68	-	-	V
142	T.Servo minimum output voltage L	VTSML		-	-	1.32	V
143	T.Servo jump H	VTJH		0.35	0.5	0.65	V
144	T.Servo jump L	VTJL		-0.65	-0.5	-0.35	V
145	T.Servo DIRC H	VDIRCH		0.35	0.5	0.65	V
146	T.Servo DIRC L	VDIRCL		-0.65	-0.5	-0.35	V
147	T.Servo output voltage L	GTFF		-	-	-39	dB
148	T.Servo AC gain 1	GTA1		9.0	12.5	16.0	dB
149	T.Servo AC phase 1	PTA1		-140	-115	-90	deg
150	T.Servo AC gain 2	GTA2		17.5	21.5	25.5	dB
151	T.Servo AC phase 2	PTA2		-195	-135	-100	deg
152	T.Servo full gain	GTFG		29.5	32	34.75	dB
153	T.Servo AC charac. 1	GTAC1		0.59	0.69	0.90	-
154	T.Servo AC charac. 2	GTAC2		0.75	0.85	0.95	-
155	T.Servo AC charac. 3	GTAC3		0.65	0.75	0.85	-
156	T.Servo AC charac. 4	GTAC4		1.30	1.35	1.50	-
157	T.Servo AC charac. 5	GTAC5		1.15	1.25	1.35	-
158	T.Servo AC charac. 6	GTAC6		1.01	1.11	1.21	-
159	T.Servo loop mute	TSMUTE		-250	0	+250	mV
160	T.Servo loop mute AC	TSMTAC		0	+50	+100	mV
161	T.Servo INT mute M1	TSMTM1		0	+50	+100	mV
162	T.Servo INT mute M2	TSMTM2		0	+50	+100	mV
163	T.Servo INT mute M4	TSMTM4		0	+50	+100	mV
164	SL.Servo DC gain	GSL	Sled servo	20.5	22.5	24.5	dB
165	T.Servo FEED through	GSLF		-	-	-34.5	dB
166	SL.Servo DC lock	SLOCK		0	+50	+100	mV
166-1	SL.Servo lock 2	SLOCK2		20.5	22.5	24.5	dB

Table 2. Electrical Characteristics(Continued)

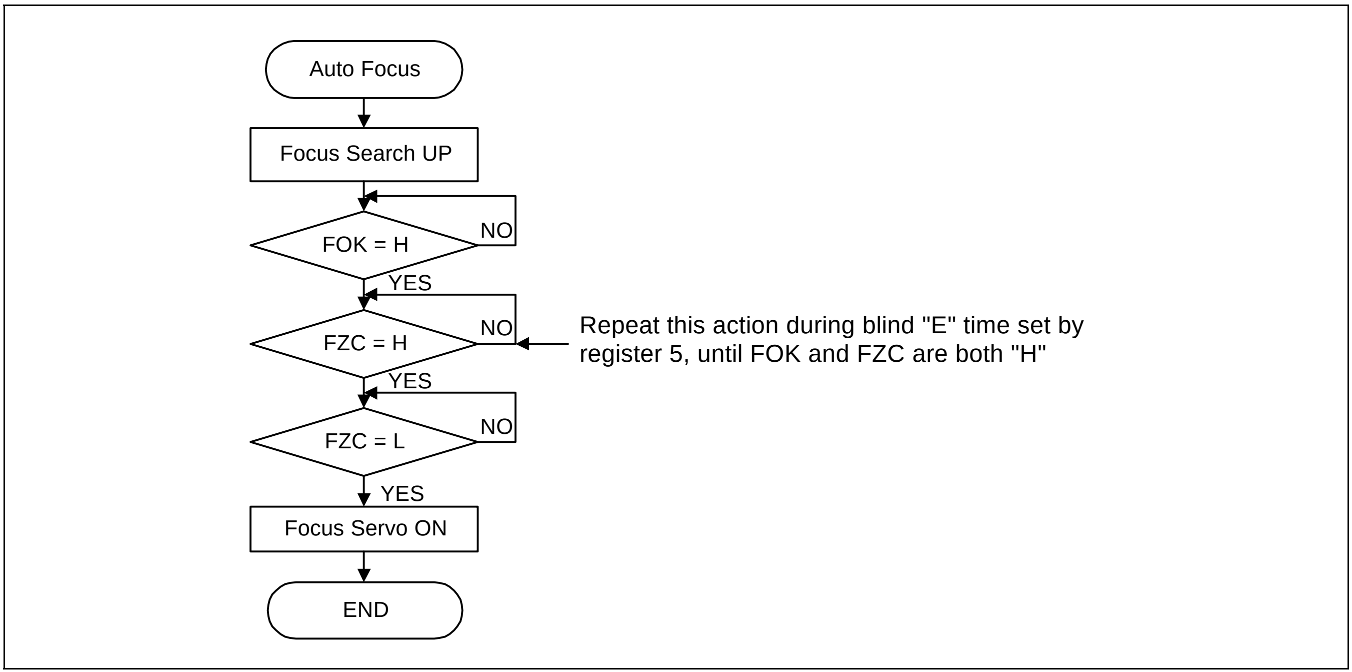
No	Item	Symbol	Block	Min	Typ	Max	Unit
167	Sled forward kick	VSKH	Sled servo	0.38	0.60	0.75	V
168	Sled reverse kick	VSKL		-0.75	-0.60	-0.38	V
169	Sled output voltage H	VSLH		4.48	-	-	V
170	Sled output voltage L	VSLL		-	-	0.52	V
171	Sled maximum output voltage H	VSLMH		3.68	-	-	V
172	Sled minimum output voltage L	VSLML		-	-	1.32	V
173	SP.Servo 1X gain	GSP	Spindle servo	14.0	16.5	19.0	dB
174	SP.Servo 2X gain	GSP2		19.0	23.0	27.0	dB
175	SP.Servo output voltage H	VSPH		4.48	-	-	V
176	SP.Servo output voltage H	VSPL		-	-	0.52	V
177	SP.Servo maximum output voltage H	VSPMH		3.68	-	-	V
178	SP.Servo minimum output voltage L	VSPML		-	-	1.32	V
179	SP.Servo AC gain 1	GSPA1		-7.0	-3.5	0	dB
180	SP.Servo AC phase 1	PSPA1		-120	-90	-60	deg
181	SP.Servo SMEF gain	GSMEF		13.0	16.5	20.0	dB
182	SP.Servo AC gain 2	GSPA2		-3.0	9.0	12.5	dB
183	SP.Servo AC phase 2	PSPC2		-120	-90	-60	deg

AUTO-SEQUENCE

This feature automatically carries out the following commands: Auto-focus, track jump, and move. During auto-sequence, it latches the data when MLT is L, and outputs H when ISTAT is L and at the end.

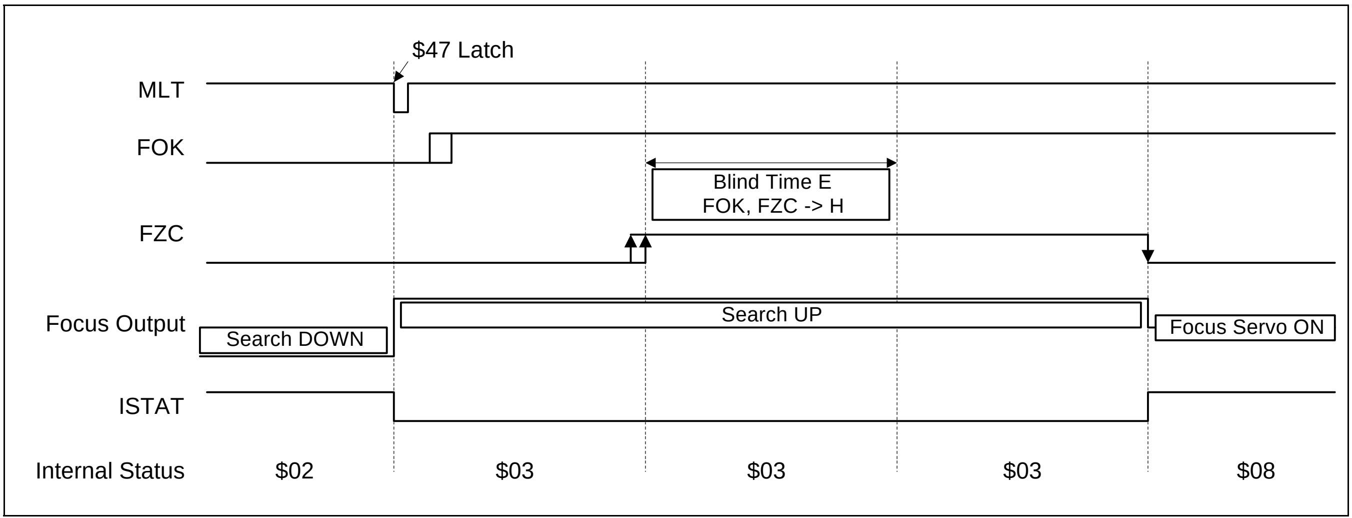
AUTO FOCUS

Flow CHart



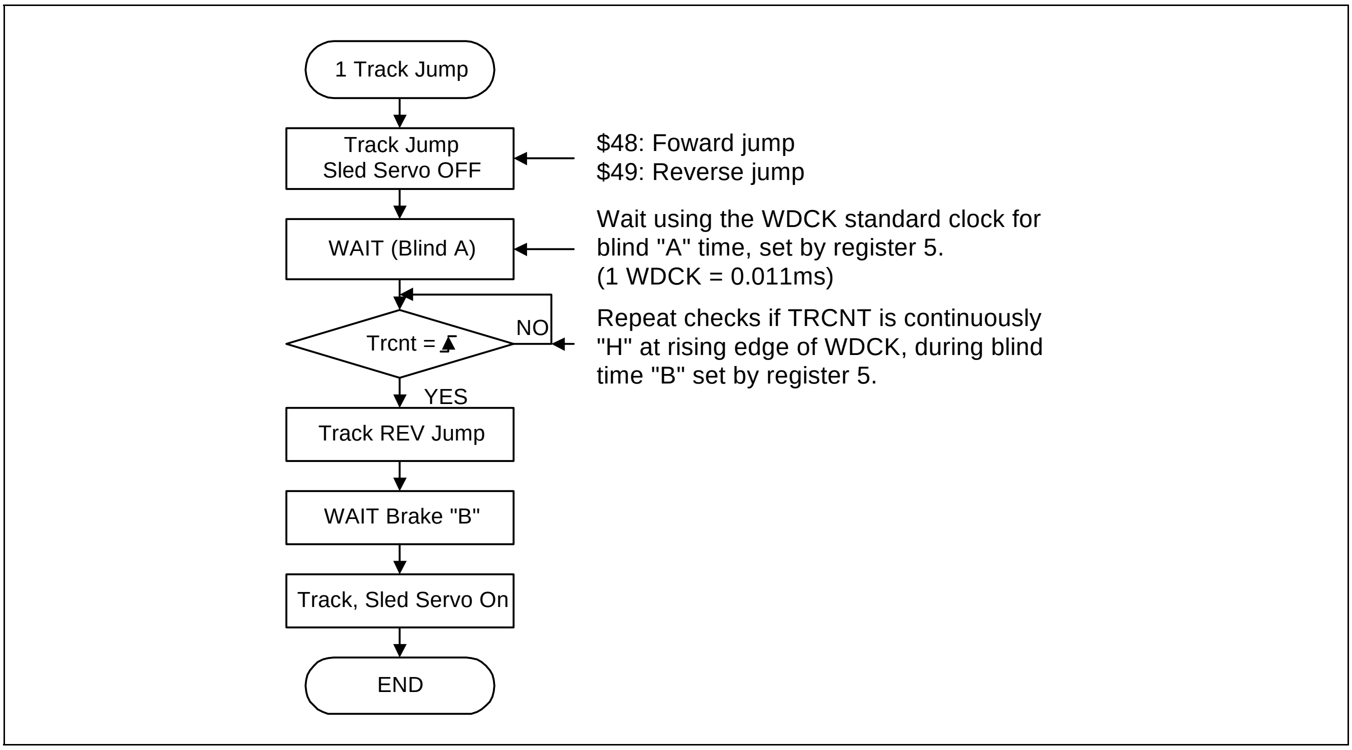
Timing Chart

The auto-focus carries out the focus search up by receiving the auto-focus command from micom in focus search down status. SSP is focus servo on when the internal FOK and FZC satisfy the all H time set blind E (register $5X) and transfer FZC to L. Then the internal auto-focus is finished, and transmitted to MICOM through the ISTAT output.



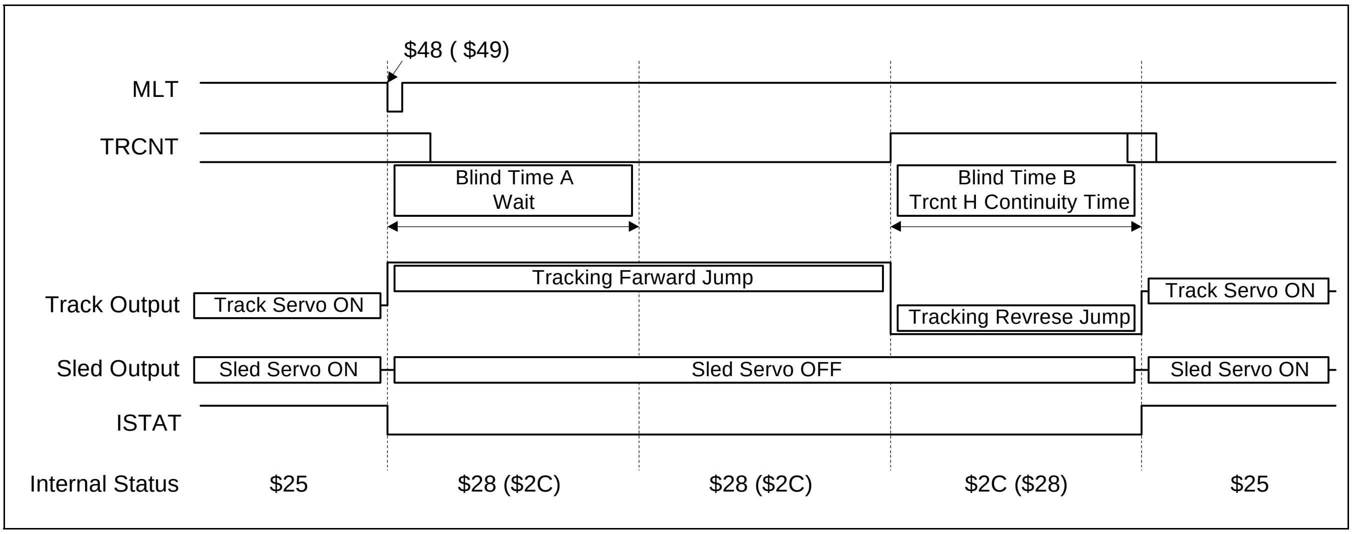
1 TRACK JUMP {$48 (FWD), $49 (REV)}

Flow-Chart



Timing Chart

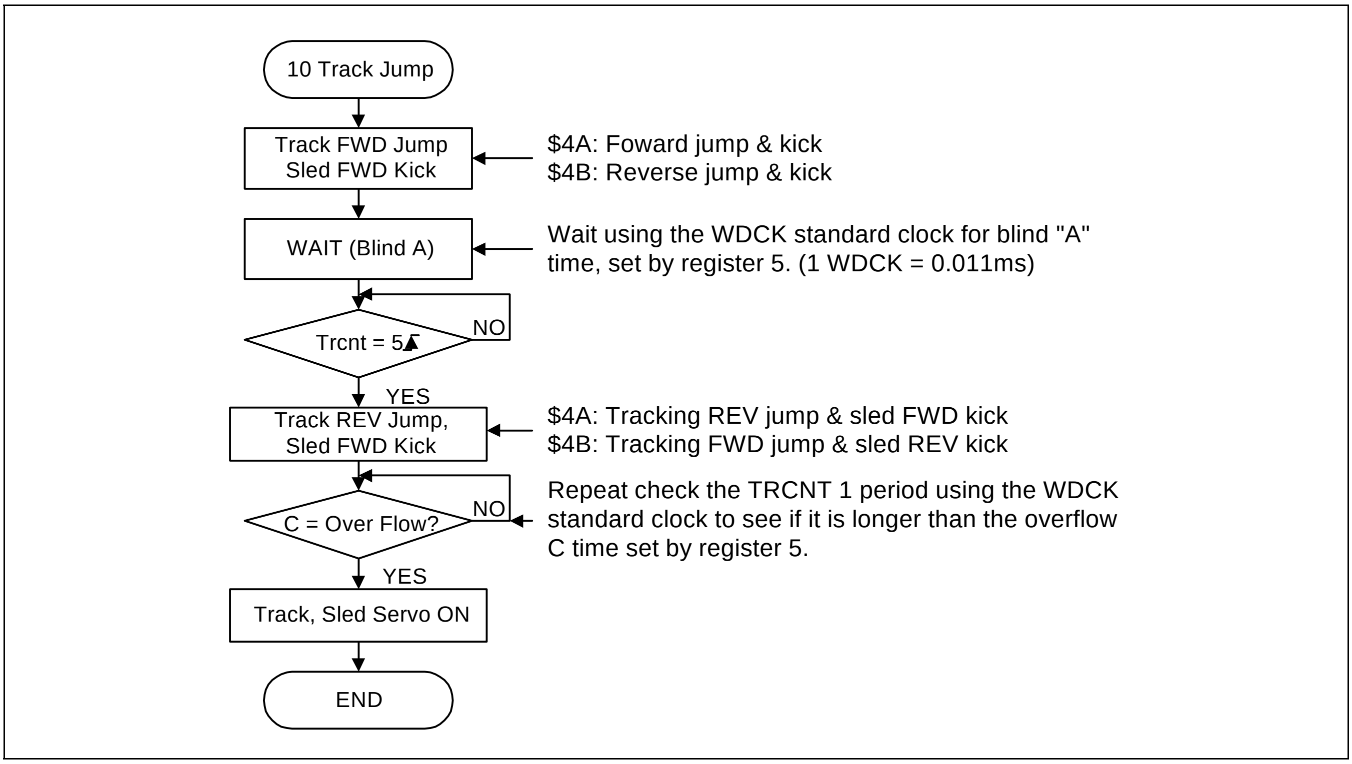
Track Jump is carried out after receiving $48 ($49), and the blind time and the brake time is set by register $5X.



NOTE: Inside () means reverse.

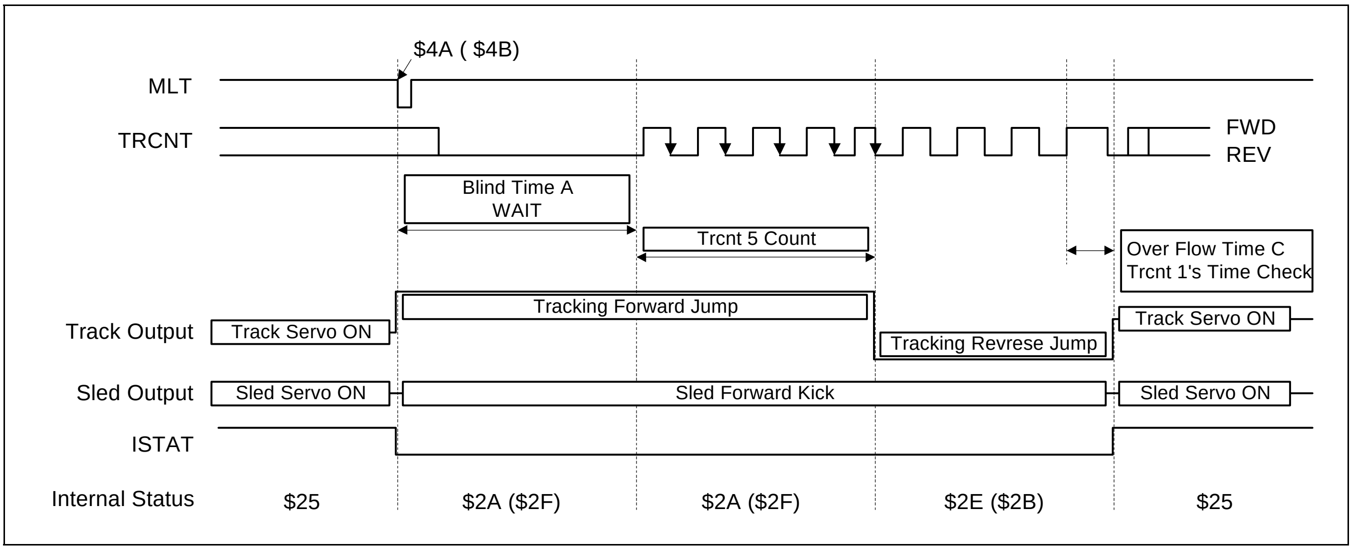
10 TRACK JUMP {$4A (FWD), $4B (REV)}

Flow-Chart



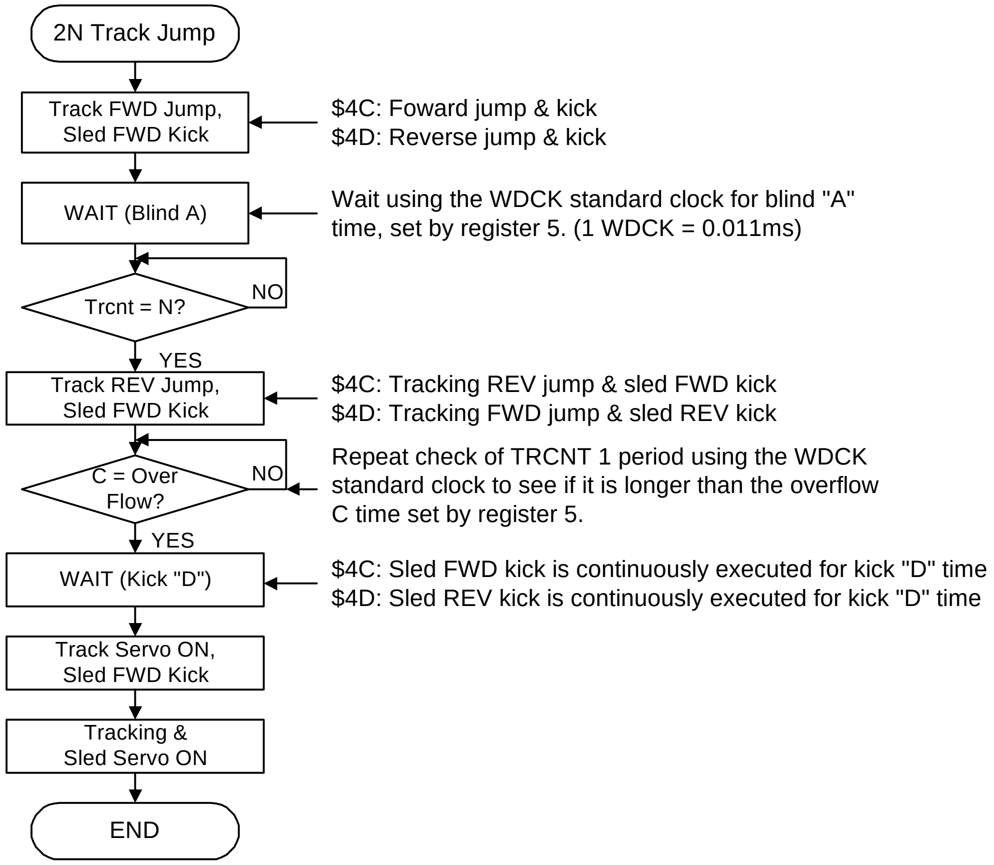
Timing Chart {$4A(FWD), $4B(REV), inside () is Reverse}

10 track jump carries out tracking forward jump until the trcnt 5 track count. It carries out tracking reverse jump until one period of trcnt is longer than the overflow C select time, then turns the tracking servo and sled servo on. This function is to check if the actuator speed is enough to turn the servo on.



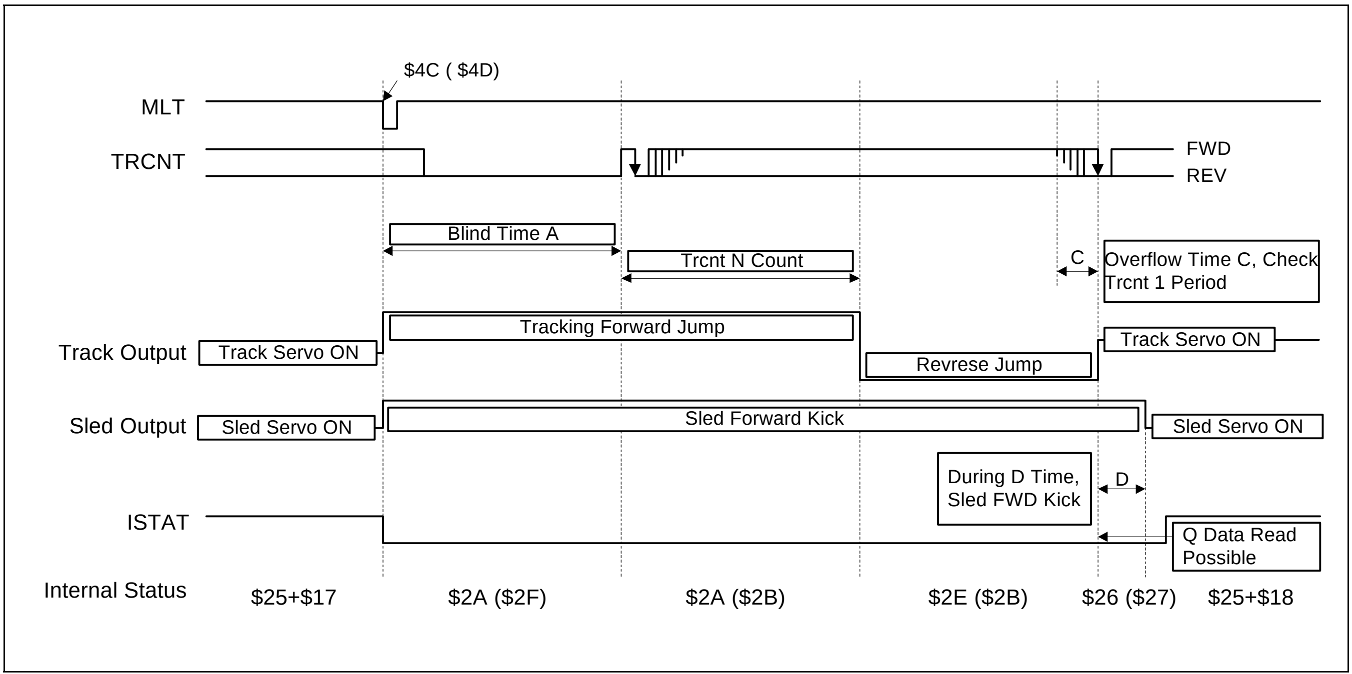
2N TRACK JUMP

Flow-Chart



2N TRACK JUMP {$4C(FWD), $4D(REV), INSIDE () IS REVERSE}

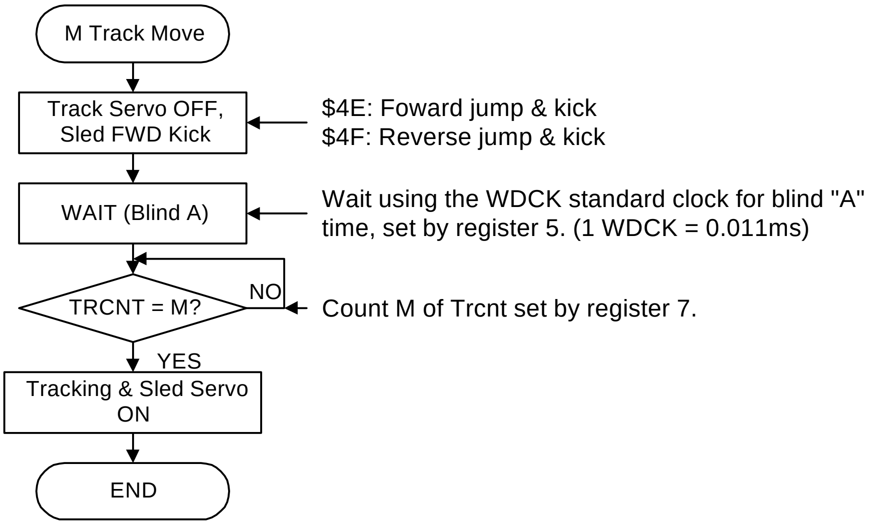
Timing Chart



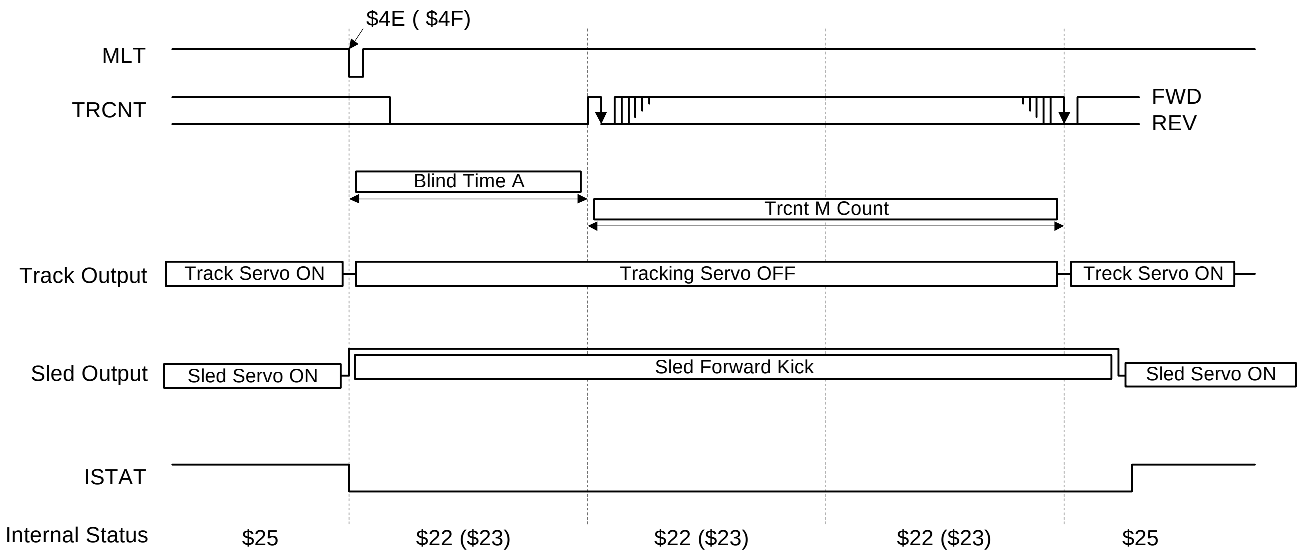
Similar to 10 track. Kick D time is added to the sled kick and carried out. Servo is turned on after lens brake execution.

M TRACK JUMP {$4E(FWD), $4F(REV)}

Flow-chart



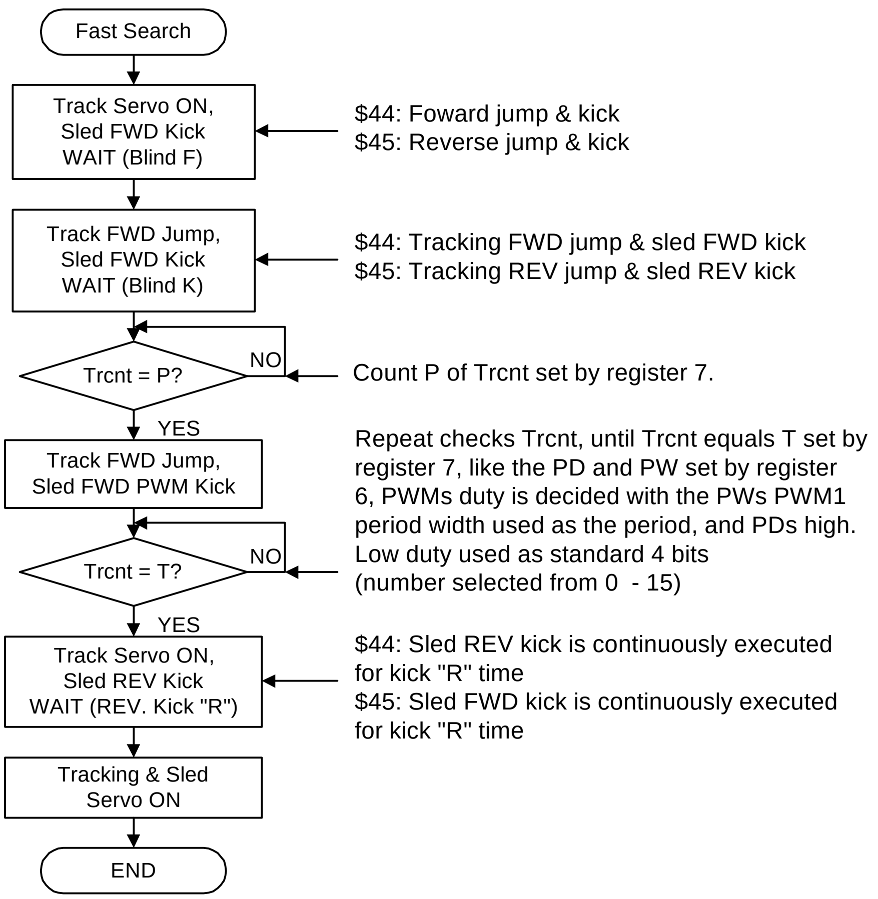
Timing Chart {$4E(FWD), $4F(REV), inside () is Reverse}



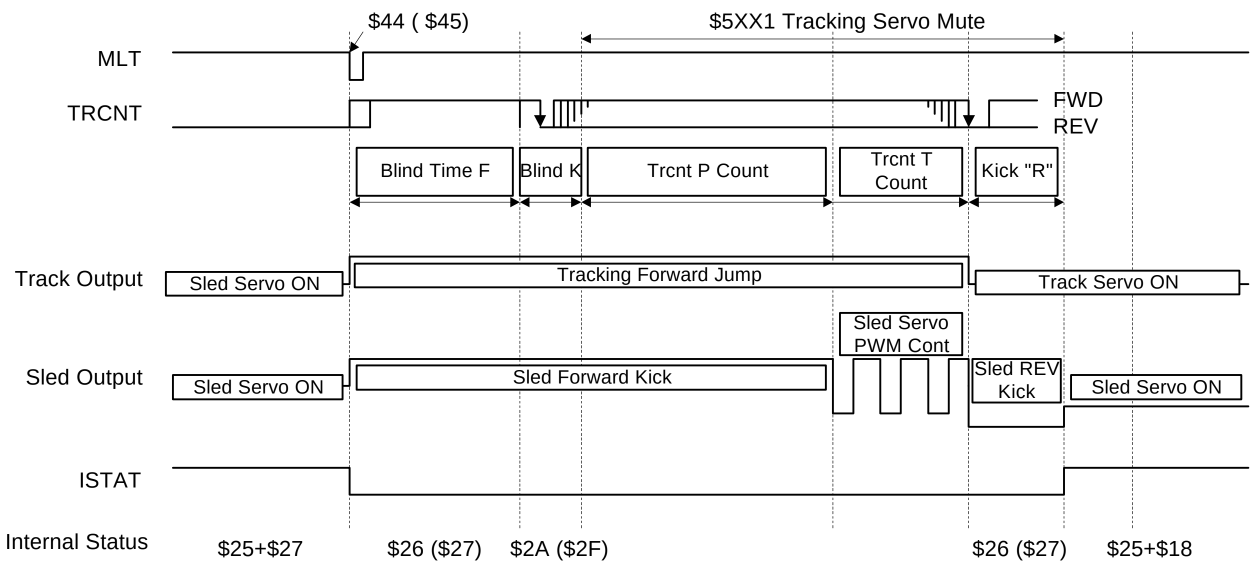
Sled kick is carried out by counting Trcnt for the set M count value set by register 7, using the clock.

FAST SEARCH

Flow-Chart



Timing Chart



Suggestions for Using Auto-Sequence

- Tracking gain up and brake on ($17) must be transmitted when carrying out 1, 10, 2n, track jump, and fast search.
- The entire auto-sequence modes MLT becomes L, and the sequence process is carried out at the initial WDCK falling edge after data latch.
- Please JUDGE play status not by Istat, but by FOK and GFS.
- Tracking gain up, brake, anti-shock and focus gain down are not carried out in auto-sequence, and needs a separate command.
- If the auto-sequence does not operate as Istat max time over, apply $40 and clear the Ssps internal status, then try again.
- The WDCK mentioned above is input from DSP as 88.2kHz (2x → 196kHz). Also, it is possible to choice 3 mode (88, 176, 500kHz) by DSP command setting.
- 2N and M track have the potential for errors within the algorithm, when jumping more than 512 tracks, so please TRY to limit use for track jumps within 512.
- Please limit the use of the fast-search algorithm for more than 512 tracks.

AUTOMATIC ADJUST COMMAND

Tracking Balance, Gain Adjust

Address (13bit command)	Address			Data						Istat	Trcnt
	D8	D7	D6	D5	D4	D3	D2	D1	D0		
Tracking balance $80XX - $81XX	0	0	0	B5	B4	B3	B2	B1	B0	BAL	TRCNT
Initial value				0	1	1	1	1	1		

Address (12bit command)	Address			Data						Istat	Trcnt
	D7	D6	D5	D4	D3	D2	D1	D0			
Tracking gain $81XX - $83XX	0	0	0	G4	G3	G2	G1	G0		TGH	TGL
Initial value				1	0	0	0	0			

Tracking Balance, Gain Adjust Window

Address	Data				ISTAT	TRCNT
	D3	D2	D1	D0		
$84XX	Tracking gain adjust window trcnt: ISTAT 0-250mV: 200mV 1-150mV: 300mV	Tracking balance adjust window 0: -10mV-15mV 1: -20mV-20mV	Focus. servo offset adjust 0: Off 1: On	Fe.bias offset adjust 0: Off 1: On	$841 (F.ERR) $842 (F.SER)	TRCNT
Initial value	0	0	0	0		

APC (Automatic Power Control)

Address	Data								
	D7 LDON	D6 PNSEL	D5 INTC2	D4 INTC	Tracking S. Window Mute (88.2kHz)	D3 FLAGSEL	D2 FLAGCON	D1 FLAGINV	D0 CLOCK
$85XX	APC On/off 0: APC on 1: APC off	APC P/N sel 0: PSUB 1: NSUB	0	0	11kHZ - 0.7kHZ	0: Hard control 1: Micom data	Micom data 0: Flag SW-on 1: Hflag SW-off	0: FALGB H: SW on 1: FLAG H: SW off	0: Lock = 1 internal lock = 1 1: Lock (0,1)
			1	0	CPEAK (RF)				
			0	1	5.5kHz - 0.7kHz				
			1	1	2.7kHz - 0.7kHz				
Initial Value	1	0	0	0		0	1	1	1

Register Set 1

<table>
<tr><th rowspan="2">Address</th><th colspan="8">Data</th></tr>
<tr><th>D7
F.SER.RE
SEL</th><th>D6
FOKSEL</th><th>D5
MONITOR</th><th>D4
FSOC</th><th>D3
DSP4</th><th>D2
DSP3</th><th>D1
DSP2</th><th>D0
DSP1</th></tr>
<tr><td>$84XX</td><td>Focus servo offset adjust reset
0: Reset
1: Reset cancel</td><td>Trcnt output sel (monitor:1) except for gain control ($82x-$83x)
0: FOK
1: TRCNT</td><td>Trcnt monitor select
0: Test output
1: FOK, TGL, Trcnt</td><td>FERR. offset focus offset adjust step time setup
0: 46.0ms
1: 5.80ms</td><td>92.87ms</td><td>46.4ms</td><td>23.2ms</td><td>11.6ms</td></tr>
<tr><td>Initial V.</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td></td><td colspan="8">TRCNT select is chosen by the MONITOR(D1), TGL is output when tracking gain adjust command ($82X-$83X) is given. Others when FOKSEL is “0”, FOK is output to the TRCNT pin, when “1” COUT is output.
DSP4 - DSP1: Flag hold time converse by total 16 steps. Default: 0101 (58ms)</td></tr>
</table>

Register Set 2

<table>
<tr><th rowspan="2">Address</th><th colspan="9">Data</th></tr>
<tr><th>D7
DIRCI</th><th>D6
RSTF</th><th>D5
AGCL1</th><th>D4
AGCL2</th><th>D3
ELOCK</th><th>D2
MT0</th><th>D1
MT1</th><th>D0
MT2</th><th>–</th></tr>
<tr><td rowspan="8">$87XX</td><td rowspan="8">DIRC 0, 1 control</td><td rowspan="8">FEBIAS reset
0: Reset
1: Reset cancel</td><td colspan="2" rowspan="8">AGC gain adjust
D5 D4
0 0 1.6V
0 1 1.45V
1 0 1.25V
1 1 1.0V</td><td rowspan="8">0: Off
1: On
Envelope lock = 1 mode conversion</td><td>0</td><td>0</td><td>0</td><td>CPEAK</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>FSCMPO</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>BALH</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>C1flag</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>DFCINT</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>FECMPO</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>BALL</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>LOVKG</td></tr>
<tr><td>Initial V.</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td></td></tr>
</table>

Register Set 3

Address	Data								
	D7 EC8	**D6 EC7**	**D5 EC6**	**D4 EC5**	**D3 EC4**	**D2 EC3**	**D1 EC2**	**D0 EC1**	**–**
$8EXX	Track. servo freq. move EC7 EC8 0 0 1 0 0 1 1 1	Track. servo freq. move freq. 1.2K 1.3K 1.4K 1.5K	Track. servo phase shift on/off 0: Off 1: On	Track. servo gain shift on/off 0: Off 1: On	Focus. servo freq. move EC4 EC3 0 0 1 0 0 1 1 1	Focus. servo freq. move freq. 1.2K 1.3K 1.4K 1.5K	Focus. servo gain shift on/off 0: Off 1: On	Focus. servo phase shift on/off 0: Off 1: On	
Initial V.	0	0	0	0	0	0	0	0	

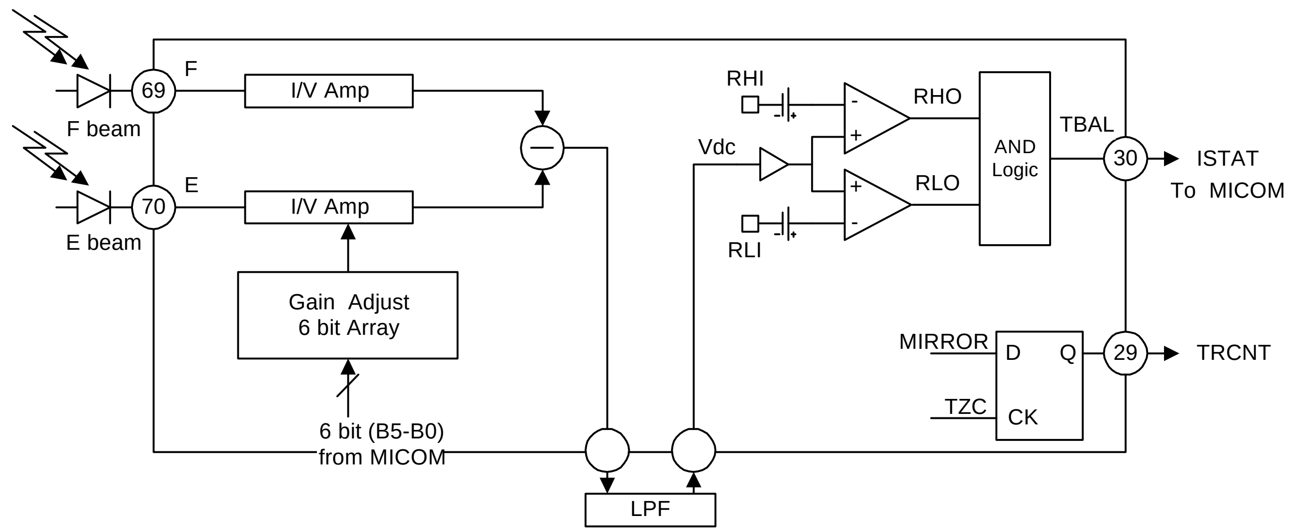
Register Set

$8FXX - Tracking GServo offset adjust command

Address	Data								
	D7 TEST	**D6 EC10**	**D5 EC9**	**D4 TOA4**	**D3 TOA3**	**D2 TOA2**	**D1 TOA1**	**D0 TOA0**	**–**
$8FXX	FOK defect mirror output on/off 0: On 1: Off	Front ASY gain 0: 1x 1: 2X	ENVELOPE gain sel 0: 2x 1: 1.5x	Tracking servo offset adjust command 8F (001XXXXX) $8F3F → $8F20 (-160mV → +160mV) Adjustment window used by balance window istat output monitor - Tracking offset value (+30mV - +50mV) is iedal system. After offset (0mV), adjust ($8F3F → $8F20) upper 3-5 step. Consider what to set.					
Initial V	0	0	0	1	0	0	0	0	

TRACKING BALANCE ADJUST CONCEPT

The tracking balance adjust automatically adjusts using the following process: The tracking error DC offset extracted from the pre-set DC voltage window level, and the external LPF are comparison monitored by MICOM.



Process Summary

Tracking balance adjust is accomplished in the following manner: With the focus on and spindle servo on, the tracking and sled servo loop is turned off to make the tracking loop into an open loop. The error signal which has passed through the wide-range pick-up and the tracking error amp, passes through the external LPF to extract the DC offset. The DC offset is compared with the pre-selected window comparator level to extract the tracking error amps DC offset within the window, to inform MICOM using the ISTAT that the balance adjust is complete.

At this time, Tracking E beam-side I/V amps gain is selected by MICOM, and the 6-bit resistance arrays resistance value is selected by the 6-bit control signal.

The values that MICOM applies are 000000 → 111111. If you select the switch, TE1s DC offset increases the (2.5V-ΔV) → (2.5V + ΔV) one step at a time, to enter the pre-selected DC window level. When it enters that level, the balance adjust is completed, and the switch condition is latched at this time.

In this adjust process, the TE1 signals frequency distribution is from DC to 2kHz, so if DC components are included, the DC offset which passed LPF are not accurate DC values. Therefore, if the frequency of the TE1 signal is above 1kHz, MICOM monitors the window comparator output. The frequency check at this time monitors the trcnt pin. Balance adjust completes the adjustment when the TBAL output is H.

	Vdc < RLI < RHI	**RLI < Vdc < RHI**	**RLI < RHI < Vdc**
RHO	H	H	L
RLO	L	H	H
TBAL (AND gate)	L	H	L

- RHI: High level threshold value
- RLI: Low level threshold value
- Vdc: Window comparator input voltage
- TBAL: Window comparator outputs and gate output value

Tracking Balance Adjust Example

Out of \$80000 → \$81F80 128 steps, the 88 steps excepting the upper and lower 20 steps, are used (\$80400-\$81A80). The limit adjust flow applies the gain to \$830 at the focus, tracking on point, and checks the TRCNTs frequency. Check if 7 TRCNT came in during 10 ms, and if the answer is YES, check ISTAT, and if NO, repeat the TRCNT number check 3 times, then go to ISTAT Check.

If the 3x repeat fails as well, increase the balance switch one step.

Also, just in case ISTAT does not immediately go to H when ISTAT checking, wait 10ms. Check if it is H after the 3x repeat, and if not, increase the balance switch one step. Adjust the wait mentioned above 10ms, when the system is running.

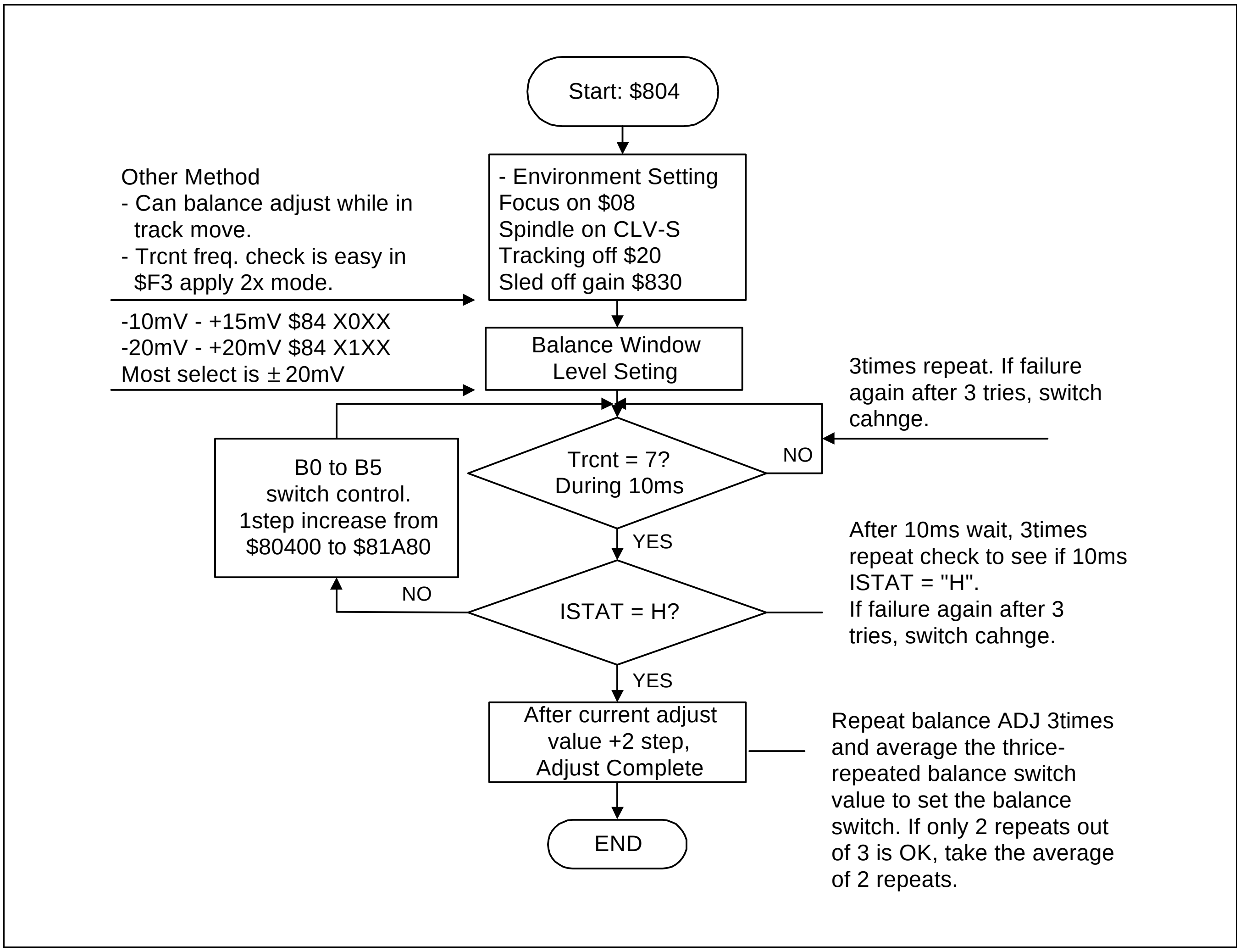
Average the values found by repeating the balance adjust three times.

If only two out of the three tries were successful in getting a balance value, average the two values.

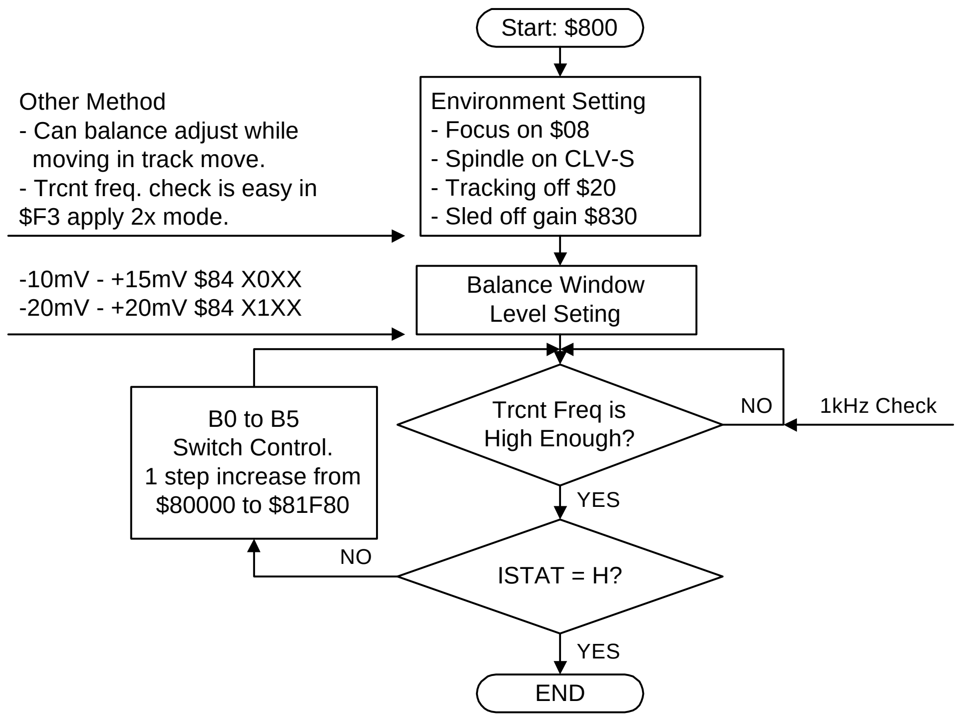
Set as balance switch, this average value, +2. This is because the balance for the system and the minus value for the DC is stable in the system.

Precision is important in balance adjust, and about 1-2 sec is spent as adjust time, which is accounted for.

Balance Adjust Flowchart 1



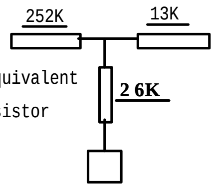
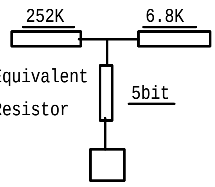
Balance Adjust Flowchart 2



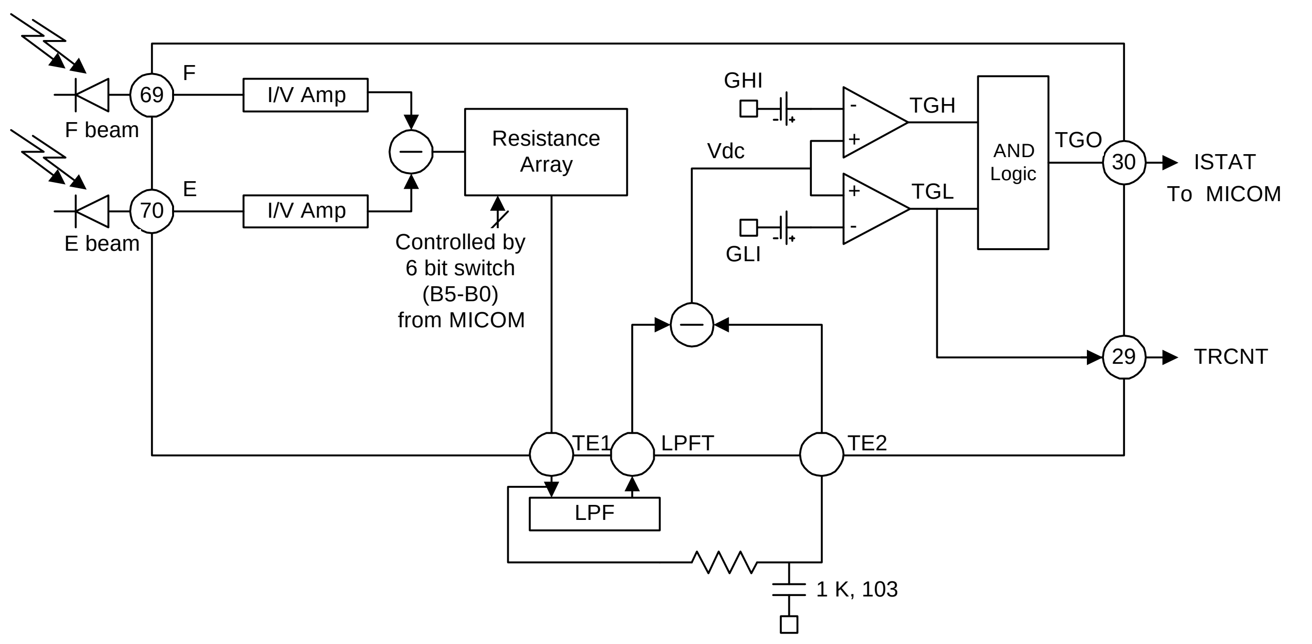
When Executing Tracking Balance Adjust

- The balance adjust is from $80000 to $81F80, and the switch mode is changed one STEP at a time by 13-bit data transmission. After adjust is completed, a separate latch pulse is not necessary.
- If the trcnt freq. is not high enough, the balance can be adjusted at $F3 applied 2x mode.
- Here, we have suggested tracking off status for the balance adjust, but the same amount of flow can be balance adjusted while in track move.
- The tracking balance window select level can be selected by D2 bit out of 12-bit data. 0: -10mV - +15mV, 1: -20mV - +20mV.
- When the tracking balance adjust is complete, start the tracking gain adjust.

Tracking Balance Equivalant register

	Tracking Balance			Fixed R and Parallel R Value		Variable Resistor (5bit)					
DATA	TE1 offset	F Eqa.	E R Equ.	75K // 5bit R	5bit Equ.	13K	27K	56K	110K	220K	Note
$800		391K	531K	6.29K	6.87K	1	1	1	1	1	F Equivalent Resistor 
$801		391K	523.6K	6.47K	7.09K	1	1	1	1	0	
$802		391K	515K	6.68K	7.33K	1	1	1	0	1	
$803		391K	507.5K	6.89K	7.58K	1	1	1	0	0	
$804		391K	500.5K	7.09K	7.84K	1	1	0	1	1	
$805		391K	492.5K	7.33K	8.12K	1	1	0	1	0	E Equivalent Resistor 
$806		391K	484.8K	7.58K	8.44K	1	1	0	0	1	
$807		391K	477.1K	7.85K	8.77K	1	1	0	0	0	
$808		391K	467.5K	8.21K	9.22K	1	0	1	1	1	
$809		391K	459.7K	8.52K	9.62K	1	0	1	1	0	
$80A	+	391K	451K	8.88K	10.1K	1	0	1	0	1	1) 220K//110K=73.33K
$80B		391K	444.8K	9.21K	10.5K	1	0	1	0	0	2) 56K//27K=18.21K
$80C		391K	437K	9.62K	11.0K	1	0	0	1	1	3) 27K//13K=8.775K
$80D		391K	429.4K	10.0K	11.6K	1	0	0	1	0	4) 110K//56K=37.10K
$80E		391K	422K	10.5K	12.2K	1	0	0	0	1	5) (1)//(2)=14.58K
$80F		391K	413.5K	11.0K	13K	1	0	0	0	0	6) (3)//(4)=7.09K
$810		391K	398.4K	12.2K	14.6K	0	1	1	1	1	7) 56K//13K=10.55K
$811		391K	391.6K	12.9K	15.6K	0	1	1	1	0	8) (1)//(7)=9.223K
$812		391K	383.8K	13.7K	16.8K	0	1	1	0	1	9) 56K//220K=44.63K
$813		391K	376K	14.6K	18.2K	0	1	1	0	0	A)56//110/220=31.74K
$814	↓	391K	368.6K	15.6K	19.7K	0	1	0	1	1	B)13//56//110=9.62K
$815		391K	360.8K	16.8K	21.6K	0	1	0	1	0	C)(1)//27K=19.73K
$816	−	391K	353K	18.2K	24K	0	1	0	0	1	D)27K//110K=21.67K
$817		391K	345K	19.8K	27K	0	1	0	0	0	E)27K//220K=24.04K
$818		391K	336K	22.3K	31.7K	0	0	1	1	1	
$819		391K	327.9K	24.8K	37.1K	0	0	1	1	0	
$81A		391K	320K	27.9K	44.6K	0	0	1	0	1	
$81B		391K	312K	32.1K	56K	0	0	1	0	0	
$81C		391K	305K	37K	73.3K	0	0	0	1	1	
$81D		391K	297K	44.6K	110K	0	0	0	1	0	
$81E		391K	289K	55.9K	220K	0	0	0	0	1	
$81F		391K	282K	75K	0K	0	0	0	0	0	

GAIN ADJUSTMENT



Process Summary

The signal TE1 output by the tracking error amp outputs resistance divide (DC+AC) passes through LPF and the DC offset extract signal (DC) difference AMP. Only pure AC components are compared with the pre-selected window comparators gain select value to carry out the tracking gain adjustment.

The resistance divide changes the 5-bit resistance combination with the MICOM command, to change the gain. tracking gain adjustment is carried out in the same conditions as balance adjustment, which is: focus loop on, spindle servo on, tracking servo off and sled servo off. It adjusts the tracking error amps gain and the wide-rage Pick-ups amount of reflection.

The external LPFs cut-off frequency is set to 10Hz - 100Hz.

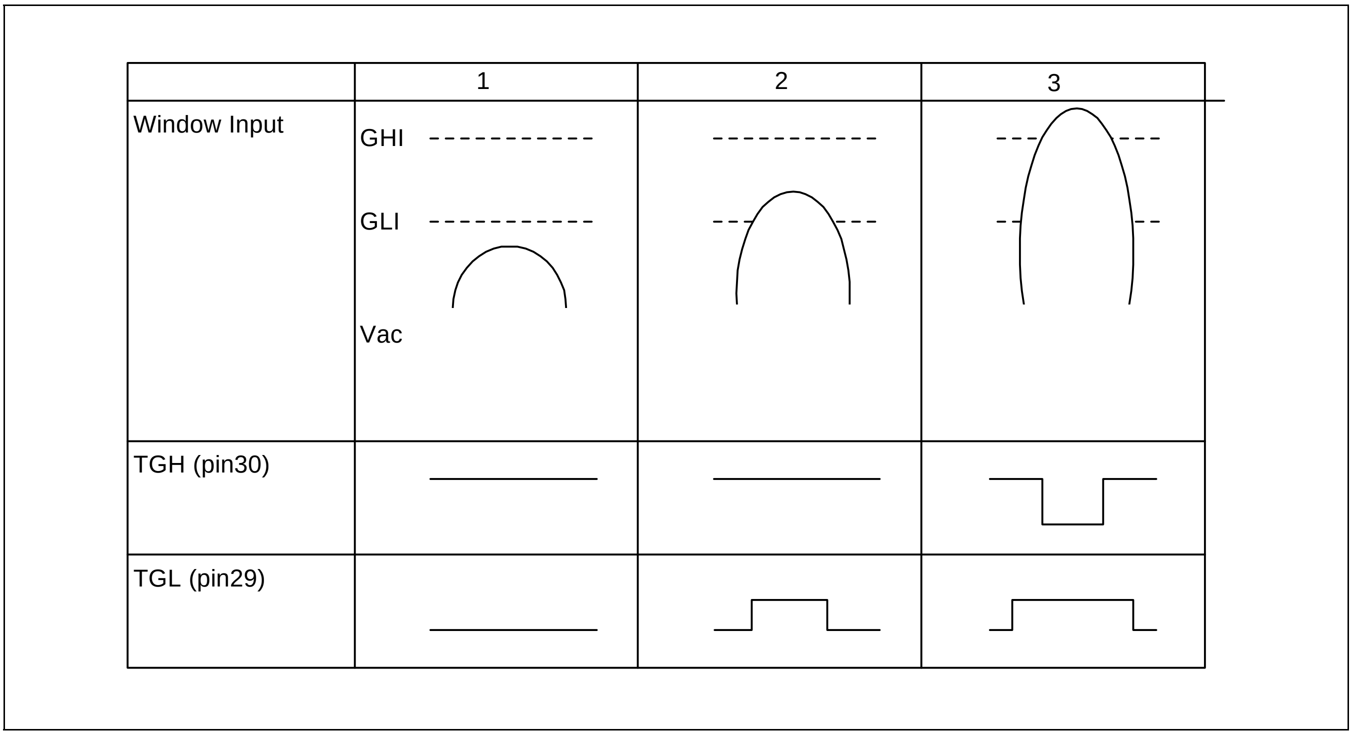
The window comparators comparison level can be chosen from +150mv - +300mV, and +250mV - +200mV by MICOM command.

TGL outputs +150mV and +250mV comparator output to TRCNT.

TGH outputs +300mV and +200mV comparator output to ISTAT.

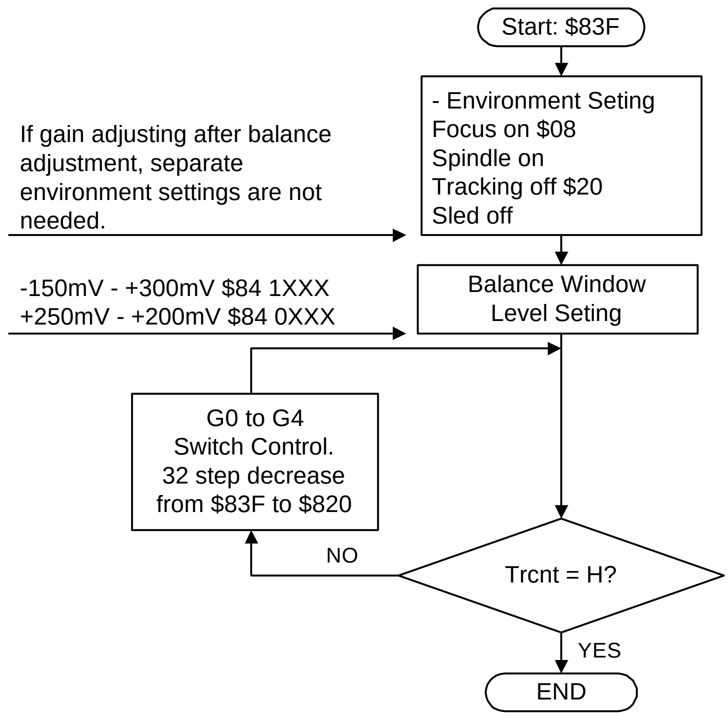
	Vac < GLI < GHI	GLI < Vac < GHI	GLI < GHI < Vac
TGH (ISTAT output)	H	H	L
TGL (TRCNT output)	L	H	H

Gain Adjustment is complete when the output is H.



When Adjusting the Tracking Gain

- In gain adjustment, the switch mode is changed one step at a time from \$83F → \$820 by 12-bit data transmission. A separate latch pulse is not needed after adjust completion.
- Trcnt and TGAL outputs H duty check standard is above 0.1ms.
- Adjustment is carried out by choosing the most appropriate out of the 4 adjustment modes, including the ones listed above.
- The tracking balance window select level can be selected by the D3 bit out of the 12-bit data.
  0: +250mV (TGL) - +200mV (TGH)
  1: +150mV (TGL) - +300mV (TGH)
- When tracking gain adjustment is complete, tracking & sled servo loop on and TOC read is initiated.



Gain adjust proceeds from status 1 → 2 → 3 when the MICOM command carries out down command from $83F → $820, in order. Adjustment is complete when in status 2.

Gain Adjustment Method 1
MICOM monitors trcnts TGL output, and if the outputs H duty (0.1ms) is detected, the adjustment is complete. At this time, the window comparator level is +150mV - +300mV.

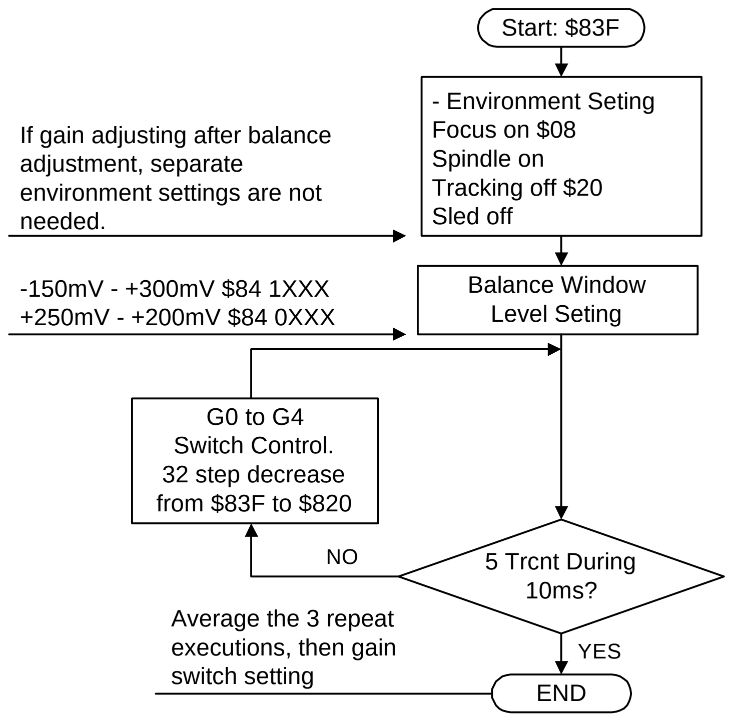
Gain Adjustment Method 2
MICOM monitors ISTATs TGO output, and if the outputs H duty (0.1ms) is detected, the adjustment is complete. At this time, the window comparator level is +150mV - +300mV.

Gain Adjustment Method 3
MICOM monitors Trcnts TGL output, and if the outputs H duty (0.1ms) is detected, the Window Comparator Level is changed from +150mV - +300mV to +250mV - +200mV. And when MICOM again monitors Trcnts TGL output and the outputs H duty (0.1 ms) is detected, the adjustment is complete. If you latch the former MICOM command value and the latter MICOM command values median, it is possible to Gain adjust +200mV.

Gain Adjustment Method 4
MICOM monitors Trcnts TGL output, and if the outputs H duty (0.1ms) is detected, MICOM command goes 1 step down, and adjustment is completed. At this time, the window comparator level is +150mV - +300mV.

Gain Adjustment Method 5
Gain adjustment is set to a total of 32 steps, and gain window is set to +250mV. That is, the process starts at $83F and carries on to $820. It first sets $83F, monitors the Trcnt pin and checks if 5 Trcnt were detected during 10ms. If YES, adjustment is complete, and if NO, carry on lowering the gain switch 1 step at a time. Repeat the above process three times and set the gain adjustment switch with the average value.

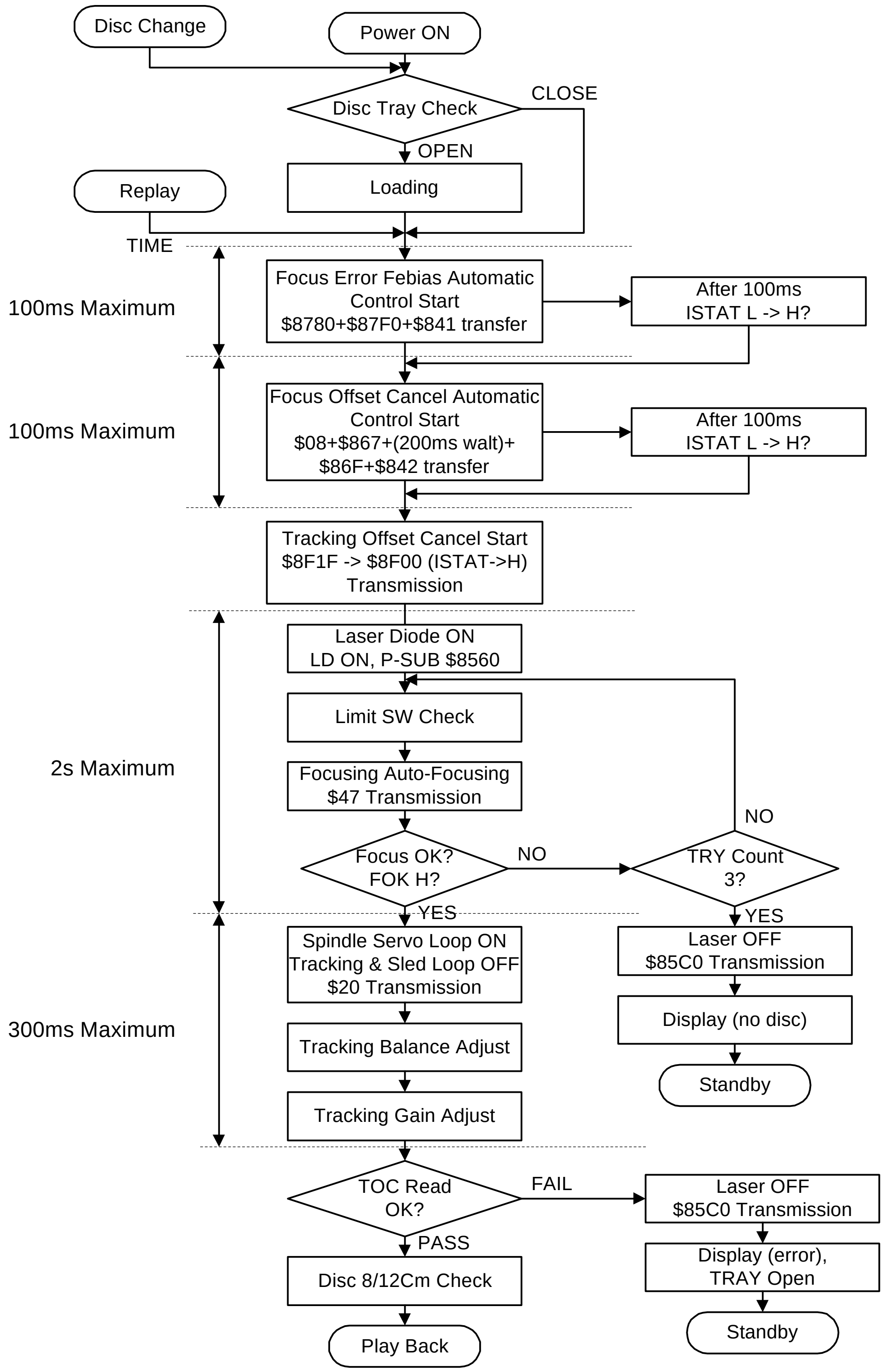
Gain Adjustment Flowchart 2



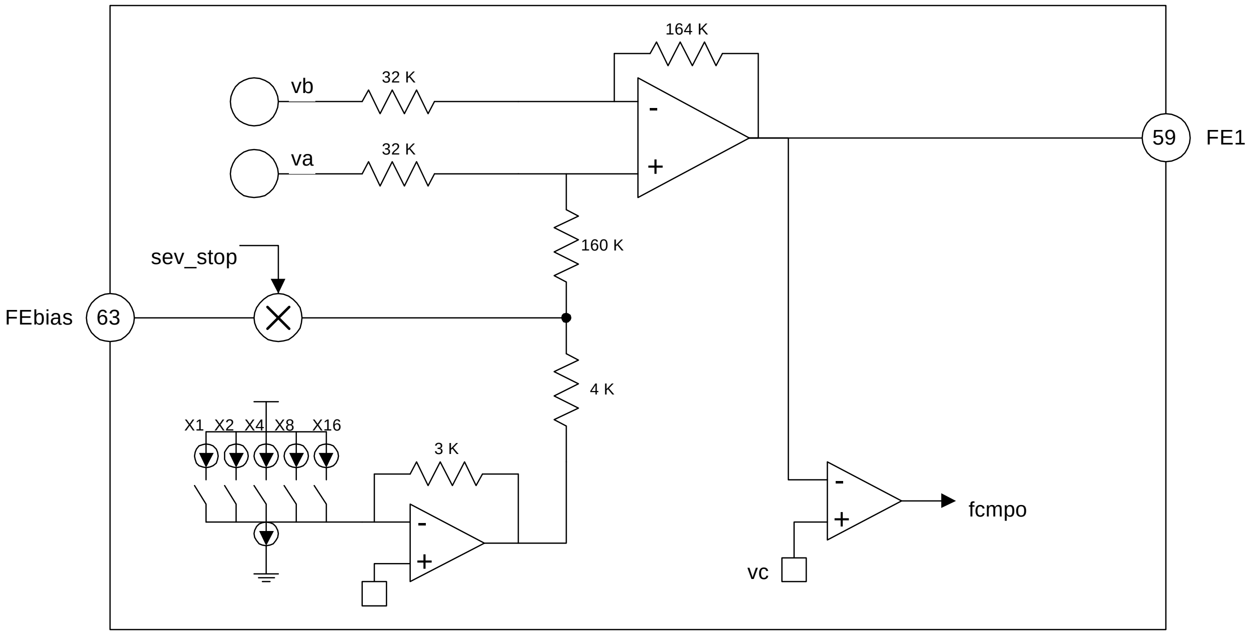
Tracking Gain Equivalant Resistance

	Tracking Gain										
Data	TERR Tot. Gain	TERR Gain	5bit Gain Ratio	Compared Value	Combination Value	5.0K	5.0K	2.5K	1.25K	0.75K	Note
$83F	0.108	96K / 32K -> 3.0 Times	0.036	10.0K	0.375K	1	1	1	1	1	The GAIN ratio is calculated in the TE1 pin.
$83E	0.303		0.101	10.0K	1.125K	1	1	1	1	0	
$83D	0.419		0.139	10.0K	1.625K	1	1	1	0	1	
$83C	0.575		1.191	10.0K	2.375K	1	1	1	0	0	
$83B	0.699		0.233	10.0K	2.875K	1	1	0	1	1	
$83A	0.798		0.266	10.0K	3.625K	1	1	0	1	0	
$839	0.876		0.292	10.0K	4.125K	1	1	0	0	1	
$838	0.981		0.327	10.0K	4.875K	1	1	0	0	0	
$837	1.048		0.349	10.0K	5.375K	1	0	1	1	1	
$836	1.139		0.379	10.0K	6.125K	1	0	1	1	0	
$835	1.195		0.398	10.0K	6.625K	1	0	1	0	1	
$834	1.273		0.424	10.0K	7.375K	1	0	1	0	0	
$833	1.321		0.440	10.0K	7.875K	1	0	0	1	1	
$832	1.389		0.463	10.0K	8.625K	1	0	0	1	0	
$831	1.431		0.477	10.0K	9.125K	1	0	0	0	1	
$830	1.490		0.496	10.0K	9.875K	1	0	0	0	0	
$82F	1.52		0.506	5.23K	5.375K	0	1	1	1	1	
$82E	1.618		0.539	5.23K	6.125K	0	1	1	1	0	
$82D	1.676		0.558	5.23K	6.625K	0	1	1	0	1	
$82C	1.755		0.585	5.23K	7.375K	0	1	1	0	0	
$82B	1.800		0.600	5.23K	7.875K	0	1	0	1	1	
$82A	1.8675		0.622	5.23K	8.625K	0	1	0	1	0	
$829	1.907		0.635	5.23K	9.125K	0	1	0	0	1	
$828	1.961		0.653	5.23K	9.875K	0	1	0	0	0	
$827	1.994		0.664	5.23K	10.375K	0	0	1	1	1	
$826	2.040		0.680	5.23K	11.125K	0	0	1	1	0	
$825	2.069		0.689	5.23K	11.625K	0	0	1	0	1	
$824	2.108		0.702	5.23K	12.375K	0	0	1	0	0	
$823	2.133		0.711	5.23K	12.875K	0	0	0	1	1	
$822	2.167		0.722	5.23K	13.625K	0	0	0	1	0	
$821	2.188		0.729	5.23K	14.125K	0	0	0	0	1	
$820	2.219		0.739	5.23K	14.875K	0	0	0	0	0	

Example of System Control Program



FEBIAS OFFSET ADJUST



MICOM sends the febias offset adjust command $841 to start the adjustment. In the focus error amp final output block, the focus output is compared with the 1/2 VDD. If the focus error amp output goes above 1/2 VDD, the Febias offset adjust is completed. The focus offset adjusts voltage change per step is about 17mV. Transition is carried out 1 step at a time from 112mV to -112mV by the total 5-bit resistance DAC, and after completion, about -8mV of offset is added to 1/2 step. Normally, the offset distribution after febias offset adjust is between -8mV - +8mV. The design is such that after focus offset, you have the option to vary the febias by turning on the switch that connects the exterior and interior of the febias block (pin 63). This control signal is Sev_stop, and it is switched on after focus servo offset adjust.

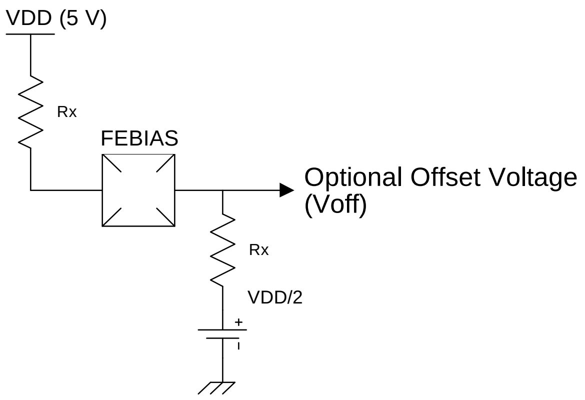
When febias block is open, the focus error offset remains unchanged, the same as febias adjust offset. The time spent per step is 5.8ms, and since there are 5 bits, a total of 32 steps and maximum 256 ms can be spent. The adjustment is carried out by hardware, and it transitions from minus offset to plus offset.

For febias offset readjust, 4-bit DAC is reset by $8780, and reset can be canceled only when the $87F0-applied D2 bit goes from 0 $\rightarrow$ 1.

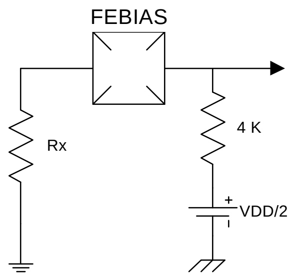
In order to prevent system errors such as static electricity, the febias DAC latch blocks reset is not carried out by the RESET block (System Reset), but by MICOM data.

FEbias Offset Setting

* Application when adjusting offset from 0mV - +100mV



* Application when adjusting offset from -100mV - 0mV

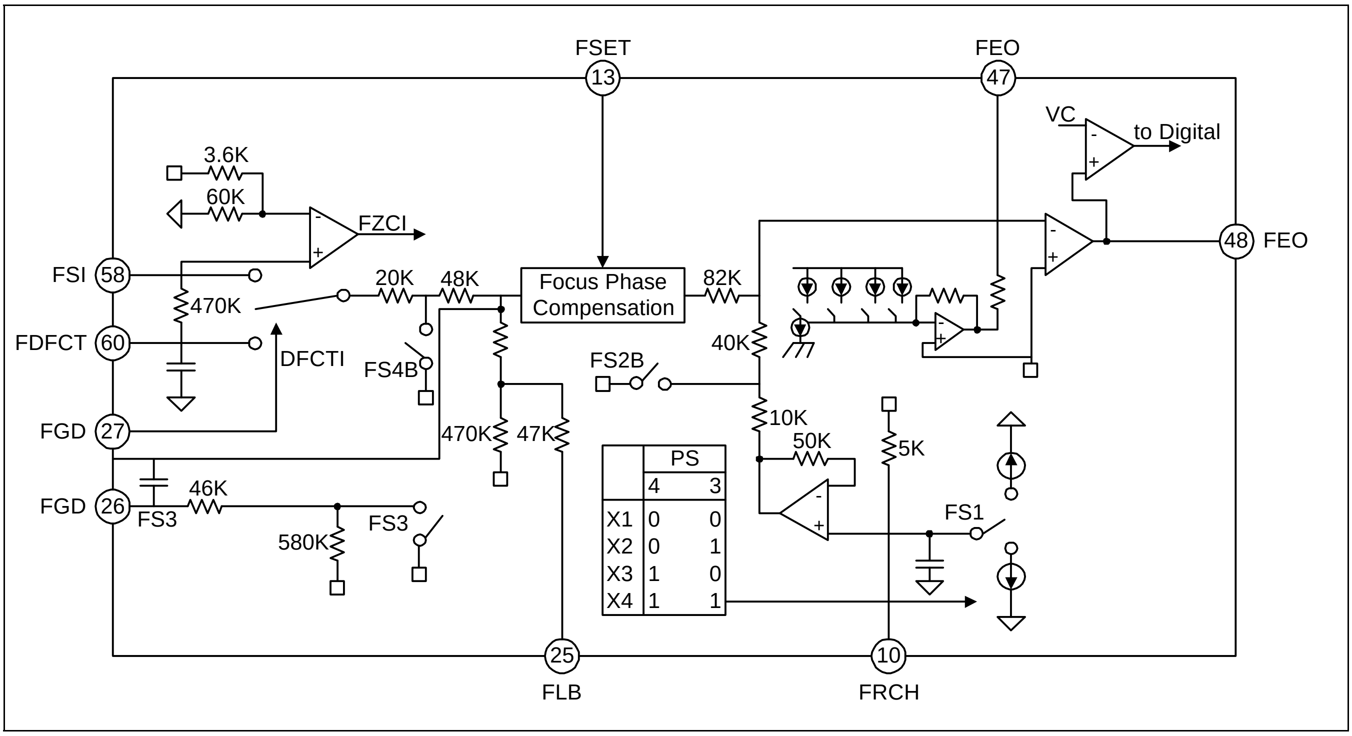


$$\frac{VDD - VDD/2}{(Rx + 4\,K)} = Voff$$

Example) When Power is 5 V

$$\frac{(5 - 2.5)\,V}{(Rx + 4\,K)}\ 4\,K = Voff \qquad \frac{10\,K}{(Rx + 4\,K)} = Voff$$

FOCUS OFFSET ADJUST



MICOM sends the focus offset adjust command $842 to start the adjustment. In the focus error amp final output block, the focus output is compared with the 1/2 VDD. If the focus error amp output goes above 1/2 VDD, the focus offset adjust is completed. The focus offset adjusts voltage change per step is about 40mV. Transition is carried out 1 step at a time from 320mV to - 320mV by the total 4-bit resistance DAC, and after completion, about +20 MVDML of Offset is added to 1/2 step. Normally, the Offset distribution after Focus Offset adjust exists between -20mV - +20mV. The design is such that after focus offset, you have the option to vary the focus by turning on the switch that connects the exterior and interior of the focus block (pin 63).

When febias block is open, the focus error offset is the same as febias adjust offset. The time spent per step is 5.8ms, and since there are 4bits, a total of 16 steps and maximum 128ms can be spent. Also, lens-collision-sounds can be generated when adjusting the pick-up with a sensitive focus actuator, so the time division that uses 46ms per step, spending a total of 736ms, is used. That is carried out by setting the $86Xs lowest D0 bit to 0. The adjustment is carried out by hardware, and it goes from minus offset to plus offset.
for febias offset readjust, 4-bit DAC is reset by $867, and reset can be canceled only when the $86F-applied D2 bit goes from 0 $\rightarrow$ 1.
In order to prevent system errors such as static electricity, the focus DAC latch blocks reset is not carried out by the RESET block (System Reset), but by MICOM data.

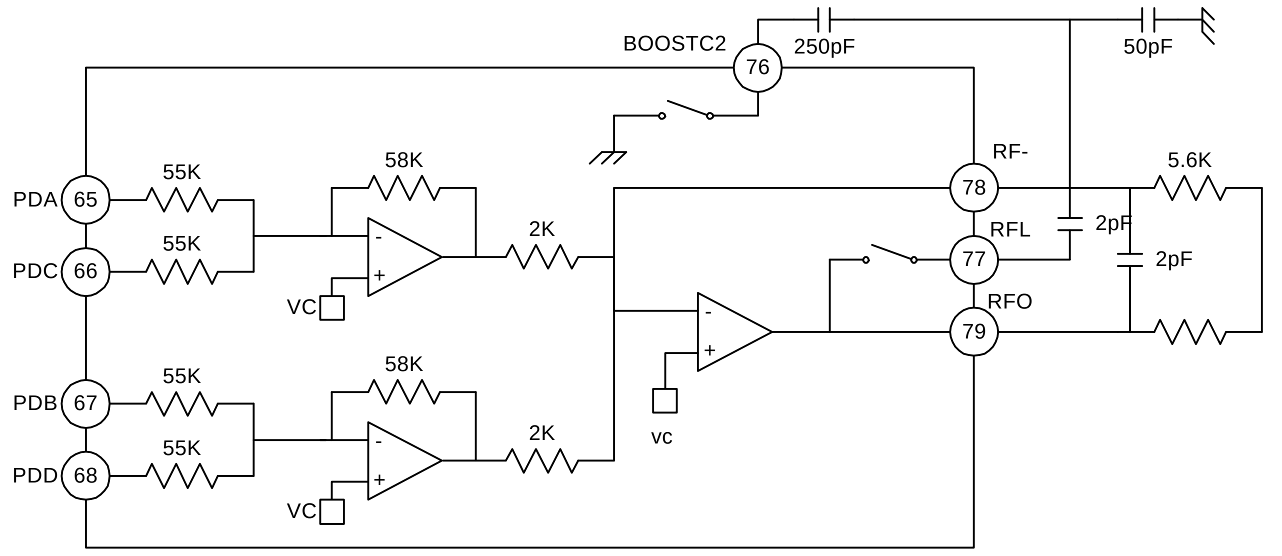
FEBIAS Adjust

FEBIAS offset is automatically adjusted from 0mV, and can be adjusted from the exterior at ±100mV. When adjusting the FEBIAS at 0mV - +100mV, RX connect to VDD, and if adjusting the FEBIAS at -100mV - 0mV, RX connect to GND.

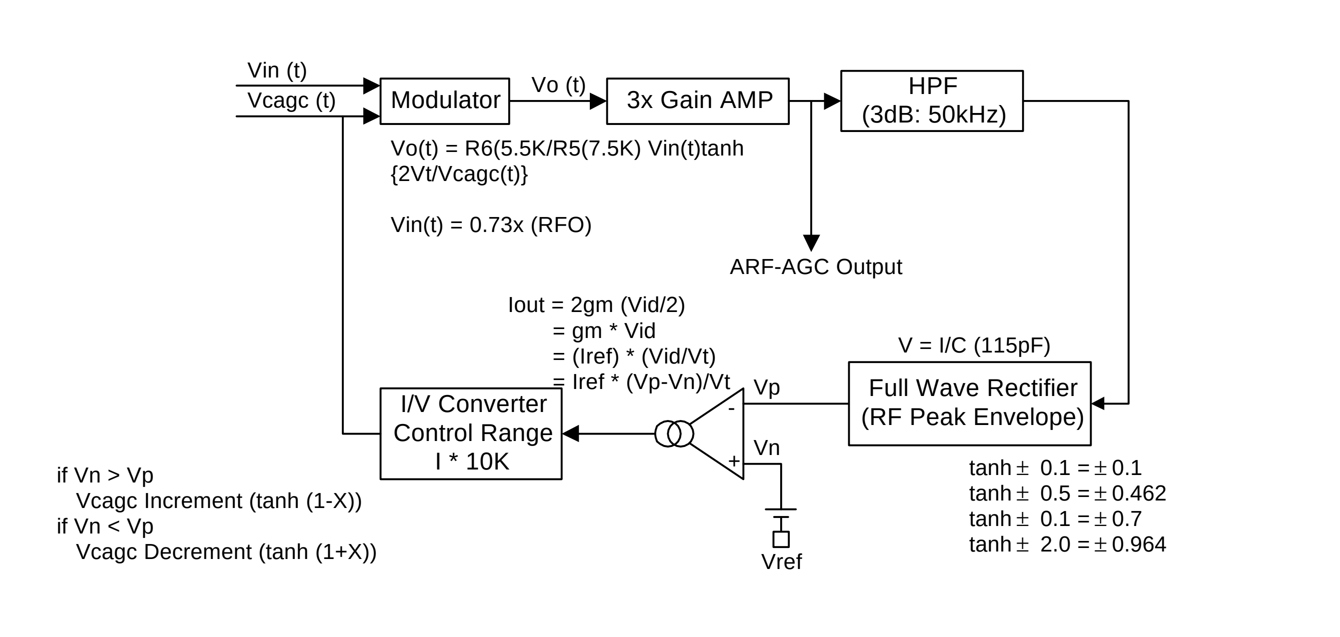
After FEBIAS offset automatic adjust is complete, the FEBIAS external resistance and focus error internal resistance is connected, so adjusting Pin 63 (FEBIAS) to an optional offset value is possible.

RF SUMMING AMPLIFIER APPLICATION

The internal switch is for selecting the 1, 2x speed-related filter. It is on when 1x, and off when 2x. please adjust the according to the set.



RF EQUALIZE & AGC



The modulator output is the product of the input and Vcagcs Tanh Term. It goes through about 3x of gain blocks, then is output to the ARF pad. The output goes through the HPF with the pole frequency of 50kHz, then is full-wave rectified to follow-up the RF levels peak envelope.

At this time, the HPFs pole frequency is set to 50kHz so that the 3t - 11t frequency components can pass without diminution. After full-wave rectification, the RF levels peak value is integrated to the 115pF CAP node. If this peak voltage is smaller than the pre-determined voltage, it outputs a sinking current, and if larger, it outputs a sourcing current. The maximum current peak value is 10uA, and this current is I/V converted and applied as a modulator control voltage.

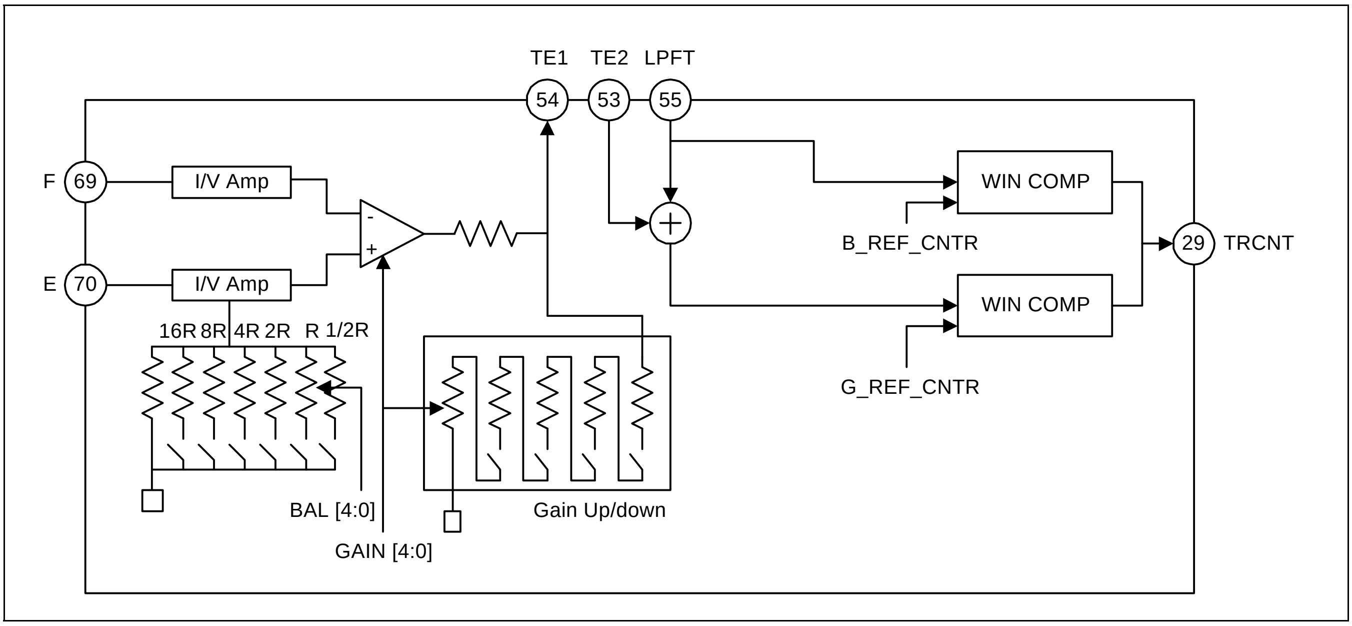
When sinking, the voltage of Vcagc is increased up to Iout x 10K and multiplied with Tanh(1-X), and when sourcing, the voltage of Vcagc is decreased to Iout x 10K and multiplied with Tanh(1+X). At this time, X is (Vcagc/2Vt).

Overall, after detecting the 3t and 11ts level by full-wave rectification, it is compared to Tanh using the modulator and multiplied to the gain to realize the wave-form equalize. The above is related to the AGC concept, which means that a specific RF level is always taken.

OTHER BLOCK

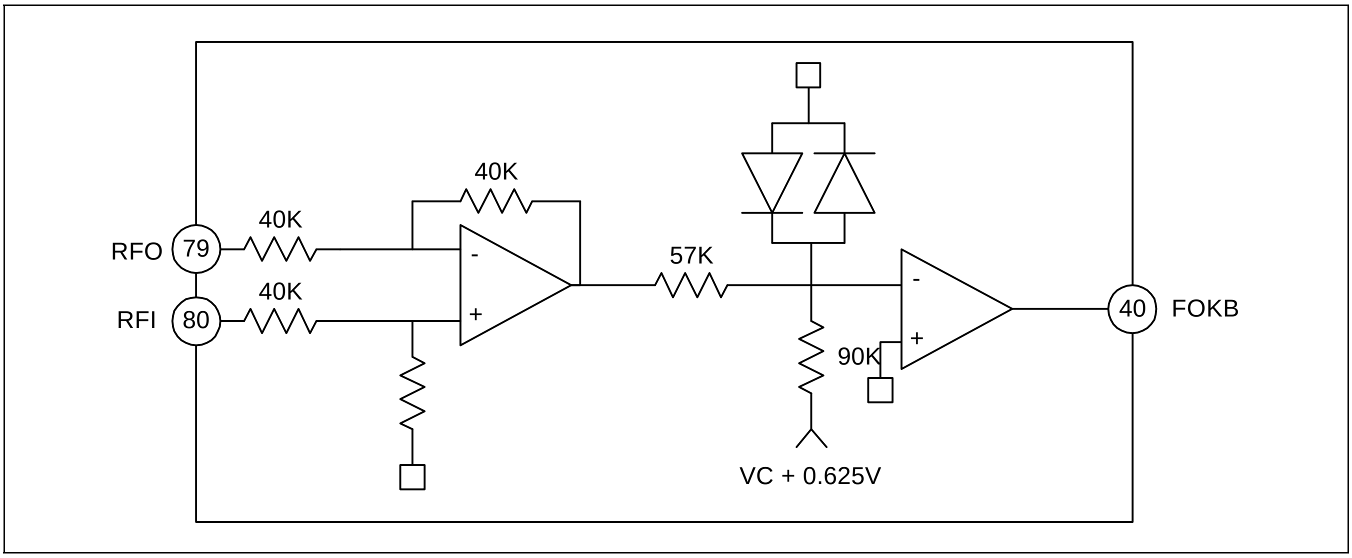
TRACKING ERROR AMPLIFIER

The side spot photo diode current which is input into blocks E and F, goes through the E loop I-V and F loop I-V AMP. It is then converted into voltage, in order to gain the difference signal in the tracking error AMP. It is MICOM programmed so that the balance is adjusted in E block, and gain is automatically adjusted in TE1.



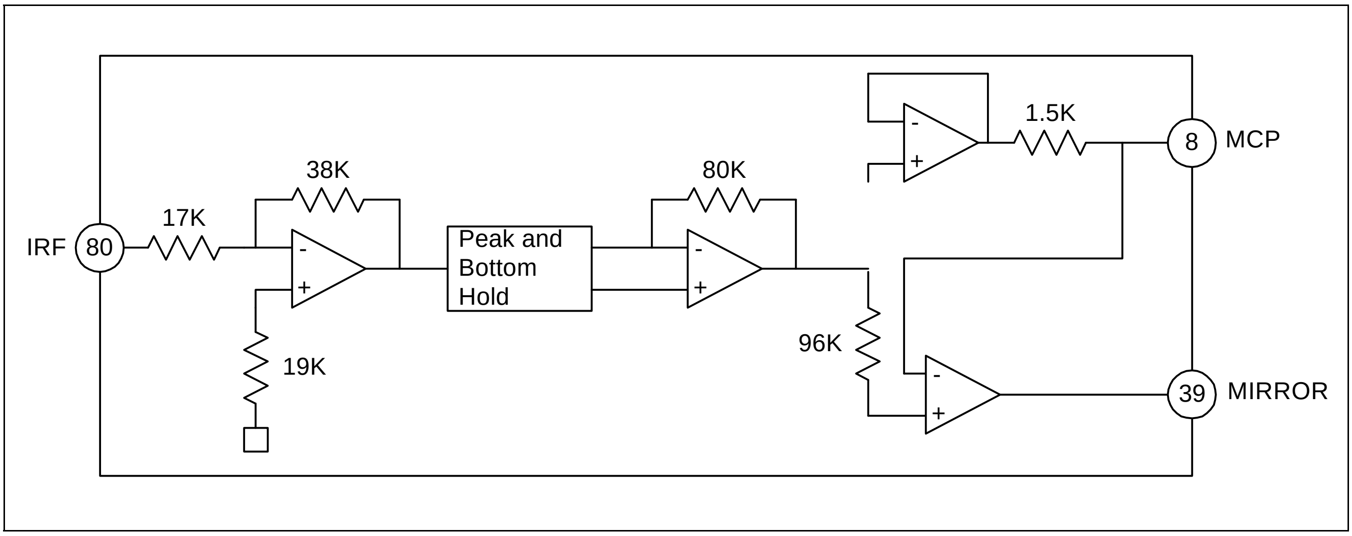
FOCUS OK CIRCUIT

The focus ok circuit compares the DC difference value between the RFI and RFO blocks to the standard DC value. If the RF level is above standard, FOK outputs L → H to make a timing window for turning the focus on during focus search status.



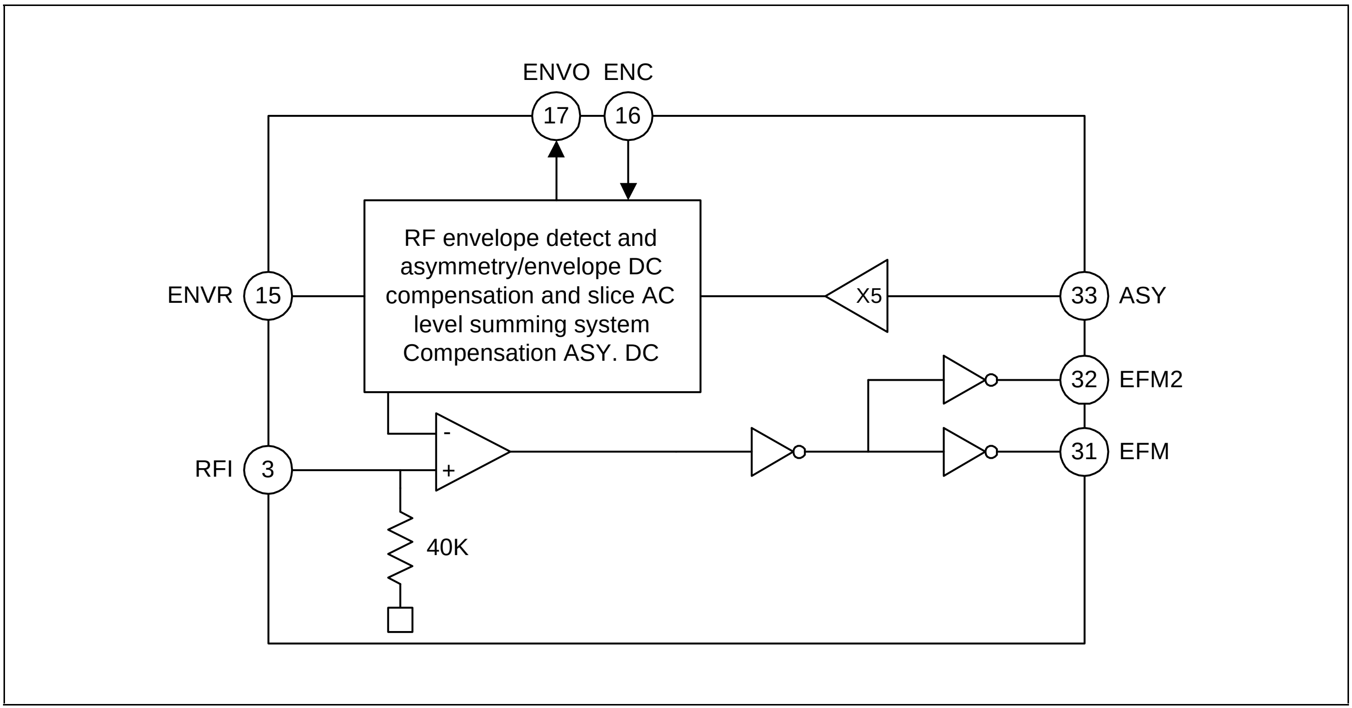
MIRROR CIRCUIT

The mirror signal amplifies the RFI signal, than peak and bottom holds it. Peak hold can follow-up on defect-type traverse, and bottom hold can follow-up on RF envelope to count the tracks. The mirror output is the following: L within DISC tracks, H between tracks, and H when a defect above 1.4ms is detected.



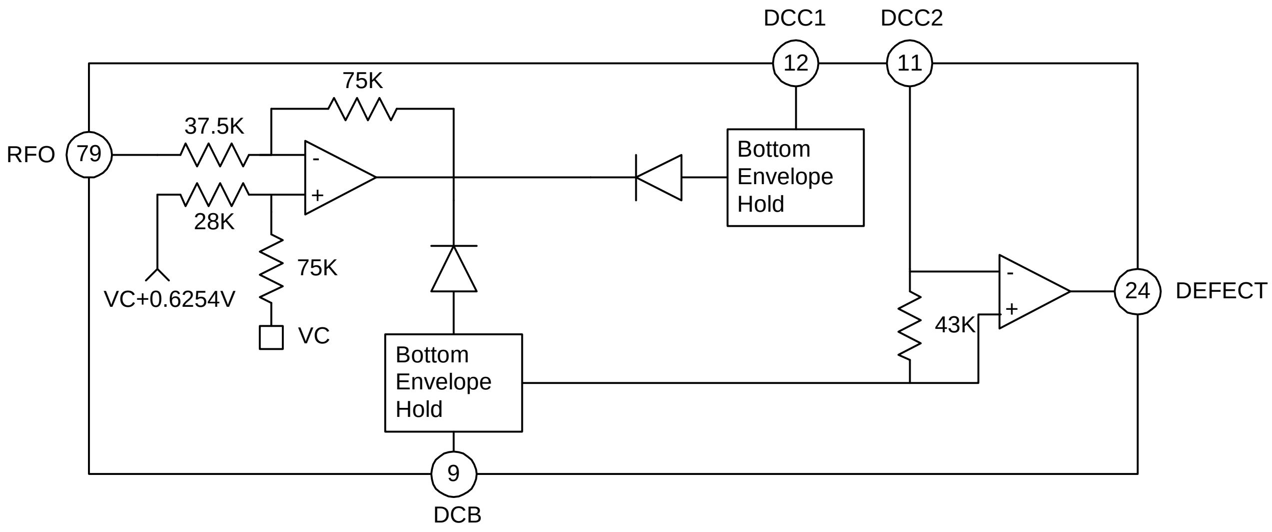
EFM COMPARATOR

The EFM comparator makes the RF signal into a secondary signal. The asymmetry generated by a fault during DISC production cannot be eliminated by only AC coupling, so control the standard voltage of the EFM comparator to eliminate it.



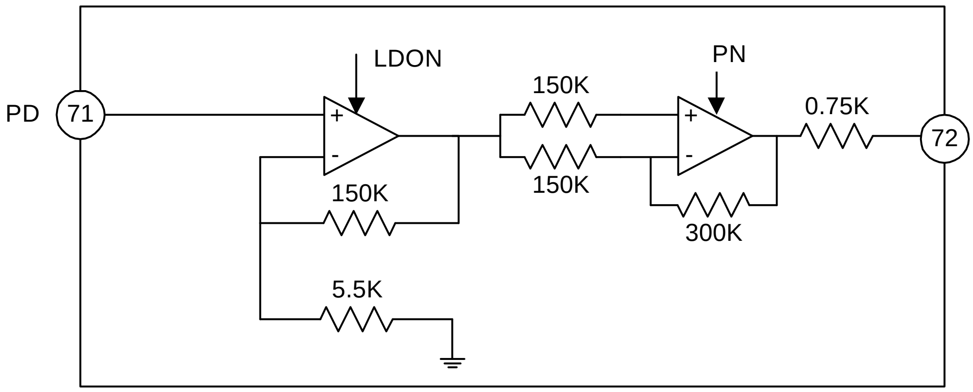
DEFECT CIRCUIT

After RFO signal inversion, bottom hold is carried out using only 2. Except, the bottom hold of holds the coupling level just before the coupling. Differentiate this with the coupling, then level shift it. Compare the signals to either direction to generate the defect detect signal.



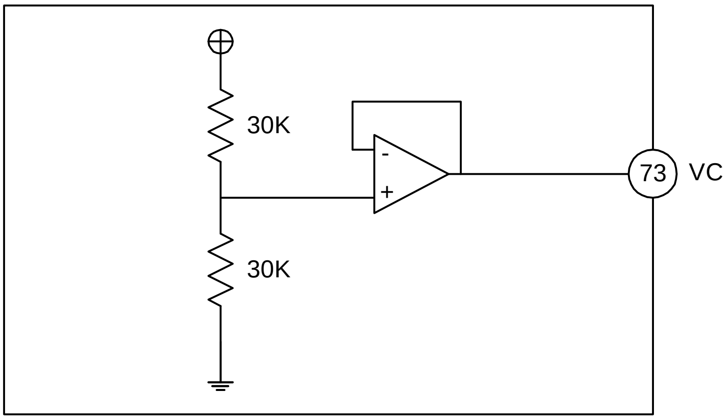
APC CIRCUIT

If you operate the laser diode in constant current, since it has a negative temperature characteristic with a large, it is controlled by the monitor photo diode so that the output is kept regular.



CENTER VOLTAGE GENERATION CIRCUIT

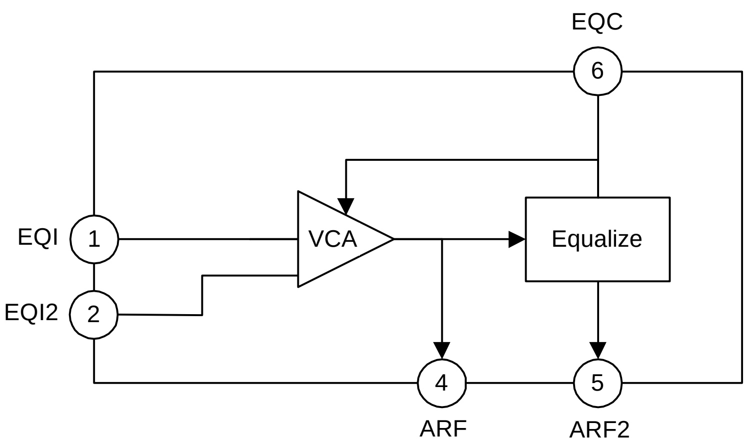
This circuit makes the center voltage using the resistance divide.



RF EQUALIZE CIRCUIT

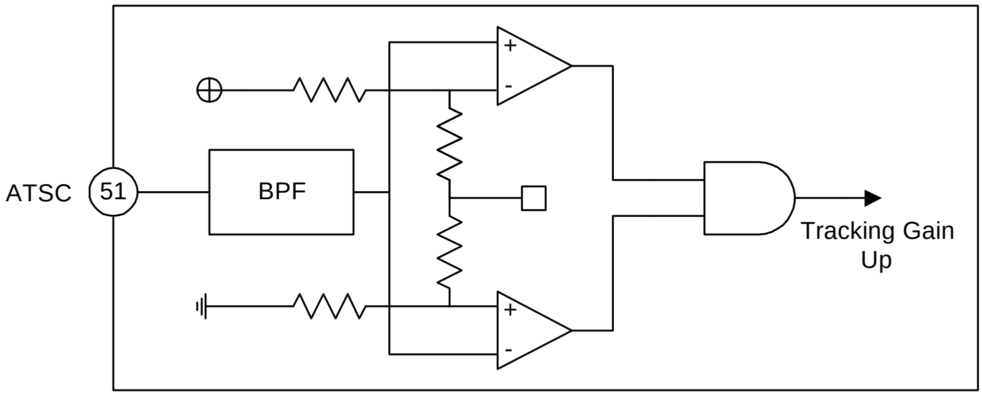
The AGC block maintains a steady RF peak to peak level, and has a built-in 3T gain boost function. It detects the RF envelope and compares it with the standard voltage to perform comparison gain adjustment.

The received RF output stabilizes the RF level to 1Vpp, and this output is applied as the EFM slice input. EQ12 (input) and ARF (output) on/off is to select by defect duty check of internal C1flag signal.



ATSC

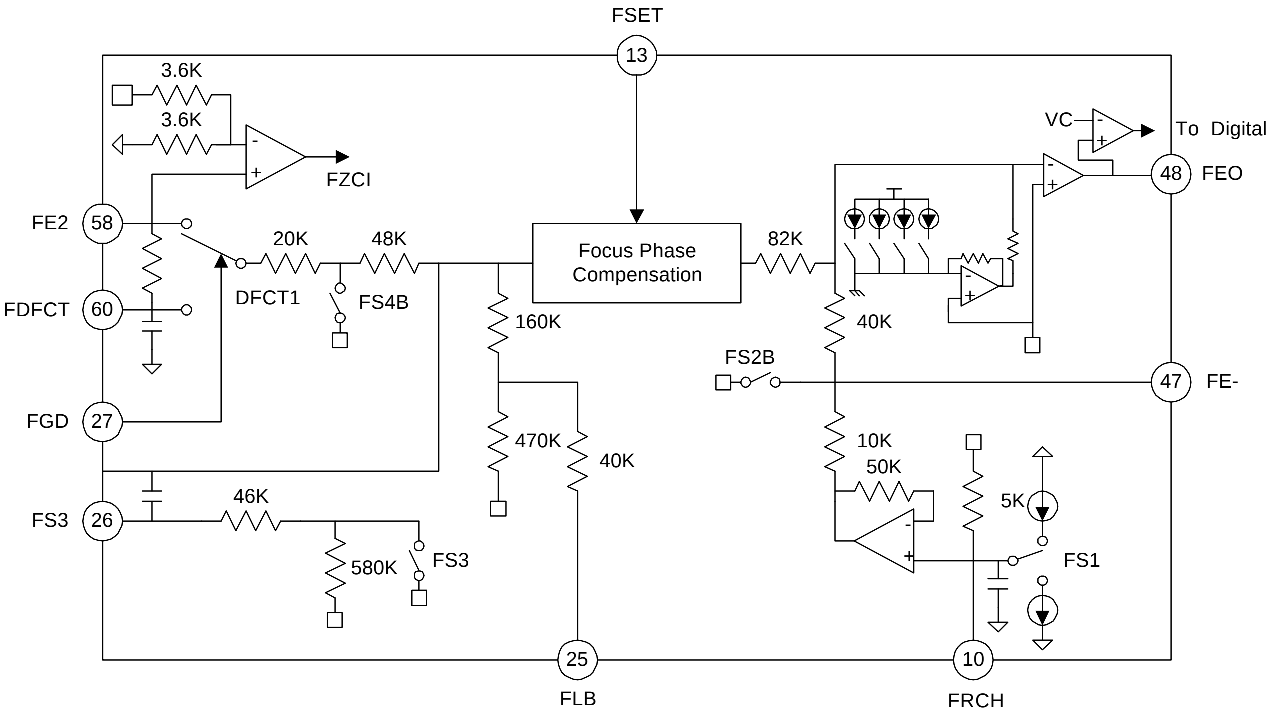
The detect circuit for the tracking gain up (about shock) is composed of a window and a comparator.



FOCUS SERVO

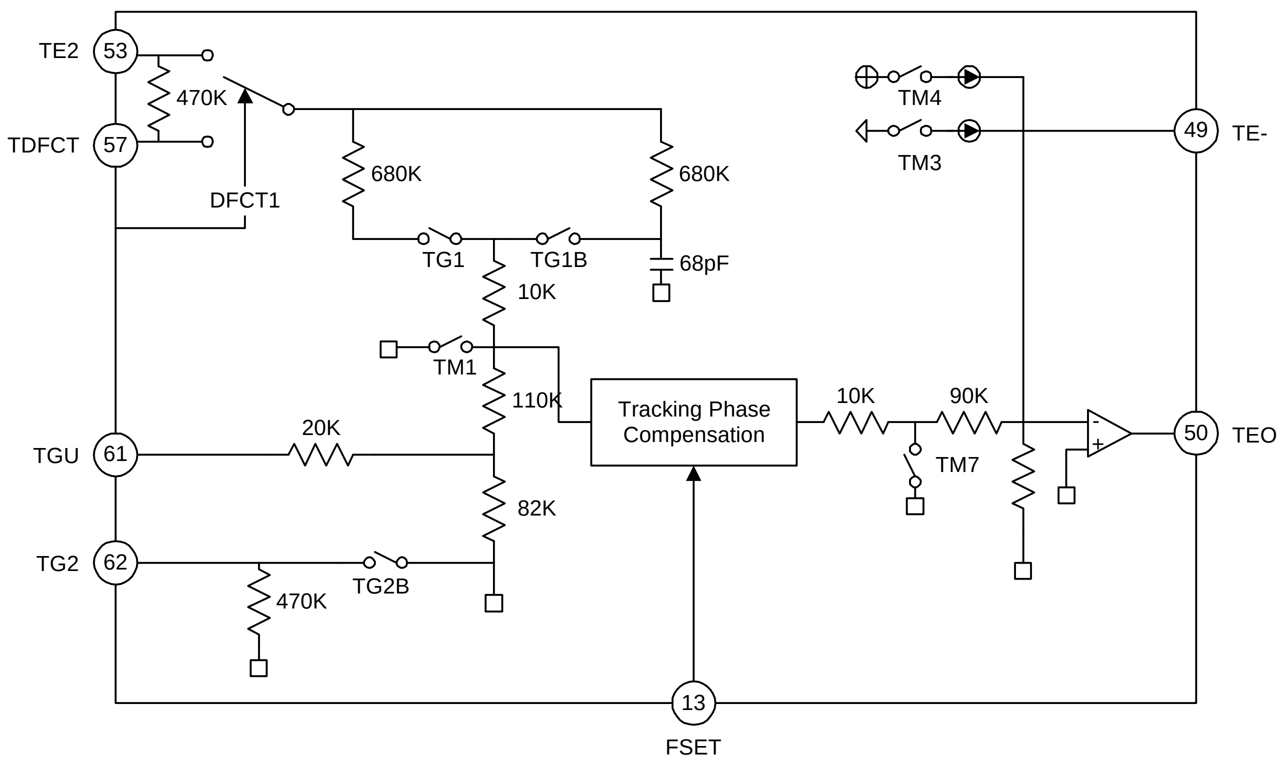
If set to phase compensate the focus servo loop, the focus servo loop is muted when defect is H. At this time, the focus error signal is integrated by the 0.1uF capacitor to be connected to the FDFCT block, and the 470K OHM resistance. It is then output through the servo loop. Therefore, during defect, the focus error output is held as the error value before the defect error. The frequency which maximizes the focus loops phase compensation is changed by the FSET block. If the resistance is 510 KOHM, the maximum frequency is 1.2kHz, and is inversely proportional to the resistance.

When in focus search, FS4 is on to intercept the error signal. The focus search signal is output through the FEO block. When focus is on, FS2 is on, and the focus error signal input through the FE2 block is output to the output pin through the loop.



TRACKING SERVO

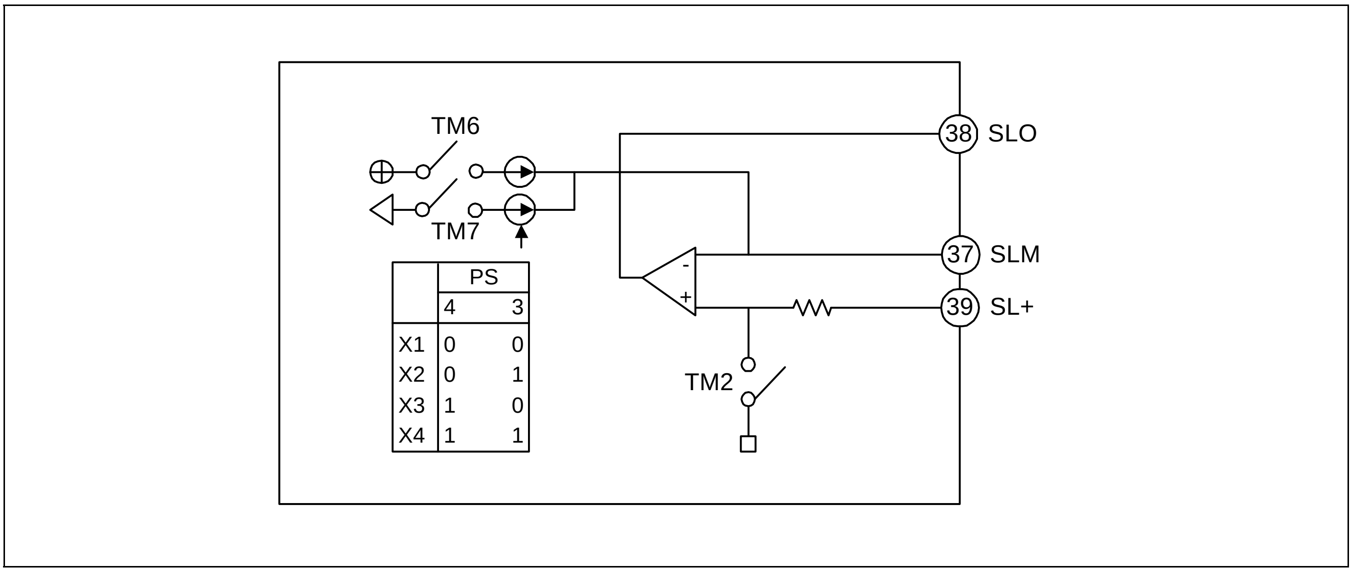
After tracking servo loops phase compensation and during defect, the tracking error signal is integrated through 470K resistance and the 0.1uF capacitor, then output through the servo loop. RTG and TG2 blocks are tracking gain up/down exchange blocks. In phase compensation, like focus loop, the peak frequency of the phase compensation is varied by the Fset block. If the resistance connected to the FSET block changes, the OP AMP dynamic range and the offset change as well.



The TM7 switch is a brake switch which turns the tracking loop on/off when the actuator is unstable after a jump. After the servo has jumped 10 tracks the servo circuit is out of the liner range, and sometimes the Actuator follows an unstable track. So this prevents unnecessary jumping caused by unwanted tracking errors. TG2 and TGU blocks adjust the tracking servo loops high frequency gain. It adjusts the gain of the wanted frequency band zone through the external cap.

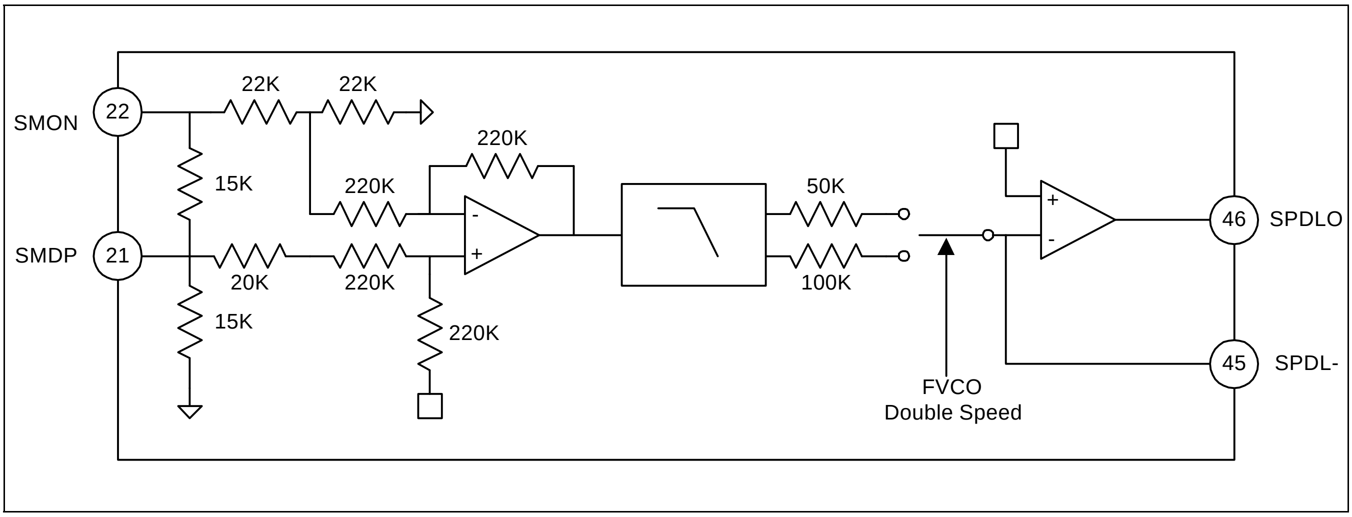
SLED SERVO

This servo integrates the tracking servo output to move the pick-up. Also, during Track movement, it outputs sled Kick voltage for the track jump along the sled axis.



SPINDLE SERVO & LOW PASS FILTER

200Hz LPF is configured by the 20K resistance and 0.33uF cap in order to eliminate carrier components. FSW becomes low in CLV-S mode, so more powerful filter movements are carried out.



ITEM1. Mirror Mute (Used for Tracking Mute Only)

This circuit is used as an ABEX-725A countermeasure, which handles tracking muting when mirror is detected. Its min and max are set, and it detects a minimum of 11kHz to a maximum of 700Hz.

Except, mute does not function in the following four cases.

- When transmitting a MICOM tracking gain up command (TG1, TG2 = 1)
- When Anti-shock is detected (ATSC)
- When lock falls to L
- When defect is detected

Mirror Mute Operating/APC P-SUB	APC On	APC Off
Interruption on (Mirror 11kHz - 0.7 kHz)	$854	$85C
Interruption off	$856	$85E
Interruption on (Mirror 2.75kHz - 0.7kHz)	$857	$85F
Interruption on (Mirror 5.5kHz - 0.7kHz)	$855	$85D

ITEM2, TRCNT Output

TRCNT is an output generated by mirror and TZC. Mirror is a track movement detect output by the main beam, and TZC is a track movement detect output by side beam. TRCNT receives these 2 inputs and determines if the pick-up is currently moving inwards or outwards to use it when in tracking brake of $17.