

July 1987

Features

- This Circuit Is Processed In Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Access Time (Max. Over Temp.).....225ns
- Low Leakage (Max. Over Temp.)..... $I_{D(OFF)}$ 50nA
- Low Charge Transfer Error (100pF Load).....25mV
- Single Ended to Differential Selectable (SDS)
- TTL/CMOS Compatible

Applications

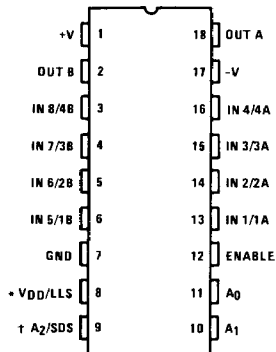
- Data Acquisition Systems
- Telemetry
- Industrial Control

Description

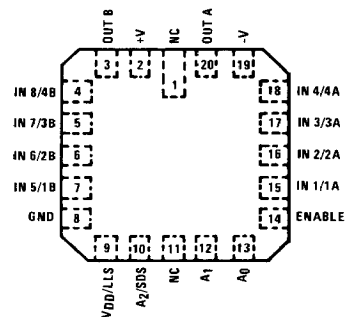
The HI-518/883 is a monolithic dielectrically isolated, high speed, high performance CMOS analog multiplexer. It offers unique built-in channel selection decoding plus an inhibit input for disabling all channels. The dual function of address input A_2 enables the HI-518/883 to be user programmed either as a single ended 8-channel multiplexer by connecting 'OUT A' to 'OUT B' and using A_2 as a digital address input, or as a 4-channel differential multiplexer by connecting A_2 to the $-V_{SUPPLY}$. The substrate leakages and parasitic capacitances are reduced substantially by using the Harris dielectric isolation process to achieve optimum performance in both high and low level signal applications. The low output leakage current ($I_{D(OFF)} < 50nA$ over temperature) of the device makes it an ideal choice for high speed data acquisition systems, precision instrumentation, and industrial process control.

Pinouts

HI1-518/883 (CERAMIC DIP)
TOP VIEW



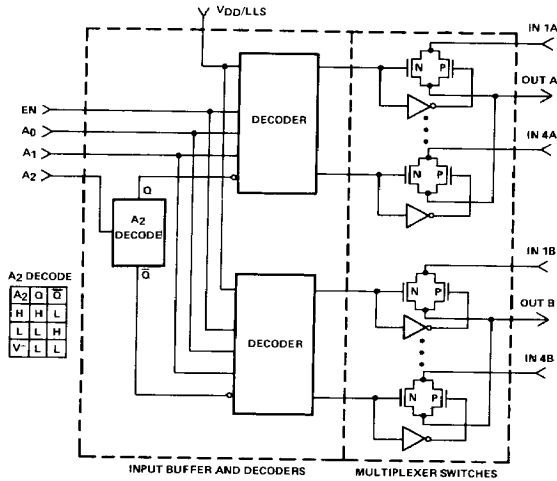
HI4-518/883 (CERAMIC LCC)
TOP VIEW



* LLS = Logic Level Select (TTL Compatible with V_{DD}/LLS Pin = Ground or Open, CMOS Compatible when V_{DD}/LLS Pin = V_{DD})

† SDS = Single Ended/Differential Select (Multiplexer is in Differential Mode when A_2/SDS Pin = $-V_{SUPPLY}$)

Functional Diagram



Truth Tables

HI-518/883 USED AS 8 CHANNEL MULTIPLEXER

USE A ₂ /SDS AS DIGITAL ADDRESS INPUT				ON CHANNEL TO	
ENABLE	A ₂	A ₁	A ₀	OUT A	OUT B
L	X	X	X	None	None
H	L	L	L	1A	None
H	L	L	H	2A	None
H	L	H	L	3A	None
H	L	H	H	4A	None
H	H	L	L	None	1B
H	H	L	H	None	2B
H	H	H	L	None	3B
H	H	H	H	None	4B

HI-518/883 USED AS DIFFERENTIAL 4 CHANNEL MULTIPLEXER

A ₂ /SDS CONNECTED TO -V _{SUPPLY}			ON CHANNEL TO	
ENABLE	A ₁	A ₀	OUT A	OUT B
L	X	X	None	None
H	L	L	1A	1B
H	L	H	2A	2B
H	H	L	3A	3B
H	H	H	4A	4B

Specifications HI-518/883

Absolute Maximum Ratings

Voltage Between Supply Pins.....	33V	Lead Temperature (Soldering 10 Seconds).....	275°C
+VSUPPLY to Ground.....	16.5V	Junction Temperature.....	+175°C
-VSUPPLY to Ground.....	16.5V	Thermal Resistance, Junction-to-Case (θ_{jc})	
+VS.....	+VSUPPLY +2V	Ceramic DIP Package.....	25°C/W
-VS.....	-VSUPPLY -2V	Ceramic LCC Package.....	21°C/W
Digital Input Voltage		Thermal Resistance, Junction-to-Ambient (θ_{ja})	
TTL Levels Selected (V_{DD}/LLS Pin = GND or Open)		Ceramic DIP Package.....	84°C/W
+VA.....	+6V	Ceramic LCC Package.....	78°C/W
-VA.....	-6V	Power Dissipation (at 75°C)	
A ₂ /SDS.....	-VSUPPLY -2V	Ceramic DIP Package.....	1.19W
A ₂ /SDS.....	+VSUPPLY +2V	Ceramic LCC Package.....	1.28W
CMOS Levels Selected (V_{DD}/LLS Pin = V_{DD})		Power Dissipation Derating Factor (Above +75°C)	
+VA.....	+VSUPPLY +2V	Ceramic DIP Package.....	11.9mW/°C
-VA.....	-2V	Ceramic LCC Package.....	12.8mW/°C
Storage Temperature Range.....	-65°C to +150°C	ESD Classification.....	≤2000V

Recommended Operating Conditions

Operating Temperature Range.....	-55°C to +125°C	Logic Level Low (V_{AL}).....	0V to 0.8V
Operating Supply Voltage ($\pm V_{SUPPLY}$).....	±15V	Logic Level High (V_{AH}).....	2.4V to +VSUPPLY
Analog Input Voltage (V_S).....	±14V	Max RMS Current, S or D.....	8mA

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested at +VSUPPLY = +15V, -VSUPPLY = -15V, VEN = 2.4V, VDD/LLS = GND, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Leakage Current	I _{IH}	Measure Inputs Sequentially. Connect All Unused Inputs to GND	1, 2, 3	+25°C, +125°C -55°C	-1.0	1.0	μA
	I _{IL}	Measure Inputs Sequentially. Connect All Unused Inputs to +5V	1, 2, 3	+25°C, +125°C -55°C	-20	20	μA
Leakage Current Into the Source Terminal of an "OFF" Switch	+I _{S(OFF)}	V _S = 10V, V _D = -10V, V _{EN} = 0.8V All Unused Inputs = -10V	1, 2, 3	+25°C, +125°C, -55°C	-50	+50	nA
	-I _{S(OFF)}	V _S = -10V, V _D = 10V, V _{EN} = 0.8V All Unused Inputs = +10V	1, 2, 3	+25°C, +125°C, -55°C	-50	+50	nA
Leakage Current Into the Drain Terminal of an "OFF" Switch	+I _{D(OFF)}	V _S = -10V, V _D = +10V, V _{EN} = 0.8V All Unused Inputs = -10V	1, 2, 3	+25°C, +125°C, -55°C	-50	+50	nA
	-I _{D(OFF)}	V _S = +10V, V _D = -10V, V _{EN} = 0.8V All Unused Inputs = +10V	1, 2, 3	+25°C, +125°C, -55°C	-50	+50	nA
Leakage Current From an "ON" Driver Into the Switch (Drain)	+I _{D(ON)}	V _S = V _D = 10V All Unused Inputs = -10V	1, 2, 3	+25°C, +125°C, -55°C	-50	+50	nA
	-I _{D(ON)}	V _S = V _D = -10V All Unused Inputs = +10V	1, 2, 3	+25°C, +125°C, -55°C	-50	+50	nA
Positive Supply Current	I(+)	V _S = 0V, V _D = Open, V _{EN} = 2.4V Sequence All Address Combinations, Record Highest I+	1, 2, 3	+25°C, +125°C, -55°C	—	+15	mA
Negative Supply Current	I(-)	V _S = 0V, V _D = Open, V _{EN} = 2.4V Sequence All Address Combinations, Record Highest I-	1, 2, 3	+25°C, +125°C, -55°C	—	+15	mA
Standby Positive Supply Current	+I _{SBY}	V _A = 0.8V, V _{EN} = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-15	—	mA
Standby Negative Supply Current	-I _{SBY}	V _A = 0.8V, V _{EN} = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-15	—	mA
Switch "ON" Resistance	+R _{DS1}	V _S = 10V I _D = 100μA	1 2, 3	+25°C +125°C, -55°C	—	750	Ω
	-R _{DS1}	V _S = -10V I _D = -100μA	1 2, 3	+25°C +125°C, -55°C	—	1000	Ω
Logic Level Voltage	V _{AL} (TTL)	V _{DD} /LLS = GND	1, 2, 3	+25°C, +125°C, -55°C	—	0.8	V
	V _{AH} (TTL)	V _{DD} /LLS = GND	1, 2, 3	+25°C, +125°C -55°C	2.4	—	V
	V _{AL} (CMOS)	V _{DD} /LLS = +15V	1, 2, 3	+25°C, +125°C -55°C	—	4.5	V
	V _{AH} (CMOS)	V _{DD} /LLS = +15V	1, 2, 3	+25°C, +125°C, -55°C	10.5	—	V

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested at +VSUPPLY = +15V, -VSUPPLY = -15V, VEN = 2.4V, VDD/LLS = GND, Unless Otherwise Specified.

A.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMP	LIMITS		UNITS
					MIN	MAX	
Break-Before-Make Time Delay	t _D	R _L = 800Ω, C _L = 12.5pF	9	+25°C	10	—	ns
			10	+125°C	2	—	ns
Propagation Delay Times: Address Inputs to I/O Channel Times	t _A	R _L = 10MΩ, C _L = 12.5pF	9	+25°C	—	175	ns
			10, 11	+125°C, -55°C	—	225	ns
Enable to I/O	t _{ON(EN)}	R _L = 800Ω, C _L = 12.5pF	9	+25°C	—	175	ns
			10, 11	+125°C, -55°C	—	225	ns
	t _{OFF(EN)}	R _L = 800Ω, C _L = 12.5pF	9	+25°C	—	175	ns
			10, 11	+125°C, -55°C	—	225	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Characterized at +VSUPPLY = +15V, -VSUPPLY = -15V, VEN = 2.4V, VDD/LLS = GND, Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMP	LIMITS		UNITS
					MIN	MAX	
Capacitance: Address Input	C _A	V ₊ = V ₋ = 0V f = 1MHz	1	+25°C	—	5.0	pF
Capacitance: Output Switch	C _{OS}	V ₊ = V ₋ = 0V f = 1MHz	1	+25°C	—	10	pF
Capacitance: Input Switch	C _{IS}	V ₊ = V ₋ = 0V f = 1MHz	1	+25°C	—	5.0	pF
Charge Transfer Error	V _{CTE}	V _S = GND, C _L = 100pF V _{GEN} = 0V to 5V	1	+25°C	—	25	mV
Off Channel Isolation	V _{ISO}	V _{EN} = 0.8V, R _L = 1kΩ C _L = 40pF, V _S = 3VRMS f = 500kHz	1	+25°C	-45	—	dB
Break-Before-Make Time Delay	t _D	R _L = 800Ω, C _L = 12.5pF	1	-55°C	2	—	ns

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1, 2 & 3)
Interim Electrical Parameters (Pre-Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

*PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

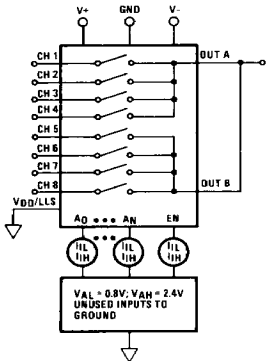
NOTE 1. The parameters listed in this table are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

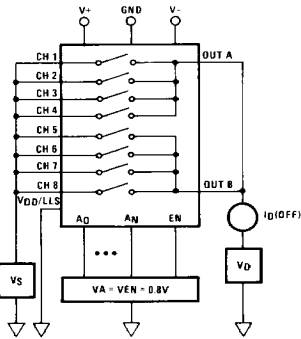
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Test Circuits

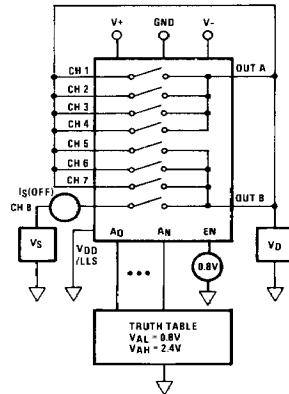
INPUT LEAKAGE CURRENT



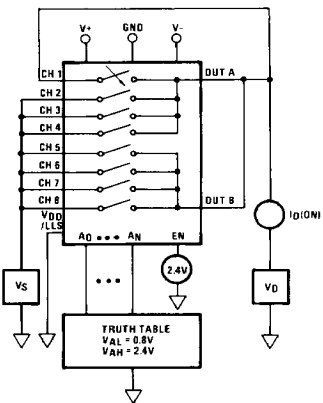
ID(OFF)



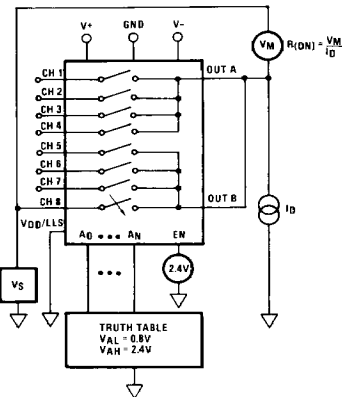
IS(OFF)



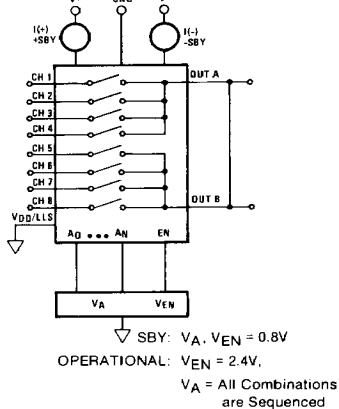
ID(ON)



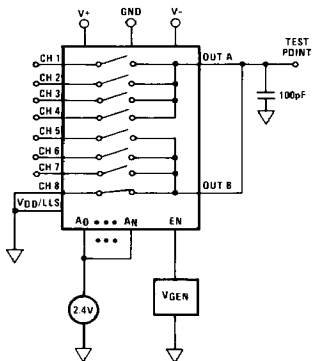
RDS



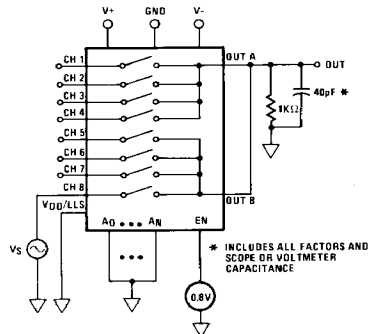
SUPPLY CURRENTS



CHARGE TRANSFER ERROR

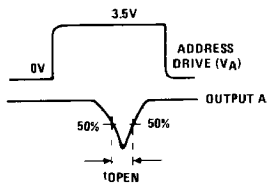


OFF CHANNEL ISOLATION

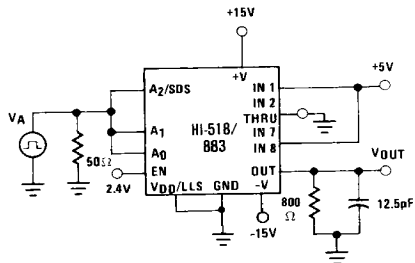


Switching Waveforms

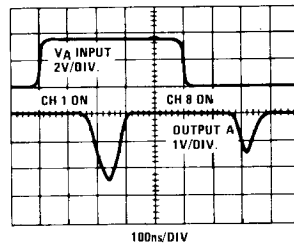
ADDRESS DRIVE



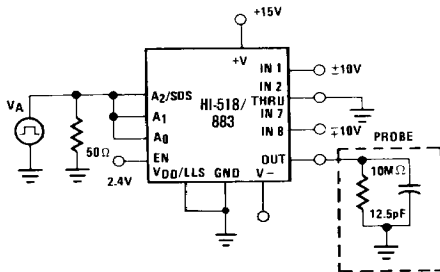
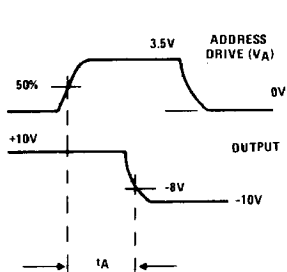
BREAK-BEFORE-MAKE DELAY (t_{OPEN})



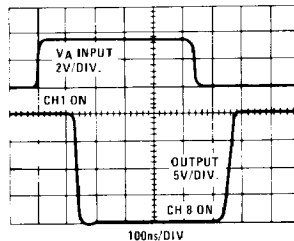
BREAK-BEFORE-MAKE DELAY (t_{OPEN})



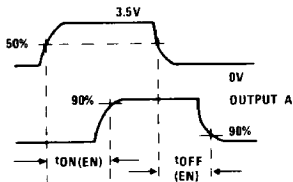
ACCESS TIME



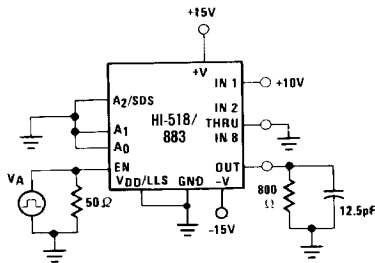
ACCESS TIME



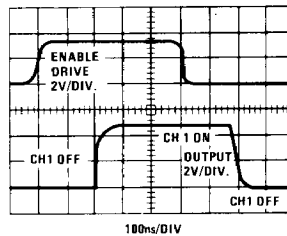
ENABLE DRIVE



ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$



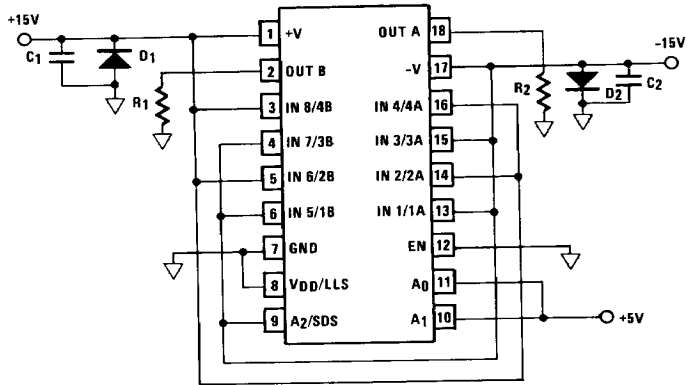
ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$



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Burn-In Circuits

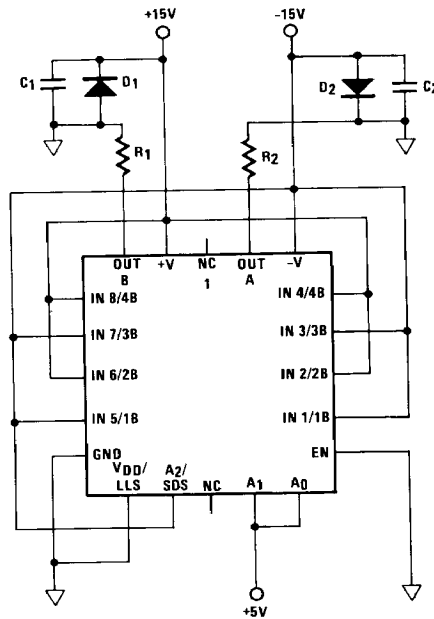
HI-518/883 CERAMIC DIP



NOTES:

- R₁ = R₂ = 10kΩ, ±5%, 1/4 or 1/2W
- C₁ = C₂ = 0.01μF (one per socket) or 0.1μF (one per row)
- D₁ = D₂ = IN4002 or equivalent (per board)

HI-518/883 CERAMIC LCC

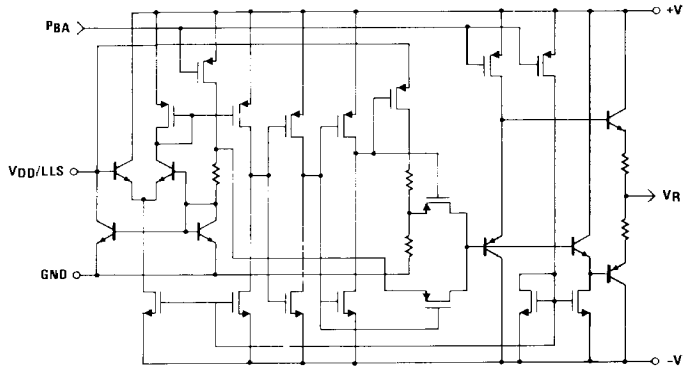


NOTES:

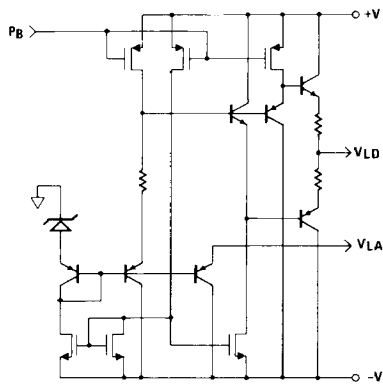
- R₁ = R₂ = 10kΩ, ±5%, 1/2 or 1/4W (per socket)
- C₁ = C₂ = 0.01μF (one per socket) or 0.1μF (one per row)
- D₁ = D₂ = IN4002 or equivalent (per board)

Schematic Diagrams (Continued)

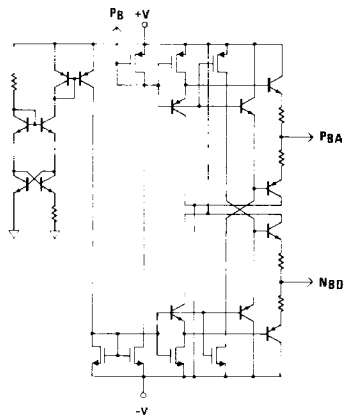
LOGIC LEVEL SELECT CIRCUIT



REFERENCE VOLTAGES



BIAS



Die Characteristics

DIE DIMENSIONS: 89 x 93 x 19 mils

METALLIZATION:

Type: Al

Thickness: $18\text{k}\text{\AA} \pm 2\text{k}\text{\AA}$

GLASSIVATION:

Type: Nitride

Thickness: $7\text{k}\text{\AA} \pm 1.0\text{k}\text{\AA}$

WORST CASE CURRENT DENSITY: $2 \times 10^5\text{A}/\text{cm}^2$

TRANSISTOR COUNT:

HI-518/883 356

PROCESS: CMOS DI

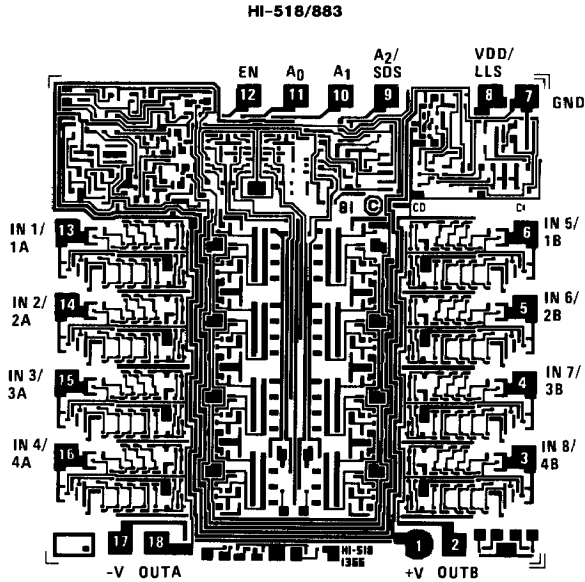
DIE ATTACH:

Material: Gold/Silicon Eutectic Alloy

Temperature: Ceramic DIP - 460° (Max)

Ceramic LCC - 420° (Max)

Metallization Mask Layout



NOTE: Pad Numbers Correspond to DIP Pin Numbers Only.

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