IP5311CX5

Dual-channel integrated passive filter network with ESD protection to IEC 61000-4-2 level 4

Rev. 01 — 30 November 2009 Product data sheet

1. Product profile

1.1 General description

IP5311CX5 is a dual-channel RC low-pass filter array which is designed to provide filtering of undesired RF signals in the 10 MHz to 6000 MHz frequency band. In addition, IP5311CX5 incorporates diodes to provide protection to downstream components from ElectroStatic Discharge (ESD) voltages as high as ±15 kV contact according the IEC 61000-4-2 model, far exceeding standard level 4.

The device is optimized for loudspeaker applications using speakers of 10 Ω to 32+ Ω impedance.

IP5311CX5 is fabricated using monolithic silicon technology and integrates several resistors, bidirectional diodes and two high density capacitors in a single Wafer-Level Chip-Scale Package (WLCSP). These features make the IP5311CX5 ideal for use in applications requiring the utmost in miniaturization such as mobile phone handsets, cordless telephones and personal digital devices.

1.2 Features

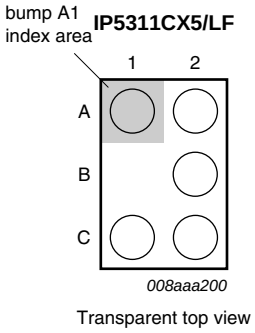
- Pb-free, RoHS compliant and free of halogen and antimony (Dark Green compliant)
- Dual-channel integrated RC filter network with high density capacitors (2 × 5 nF)
- Integrated ESD protection withstanding ±15 kV contact discharge, far exceeding IEC 61000-4-2 level 4
- WLCSP with 0.4 mm pitch

1.3 Applications

- Cellular and Personal Communication System (PCS) mobile handsets
- Cordless telephones
- Wireless data (WAN/LAN) systems

2. Pinning information

2.1 Pinning



Transparent top view

Fig 1. Pin configuration IP5311CX5/LF

2.2 Pin description

Table 1. Pinning

	Description
A1	filter channel 1 internal 2 kV amplifier connection
A2	filter channel 1 external 15 kV speaker connection
C1	filter channel 2 internal 2 kV amplifier connection
C2	filter channel 2 external 15 kV speaker connection
B1	not connected (missing ball)
B2	ground

3. Ordering information

Table 2. Ordering information

	Package		
	Name	Description	Version
IP5311CX5/LF	WLCSP5	wafer level chip-size package; 5 bumps; 1.16 × 0.8 × 0.61 mm	IP5311CX5/LF
IP5311CX5/LF/P	WLCSP5	wafer level chip-size package; 5 bumps; 1.16 × 0.8 × 0.61 mm	IP5311CX5/LF/P

4. Functional diagram

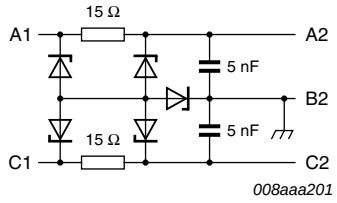


Fig 2. Schematic diagram IP5311CX5

5. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Max	Unit
V_I	input voltage		–0.5	+4.5	V
V_{ESD}	electrostatic discharge voltage	pins A2 and C2 to ground			
		contact discharge [1]	–15	+15	kV
		air discharge [1]	–15	+15	kV
		IEC 61000-4-2 level 4; pins A2 and C2 to ground			
		contact discharge	–8	+8	kV
		air discharge	–15	+15	kV
		IEC 61000-4-2 level 1; pins A1 and C1 to ground			
		contact discharge	–2	+2	kV
		air discharge	–2	+2	kV
I_{ch}	channel current (DC)		-	92	mA
P_{ch}	channel power dissipation	continuous power	-	100	mW
P_{tot}	total power dissipation	continuous power	-	200	mW
T_{stg}	storage temperature		–55	+150	°C
$T_{reflow(peak)}$	peak reflow temperature	10 s maximum	-	260	°C
T_{amb}	ambient temperature		–35	+85	°C

[1] Device is qualified with 1000 pulses of ±15 kV contact discharges each, according to the IEC61000-4-2 model and far exceeds the specified level 4 (8 kV contact discharge).

6. Characteristics

Table 4. Channel characteristics

T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Typ	Max	Unit
$R_{s(ch)}$	channel series resistance		13.5	15	16.5	Ω
C_1	capacitance 1	high density; $V_{bias(DC)}$ = 0 V; f = 100 kHz	4	5	6	nF
C_2	capacitance 2		4	5	6	nF
C_d	diode capacitance	$V_{bias(DC)}$ = 0 V; f = 100 kHz	[1] -	14	-	pF
V_{BR}	breakdown voltage	positive direction; I_{test} = 1 mA	14	16.5	-	V
		negative direction; I_{test} = −1 mA	-	−16.5	−14	V
I_{LR}	reverse leakage current	per channel; V_I = 3.0 V	-	-	60	nA
		per channel; V_I = −3.0 V	−60	-	-	nA

[1] Guaranteed by design.

7. Application information

7.1 Insertion loss

The insertion loss measurement configuration of a typical 50 Ω NetWork Analyzer (NWA) system for evaluation of the IP5311CX5 is shown in Figure 3.

The insertion loss of both channels at frequencies up to 6 GHz is displayed in Figure 4.

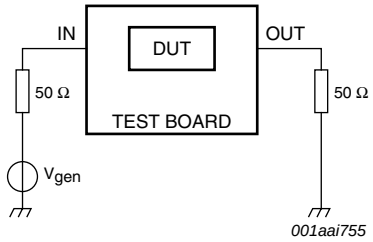
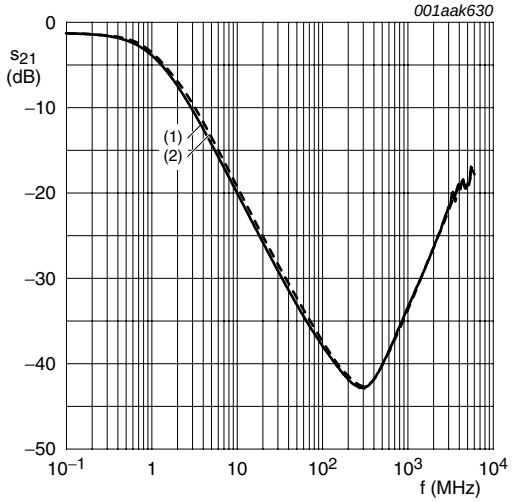


Fig 3. Frequency response measurement configuration



(1) Channel 1 (pins A1 and A2).

(2) Channel 2 (pins C1 and C2).

Fig 4. Measured insertion loss magnitudes

7.2 Crosstalk

The crosstalk measurement configuration of a typical 50 Ω NWA system for evaluation of the IP5311CX5 is shown in Figure 5.

The measured crosstalk within the IP5311CX5 in a 50 Ω NWA system from one channel to the other channel is shown in Figure 6. In all cases, unused connections are terminated with 50 Ω to ground.

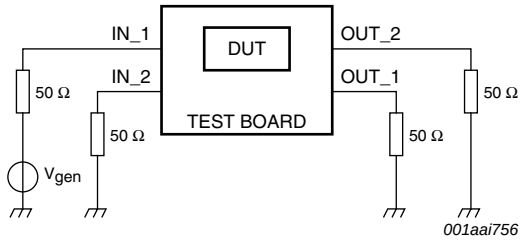
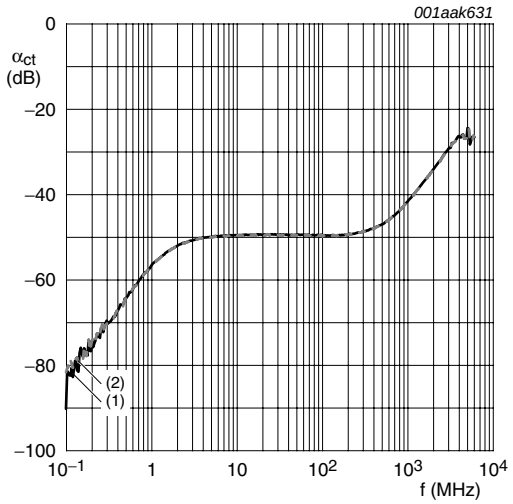


Fig 5. Crosstalk measurement configuration



(1) Channel 1 to channel 2 (pins A1 and C2).

(2) Channel 2 to channel 1 (pins A2 and C1).

Fig 6. Measured crosstalk between adjacent channels

7.3 Voltage dependency of high density capacitors

The high density capacitors integrated in IP5311CX5 show a voltage dependency similar to some higher value discrete ceramic capacitors.

When used in an average mobile application, the typical voltage swing across the capacitance will be in the range of −0.5 V to +4 V. In this event, the capacitor values change proportional to the bias voltage as depicted in Figure 7.

The measurement is performed several times, starting at the 'starting point' at 0 V, increasing to 4 V (arrow 1), decreasing to −0.5 V (following arrow 2) and back to +4 V (arrow 3).

When measuring the capacitance over voltage for voltage swings of e.g. −20 V to +20 V, a hysteresis in the capacitance over $V_{bias(DC)}$ can be observed (see Figure 8), which is inherent to the integration process for the high density capacitors in this product.

Again, the measurement starts at 'starting point', following arrow 1 up to $V_{bias(DC)}$ = 20 V, from there along arrow 2 down to $V_{bias(DC)}$ = −20 V and back via arrow 3 and arrow 4.

Values of C_1 and C_2 specified in Table 4 are based on measurements at the starting point.

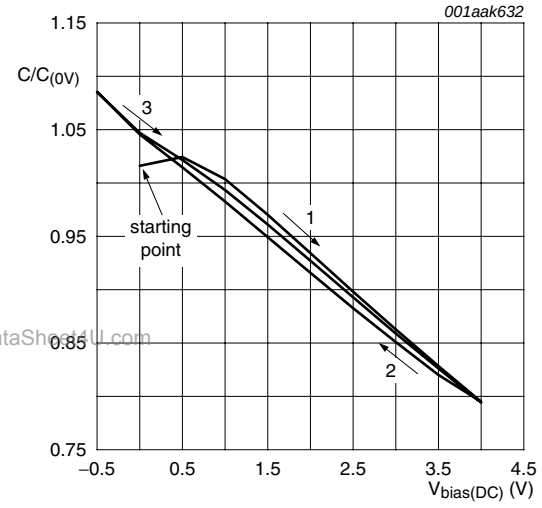


Fig 7. Relative capacitance $C/C_{(0V)}$ of high density capacitors for $-0.5\ V \leq V_{bias(DC)} \leq +4\ V$

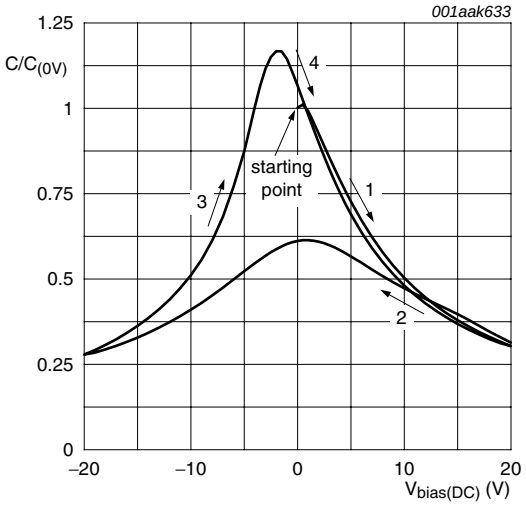
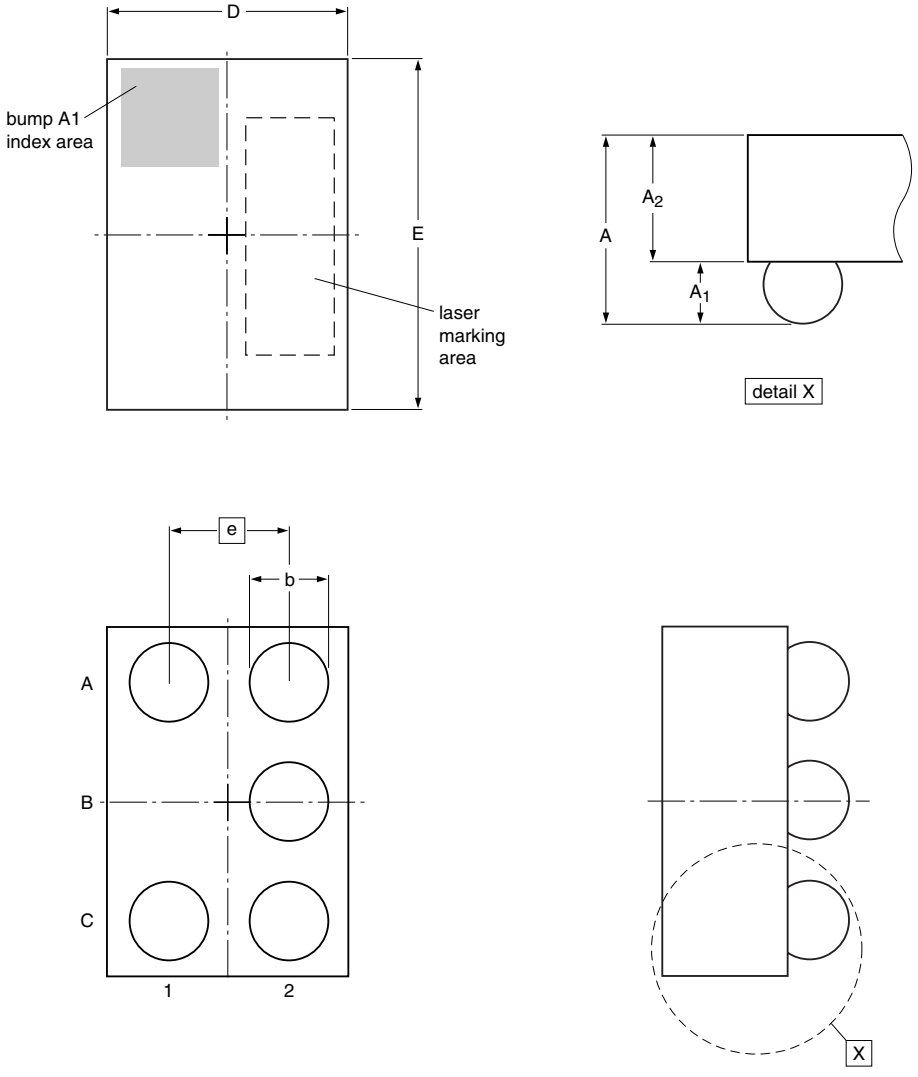


Fig 8. Relative capacitance $C/C_{(0V)}$ of high density capacitors for $-20\ V \leq V_{bias(DC)} \leq +20\ V$

8. Package outline

WLCSP5: wafer level chip-size package; 5 bumps; 1.16 x 0.8 x 0.61 mm **IP5311CX5/LF**



Dimensions

Unit		A	A_1	A_2	b	D	E	e
mm	max	0.66	0.22	0.44	0.31	0.85	1.21	
	nom	0.61	0.20	0.41	0.26	0.80	1.16	0.40
	min	0.56	0.18	0.38	0.21	0.75	1.11	

ip5311cx5_lf_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
IP5311CX5/LF						~~09-09-03~~ 09-10-30

Fig 9. Package outline IP5311CX5/LF (WLCSP5)

9. Soldering of WLCSP packages

9.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note *AN10439 "Wafer Level Chip Scale Package"* and in application note *AN10365 "Surface mount reflow soldering description"*.

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

9.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

9.3 Reflow soldering

Key characteristics in reflow soldering are:

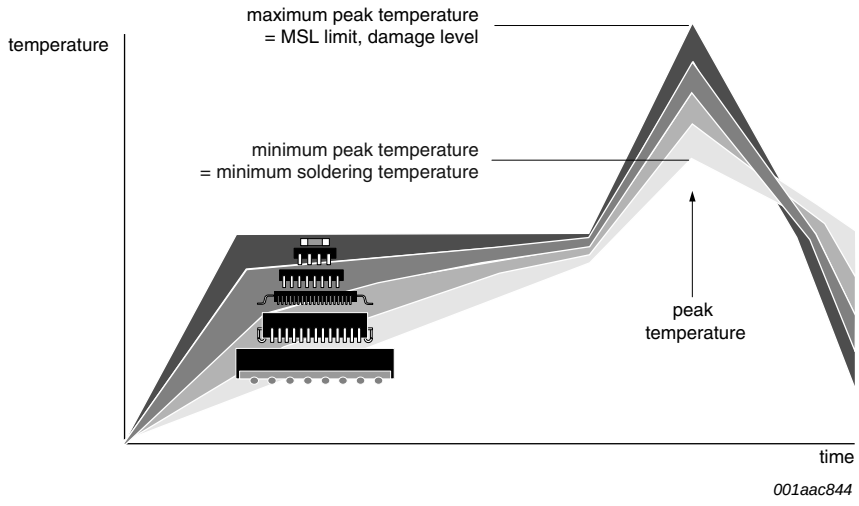
- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 10) than a PbSn process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 5.

Table 5. Lead-free process (from J-STD-020C)

	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 10.



MSL: Moisture Sensitivity Level

Fig 10. Temperature profiles for large and small components

For further information on temperature profiles, refer to application note *AN10365 "Surface mount reflow soldering description"*.

9.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

9.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

9.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note *AN10365 "Surface mount reflow soldering description"*.

9.3.4 Cleaning

Cleaning can be done after reflow soldering.

10. Abbreviations

Table 6. Abbreviations

	Description
DUT	Device Under Test
ESD	ElectroStatic Discharge
LAN	Local Area Network
NWA	NetWork Analyzer
PCS	Personal Communication System
RoHS	Restriction of Hazardous Substances
WAN	Wide Area Network
WLCSP	Wafer-Level Chip-Scale Package

11. Revision history

Table 7. Revision history

	Release date	Data sheet status	Change notice	Supersedes
IP5311CX5_1	20091130	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

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