

16-Bit Microcontrollers with Infrared Module and Optional USB

MAXQ612/MAXQ622

General Description

The MAXQ612/MAXQ622 are low-power, 16-bit MAXQ® microcontrollers designed for low-power applications including universal remote controls, consumer electronics, and white goods. Both devices use a low-power, high-throughput, 16-bit RISC microcontroller. Serial peripherals include two universal synchronous/asynchronous receiver-transmitters (USARTs), two SPI™ master/slave communications ports, and an inter-integrated circuit (I²C) bus. The devices also incorporate an IR module with carrier frequency generation and flexible port I/O capable of multiplexed keypad control. The MAXQ622 adds a universal serial bus (USB) with integrated physical interface (PHY).

The MAXQ612/MAXQ622 include 128KB of flash memory and 6KB of data SRAM. Intellectual property (IP) protection is provided by a secure memory management unit (MMU) that supports multiple application privilege levels and protects code against copying and reverse engineering. Privilege levels enable vendors to provide libraries and applications to execute on the MAXQ612/MAXQ622, while limiting access to only data and code allowed by their privilege level.

For the ultimate in low-power battery-operated performance, the devices include an ultra-low-power stop mode (0.3µA typical). In this mode, the minimum amount of circuitry is powered. Wake-up sources include external interrupts, the power-fail interrupt, and a timer interrupt. The microcontroller runs from a wide operating voltage of 1.70V to 3.6V, and can also be powered from the USB.

Applications

Remote Controls	Consumer Electronics
Battery-Powered	Home Appliances
Portable Equipment	White Goods

Features

- ◆ High-Performance, Low-Power, 16-Bit RISC Core
- ◆ DC to 12MHz Operation Across Entire Operating Range

- ◆ 1.70V to 3.6V Operating Voltage
- ◆ Can Be Powered from Battery (V_{DD}) or USB (V_{DDB})
- ◆ 33 Total Instructions for Simplified Programming
- ◆ Three Independent Data Pointers Accelerate Data Movement with Automatic Increment/Decrement
- ◆ Dedicated Pointer for Direct Read from Code Space
- ◆ 16-Bit Instruction Word, 16-Bit Data Bus
- ◆ 16 x 16-Bit General-Purpose Working Registers
- ◆ Secure MMU for Application Partitioning and IP Protection
- ◆ Memory Features
 - 128KB Flash Memory
 - 512-Byte Sectors
 - 20,000 Erase/Write Cycles per Sector
 - 6KB Data SRAM
- ◆ USB Features (MAXQ622 Only)
 - USB 2.0 Full-Speed Compatible
 - Hardware Receive and Transmit Buffers for High Throughput
 - Integrated Full-Speed Transceiver
 - On-Chip Termination and Pullup Resistors
- ◆ Additional Peripherals
 - Power-Fail Warning
 - Power-On Reset (POR)/Brownout Reset
 - Automatic IR Carrier Frequency Generation and Modulation
 - Two 16-Bit Programmable Timers/Counters with Prescaler and Capture/Compare
 - Two SPI Communication Ports
 - Two USART Communication Ports
 - I²C Port
 - Programmable Watchdog Timer
 - 8kHz Nanopower Ring Oscillator Wake-Up Timer
 - Up to 56 General-Purpose I/O
- ◆ Low Power Consumption
 - 0.3µA (typ), 3µA (max) in Stop Mode
 - TA = +25°C, Power-Fail Monitor Disabled
 - 4.8mA (typ) at 12MHz, 520µA (typ) at 1MHz in Active Mode

Ordering Information/Selector Guide

PART	TEMP RANGE	OPERATING VOLTAGE (V)	PROGRAM MEMORY (KB)	DATA MEMORY (KB)	USB FULL SPEED	PIN-PACKAGE
MAXQ612J-0000+	0°C to +70°C	1.7 to 3.6	128 Flash	6	No	44 TQFN-EP*
MAXQ612G-0000+	0°C to +70°C	1.7 to 3.6	128 Flash	6	No	64 LQFP
MAXQ622G-0000+	0°C to +70°C	1.7 to 3.6	128 Flash	6	Yes	64 LQFP

+Denotes a lead(Pb)-free/RoHS-compliant package.

*EP = Exposed pad.

Note: Bare die versions for most of these devices are available. Contact the factory for availability at <https://support.maxim-ic.com/micro>.

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Note: Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, go to: www.maxim-ic.com/errata.



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ABSOLUTE MAXIMUM RATINGS

Voltage Range on VDD with Respect to GND-0.3V to +3.6V
 Voltage Range on Any Lead with
 Respect to GND Except VBUS..... -0.3V to (VDD + 0.5V)
 Voltage Range on VBUS with Respect to GND.....-0.3V to +6.0V
 Continuous Output Current
 Any Single I/O Pin25mA
 All I/O Pins Combined.....25mA

Voltage Range on DP, DM with
 Respect to GND.....-0.3V to (VBUS + 0.3V)
 Operating Temperature Range 0°C to +70°C
 Storage Temperature Range.....-65°C to +150°C
 Soldering Temperature Refer to the IPC/JEDEC
 J-STD-020 Specification.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(VDD = VRST to 3.6V, TA = 0°C to +70°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	VDD		VRST		3.6	V
1.8V Internal Regulator	VREG18		1.62	1.8	1.98	V
Power-Fail Warning Voltage for Supply	VPFW	Monitors VDD (Notes 2, 3, 4)	1.75	1.8	1.85	V
Power-Fail Reset Voltage	VRST	Monitors VDD (Note 5)	1.64	1.67	1.70	V
POR Voltage	VPOR	Monitors VDD	1.0		1.42	V
RAM Data-Retention Voltage	VDRV	(Note 6)	1.0			V
Active Current	IDD_1	Sysclk = 12MHz		4.8	5.5	mA
	IDD_2	Sysclk = 1MHz (Note 6)		0.52	0.8	
Stop-Mode Current	IS1	Power-Fail Off (Note 7)	TA = +25°C	0.3	3	μA
			TA = +70°C	2.8	13	
	IS2	Power-Fail On	TA = +25°C	24	30	
			TA = +70°C	30	40	
Current Consumption During Power Fail	IPFR	(Notes 6, 8, 9)	$\frac{[(3 \times IS_2) + ((PCI - 3) \times (IS_1 + I_{NANO}))]}{PCI}$			μA
Current Consumption During POR	IPOR	(Note 10)		100		nA
Stop-Mode Resume Time	tON			375 + 8192 tHFXIN		μs
Power-Fail Monitor Startup Time	tPFM_ON	(Note 6)			150	μs
Power-Fail Warning Detection Time	tPFW	(Notes 6, 11)	10			μs
Input Low Voltage for IRTX, IRRX, RESET, and All Port Pins	VIL		VGND		0.3 x VDD	V
Input High Voltage for IRTX, IRRX, RESET, and All Port Pins	VIH		0.7 x VDD		VDD	V

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RECOMMENDED OPERATING CONDITIONS (continued)

(V_{DD} = V_{RST} to 3.6V, T_A = 0°C to +70°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Hysteresis (Schmitt)	V _{IHYS}			300		mV
Input Low Voltage for HFXIN	V _{IL_HFXIN}	External driven clock and not feedback connected crystal oscillator	V _{GND}		0.3 x V _{DD}	V
Input High Voltage for HFXIN	V _{IH_HFXIN}	External driven clock and not feedback connected crystal oscillator	0.7 x V _{DD}		V _{DD}	V
IRRX Input Filter Pulse-Width Reject	t _{IRRX_R}				50	ns
IRRX Input Filter Pulse-Width Accept	t _{IRRX_A}		300			ns
Output Low Voltage for IRTX	V _{OL_IRTX}	V _{DD} = 3.6V, I _{OL} = 25mA (Note 6)			1.0	V
		V _{DD} = 2.35V, I _{OL} = 10mA (Note 6)			1.0	
		V _{DD} = 1.85V, I _{OL} = 4.5mA			1.0	
Output Low Voltage for $\overline{\text{RESET}}$ and All Port Pins (Note 12)	V _{OL}	V _{DD} = 3.6V, I _{OL} = 11mA (Note 6)		0.4	0.5	V
		V _{DD} = 2.35V, I _{OL} = 8mA (Note 6)		0.4	0.5	
		V _{DD} = 1.85V, I _{OL} = 4.5mA		0.4	0.5	
Output High Voltage for IRTX and All Port Pins	V _{OH}	I _{OH} = -2mA	V _{DDIO} - 0.5		V _{DDIO}	V
Input/Output Pin Capacitance for All Port Pins Except DP, DM	C _{IO}	(Note 6)			15	pF
Input Leakage Current	I _L	Internal pullup disabled	-100		+100	nA
Input Pullup Resistor for $\overline{\text{RESET}}$, IRTX, IRRX, P0 to P6	R _{PU}	V _{DD} = 3V, V _{OL} = V _{DD} /2 (Note 6)	16	25	39	k Ω
		V _{DD} = 2V, V _{OL} = V _{DD} /2	17	27	41	
		V _{DD} = 3.0V, V _{OL} = 0.4V (Note 6)	16	28	39	
		V _{DD} = 2.0V, V _{OL} = 0.4V (Note 6)	17	30	41	
GPIO Supply Output High Voltage	V _{DDIOH}	V _{DDIOH} current is the sum of V _{DDIO} current and I _{OH} of all GPIO, I _{OH} = 20mA	V _{DD} - 0.4		V _{DD}	V
EXTERNAL CRYSTAL/RESONATOR						
Crystal/Resonator	f _{HFXIN}	(Note 13)	1		12	MHz
Crystal/Resonator Period	t _{HFXIN}			1/f _{HFXIN}		ns
Crystal/Resonator Warmup Time	t _{TAL_RDY}	From initial oscillation		8192 x t _{HFXIN}		ms
Oscillator Feedback Resistor	R _{OSCF}	(Note 6)	0.5	1.0	1.5	M Ω
Crystal ESR		(Note 6)			60	Ω
EXTERNAL CLOCK INPUT						
External Clock Frequency	f _{XCLK}	(Note 13)	DC		12	MHz
External Clock Period	t _{XCLK}			1/f _{XCLK}		ns
External Clock Duty Cycle	t _{XCLK_DUTY}		45		55	%
System Clock Frequency	f _{CK}			f _{HFXIN}		MHz
		HFXOUT = GND		f _{XCLK}		

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RECOMMENDED OPERATING CONDITIONS (continued)

(V_{DD} = V_{RST} to 3.6V, T_A = 0°C to +70°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
System Clock Period	t _{CK}			1/f _{CK}		ns
NANOPOWER RING						
Nanopower Ring Frequency	f _{NANO}	T _A = +25°C	3	13	20	kHz
		T _A = +25°C, V _{DD} = POR voltage (Note 6)	1.7	2.4		
Nanopower Ring Duty Cycle	t _{NANO}	(Note 6)	40		60	%
Nanopower Ring Current	I _{NANO}	Typical at V _{DD} = 1.64V, T _A = +25°C (Note 6)		40	400	nA
WAKE-UP TIMER						
Wake-Up Timer Interval	t _{WAKEUP}		1/f _{NANO}		65,535/f _{NANO}	s
FLASH MEMORY						
System Clock During Flash Programming/Erase	f _{FPSYSCLK}		1			MHz
Flash Erase Time	t _{ME}	Mass erase	20		40	ms
	t _{ERASE}	Page erase	20		40	
Flash Programming Time per Word	t _{PROG}	(Note 14)	20		100	μs
Write/Erase Cycles			20,000			Cycles
Data Retention		T _A = +25°C	100			Years
USB						
USB Supply Voltage	V _{BUS}	(Note 15)	4.5	5.0	5.5	V
V _{BUS} Supply Current (Note 16)	I _{BUS}	Transmitting on DP and DM at 12Mbps, C _L = 50pF on DP and DM to GND, FRCVDD = 0			13.5	mA
		Transmitting on DP and DM at 12Mbps, C _L = 50pF on DP and DM to GND, FRCVDD = 1			3.5	mA
V _{BUS} Supply Current During Idle (Note 16)	I _{BUSID}	DP = high, DM = low, FRCVDD = 0 (Note 6)			6	mA
		DP = high, DM = low, FRCVDD = 1			0.2	mA
V _{BUS} Suspend Supply Current	I _{BUSUS}				500	μA
Single-Ended Input High Voltage DP, DM	V _{IHD}		2.0			V
Single-Ended Input Low Voltage DP, DM	V _{ILD}				0.8	V
Output Low Voltage DP, DM	V _{OLD}	R _L = 1.5kΩ from DP to 3.6V			0.3	V
Output High Voltage DP, DM	V _{OHD}	R _L = 15kΩ from DP and DM to GND	2.8			V
Differential Input Sensitivity DP, DM	V _{DI}	DP to DM	0.2			V
Common-Mode Voltage Range	V _{CM}	Includes V _{DI} range	0.8		2.5	V

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RECOMMENDED OPERATING CONDITIONS (continued)

(V_{DD} = V_{RST} to 3.6V, T_A = 0°C to +70°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Single-Ended Receiver Threshold	V _{SE}		0.8		2.0	V
Single-Ended Receiver Hysteresis	V _{SEH}			200		mV
Differential Output Signal Cross-Point Voltage	V _{CRS}	C _L = 50pF (Note 6)	1.3		2.0	V
DP, DM Off-State Input Impedance	R _{LZ}		300			kΩ
Driver Output Impedance	R _{DRV}	Steady-state drive	28		44	Ω
DP Pullup Resistor	R _{PU}	Idle	0.9		1.575	kΩ
		Receiving	1.425		3.090	
USB TIMING						
DP, DM Rise Time (Transmit)	t _R	C _L = 50pF	4		20	ns
DP, DM Fall Time (Transmit)	t _F	C _L = 50pF	4		20	ns
Rise/Fall Time Matching (Transmit)	t _R /t _F	C _L = 50pF (Note 6)	90		110	%
IR						
Carrier Frequency	f _{IR}				f _{CK} /2	Hz
SPI (Note 6)						
SPI Master Operating Frequency	1/t _{MCK}				f _{CK} /2	MHz
SPI Slave Operating Frequency	1/t _{SCK}				f _{CK} /4	MHz
SPI I/O Rise/Fall Time	t _{SPI_RF}	C _L = 15pF, pullup = 560Ω	8		24	ns
SCLK_ Output Pulse-Width High/Low	t _{MCH} , t _{MCL}		t _{MCK} /2 - t _{SPI_RF}			ns
MOSI_ Output Hold Time After SCLK_ Sample Edge	t _{MOH}		t _{MCK} /2 - t _{SPI_RF}			ns
MOSI_ Output Valid to Sample Edge	t _{MOV}		t _{MCK} /2 - t _{SPI_RF}			ns
MISO_ Input Valid to SCLK_ Sample Edge Rise/Fall Setup	t _{MIS}		25			ns
MISO_ Input to SCLK_ Sample Edge Rise/Fall Hold	t _{MIH}		0			ns
SCLK_ Inactive to MOSI_ Inactive	t _{MLH}		t _{MCK} /2 - t _{SPI_RF}			ns
SCLK_ Input Pulse-Width High/Low	t _{SCH} , t _{SCL}			t _{SCK} /2		ns
SSEL_ Active to First Shift Edge	t _{SSE}		t _{SPI_RF}			ns

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RECOMMENDED OPERATING CONDITIONS (continued)

(V_{DD} = V_{RST} to 3.6V, T_A = 0°C to +70°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MOSI_ Input to SCLK_ Sample Edge Rise/Fall Setup	t _{SIS}		t _{SPI_RF}			ns
MOSI_ Input from SCLK_ Sample Edge Transition Hold	t _{SIH}		t _{SPI_RF}			ns
MISO_ Output Valid After SCLK_ Shift Edge Transition	t _{SOV}				50	ns
$\overline{\text{SSEL}}$ _ Inactive	t _{SSH}		t _{CK} + t _{SPI_RF}			ns
SCLK_ Inactive to $\overline{\text{SSEL}}$ _ Rising	t _{SD}		t _{SPI_RF}			ns
MISO_ Output Disabled After $\overline{\text{SSEL}}$ _ Edge Rise	t _{SLH}				2t _{CK} + 2t _{SPI_RF}	ns

I²C ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.7V to 3.6V, T_A = 0°C to +70°C.) (Note 1, Figure 1)

PARAMETER	SYMBOL	CONDITIONS	STANDARD MODE		FAST MODE		UNITS
			MIN	MAX	MIN	MAX	
Input Low Voltage	V _{IL_I2C}	(Note 18)	-0.5	0.3 x V _{DD}	-0.5	0.3 x V _{DD}	V
Input High Voltage	V _{IH_I2C}	(Note 18)	0.7 x V _{DD}		0.7 x V _{DD}	V _{DD} + 0.5V	V
Input Hysteresis (Schmitt)	V _{IHYS_I2C}	V _{DD} > 2V			0.05 x V _{DD}		V
Output Logic-Low (Open Drain or Open Collector)	V _{OL_I2C}	V _{DD} > 2V, 3mA sink current	0	0.4	0	0.4	V
Output Fall Time from V _{IH_MIN} to V _{IL_MAX} with Bus Capacitance from 10pF to 400pF	t _{OF_I2C}	(Notes 19, 20)		250	20 + 0.1C _B	250	ns
Pulse Width of Spike Filtering That Must Be Suppressed by Input Filter	t _{SP_I2C}				0	50	ns
Input Current on I/O	I _{IN_I2C}	Input voltage from 0.1 x V _{DD} to 0.9 x V _{DD}	-10	+10	-10	+10	μA
I/O Capacitance	C _{IO_I2C}			10		10	pF

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I²C BUS CONTROLLER TIMING

(Notes 6, 21) (Figure 2)

PARAMETER	SYMBOL	STANDARD MODE		FAST MODE		UNITS
		MIN	MAX	MIN	MAX	
I ² C Bus Operating Frequency	f _{I2C}	0	100	0	400	kHz
System Frequency	f _{SYS}	0.90		3.60		MHz
I ² C Bit Rate	f _{I2C}		f _{SYS} /8		f _{SYS} /8	Hz
Hold Time After (Repeated) START	t _{HD:STA}	4.0		0.6		μs
Clock Low Period	t _{LOW_I2C}	4.7		1.3		μs
Clock High Period	t _{HIGH_I2C}	4.0		0.6		μs
Setup Time for Repeated START	t _{SU:STA}	4.7		0.6		μs
Hold Time for Data (Notes 22, 23)	t _{HD:DAT}	0	3.45	0	0.9	μs
Setup Time for Data (Note 24)	t _{SU:DAT}	250		100		ns
SDA/SCL Fall Time (Note 20)	t _{F_I2C}		300	20 + 0.1C _B	300	ns
SDA/SCL Rise Time (Note 20)	t _{R_I2C}		1000	20 + 0.1C _B	300	ns
Setup Time for STOP	t _{SU:STO}	4.0		0.6		μs
Bus Free Time Between STOP and START	t _{BUF}	4.7		1.3		μs
Capacitive Load for Each Bus Line	C _B		400		400	pF
Noise Margin at the Low Level for Each Connected Device (Including Hysteresis)	V _{nL_I2C}	0.1 x V _{DD}		0.1 x V _{DD}		V
Noise Margin at the Low Level for Each Connected Device (Including Hysteresis)	V _{nH_I2C}	0.2 x V _{DD}		0.2 x V _{DD}		V

Note 1: Specifications to 0°C are guaranteed by design and are not production tested.

Note 2: V_{PFW} can be programmed to the following nominal voltage trip points: 1.8V, 1.9V, 2.55V, and 2.75V ±3%. The values listed in the *Recommended Operating Conditions* table are for the default configuration of 1.8V nominal.

Note 3: It is not recommended to write to flash when the supply voltage drops below the power-fail warning levels, as there is uncertainty in the duration of continuous power supply. The user application should check the status of the power-fail warning flag before writing to flash to ensure complete write operations.

Note 4: The power-fail warning monitor and the power-fail reset monitor are designed to track each other with a minimum delta between the two of 0.11V.

Note 5: The power-fail reset and POR detectors are designed to operate in tandem to ensure that one or both of these signals is active at all times when V_{DD} < V_{RST}, ensuring the device maintains the reset state until minimum operating voltage is achieved.

Note 6: Guaranteed by design and not production tested.

Note 7: I_{S1} is measured with the USB data RAM powered down.

Note 8: The power-check interval (PCI) can be set to always on, or to 1024, 2048, or 4096 nanopower ring clock cycles.

Note 9: Measured on the V_{DD} pin and the device not in reset. All inputs are connected to GND or V_{DD}. Outputs do not source/sink any current. The device is executing code from flash memory.

Note 10: Current consumption during POR when powering up while V_{DD} is less than the POR release voltage.

Note 11: The minimum amount of time that V_{DD} must be below V_{PFW} before a power-fail event is detected.

Note 12: The maximum total current, I_{OH(MAX)} and I_{OL(MAX)}, for all listed outputs combined should not exceed 25mA to satisfy the maximum specified voltage drop. This does not include the IRTX output.

Note 13: External clock frequency must be 12MHz to support USB functionality. Full-speed USB(12Mbps)-required bit-rate accuracy is ±2500ppm or ±0.25%. This is inclusive of all potential error sources: frequency tolerance, temperature, aging, crystal capacitive loading, board layout, etc.

Note 14: Programming time does not include overhead associated with utility ROM interface.

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Note 15: For USB operation, both V_{DD} and V_{BUS} must be connected.

Note 16: FRCVDD is the force V_{DD} power-supply bit (PWCN.10). When FRCVDD = 1, V_{DDB} power switching is disabled, and V_{DD} is always used as the core 3V power supply.

Note 17: The ESD protection scheme is in production on existing parts. The $1\mu\text{F}$ capacitor on V_{BUS} is intended to protect that pin from ESD damage (rather than DP or DM) since it is externally exposed. The ESD test uses 150pF charged to 15kV applied to the $1\mu\text{F}$ capacitor creating a delta V of approximately 2.25V and limiting the voltage on V_{BUS} .

Note 18: Devices that use nonstandard supply voltages that do not conform to the intended I²C bus system levels must relate their input levels to the voltage to which the pullup resistors R_p are connected.

Note 19: The maximum fall time, t_{F_I2C} of 300ns for the SDA and SCL bus lines is longer than the specified maximum t_{OF_I2C} of 250ns for the output stages. This allows series protection resistors (R_s) to be connected between the SDA/SCL pins and the SDA/SCL bus lines as shown in I²C Bus Controller Timing without exceeding the maximum specified fall time.

Note 20: C_B = Capacitance of one bus line in pF.

Note 21: All values referred to $V_{IH_I2C}(\text{MIN})$ and $V_{IL_I2C}(\text{MAX})$.

Note 22: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IH_I2C}(\text{MIN})$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 23: The maximum $t_{HD:DAT}$ need only be met if the device does not stretch the low period (t_{LOW_I2C}) of the SCL signal.

Note 24: A fast-mode I²C bus device can be used in a standard-mode I²C bus system, but the requirement $t_{SU:DAT} \geq 250\text{ns}$ must be met. This is automatically the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line $t_{R_I2C}(\text{MAX}) + t_{SU:DAT} = 1000 + 250 = 1250\text{ns}$ (according to the standard-mode I²C specification) before the SCL line is released.

Note 25: AC electrical specifications are guaranteed by design and are not production tested.

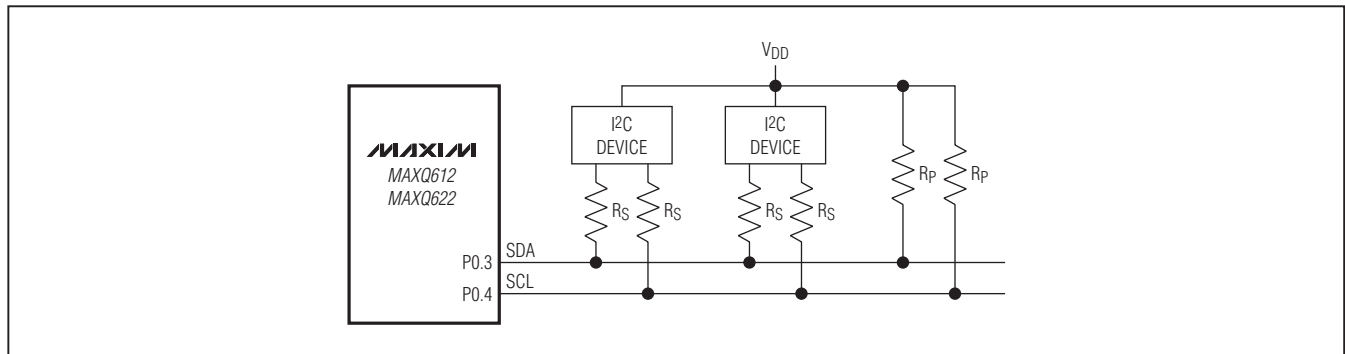


Figure 1. Series Resistors (R_s) for Protecting Against High-Voltage Spikes

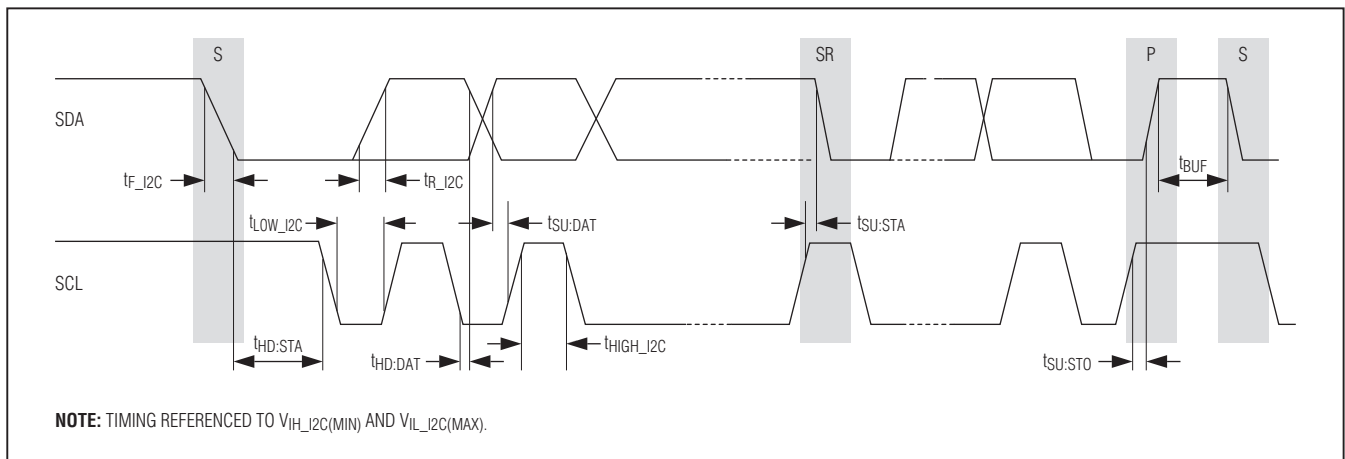
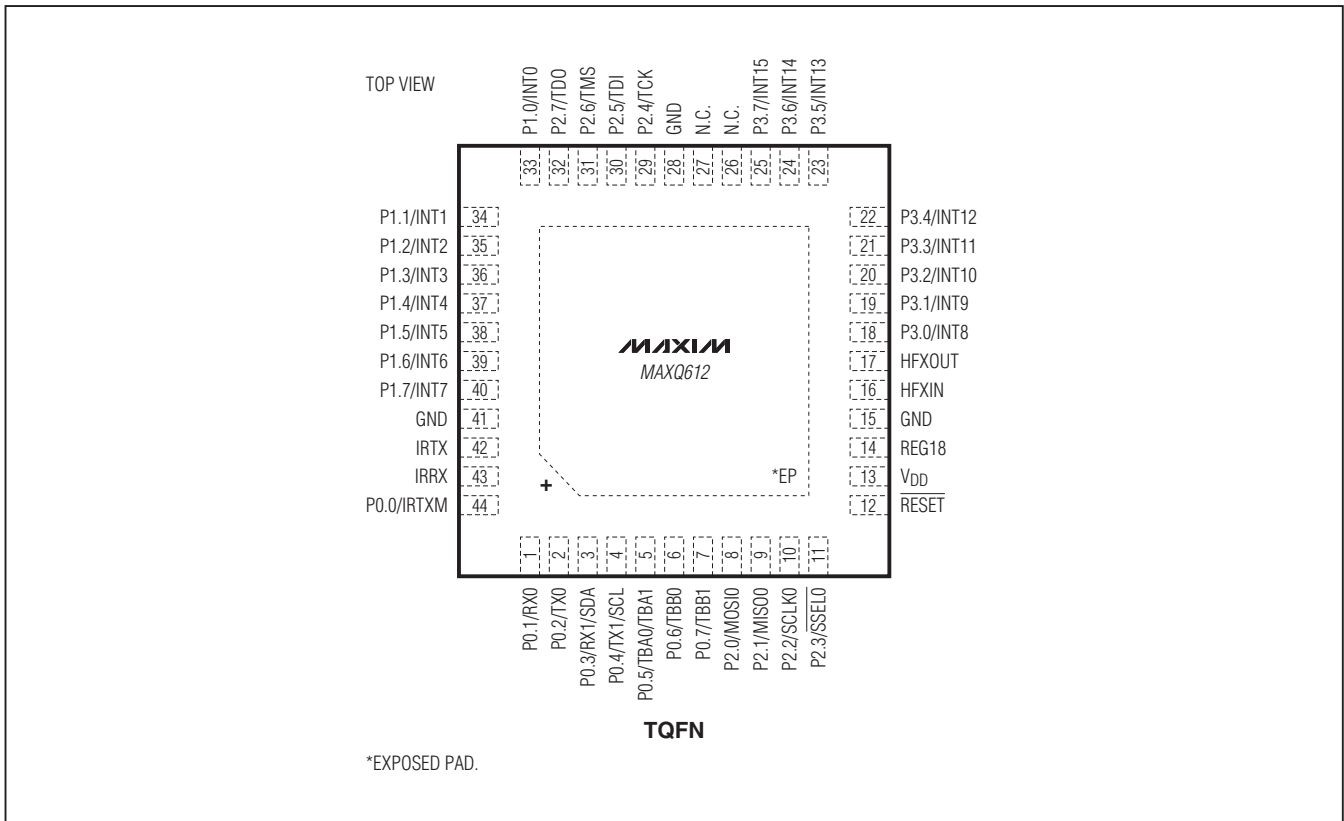


Figure 2. I²C Bus Controller Timing Diagram

16-Bit Microcontrollers with Infrared Module and Optional USB

Pin Configurations

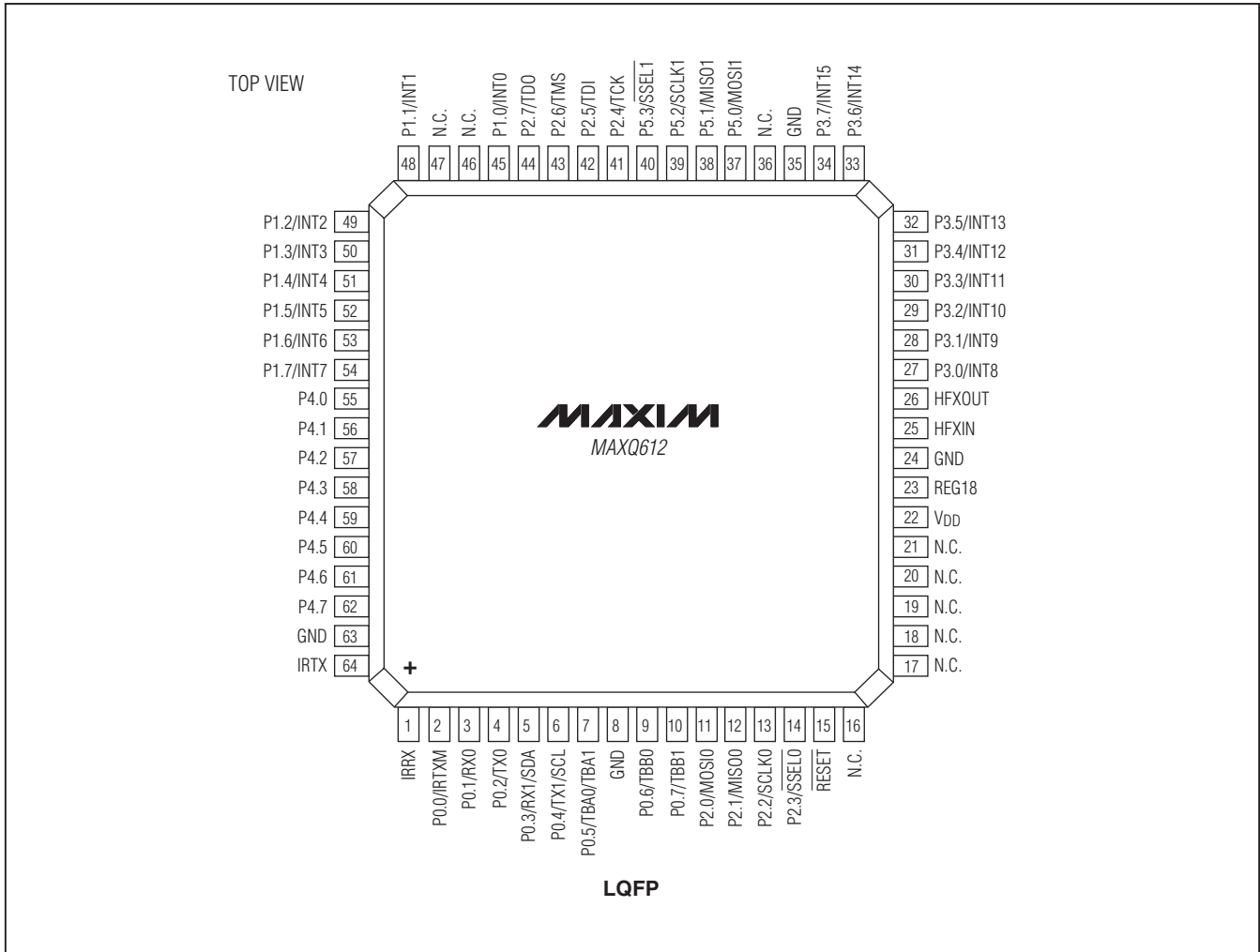
MAXQ612/MAXQ622



16-Bit Microcontrollers with Infrared Module and Optional USB

Pin Configurations (continued)

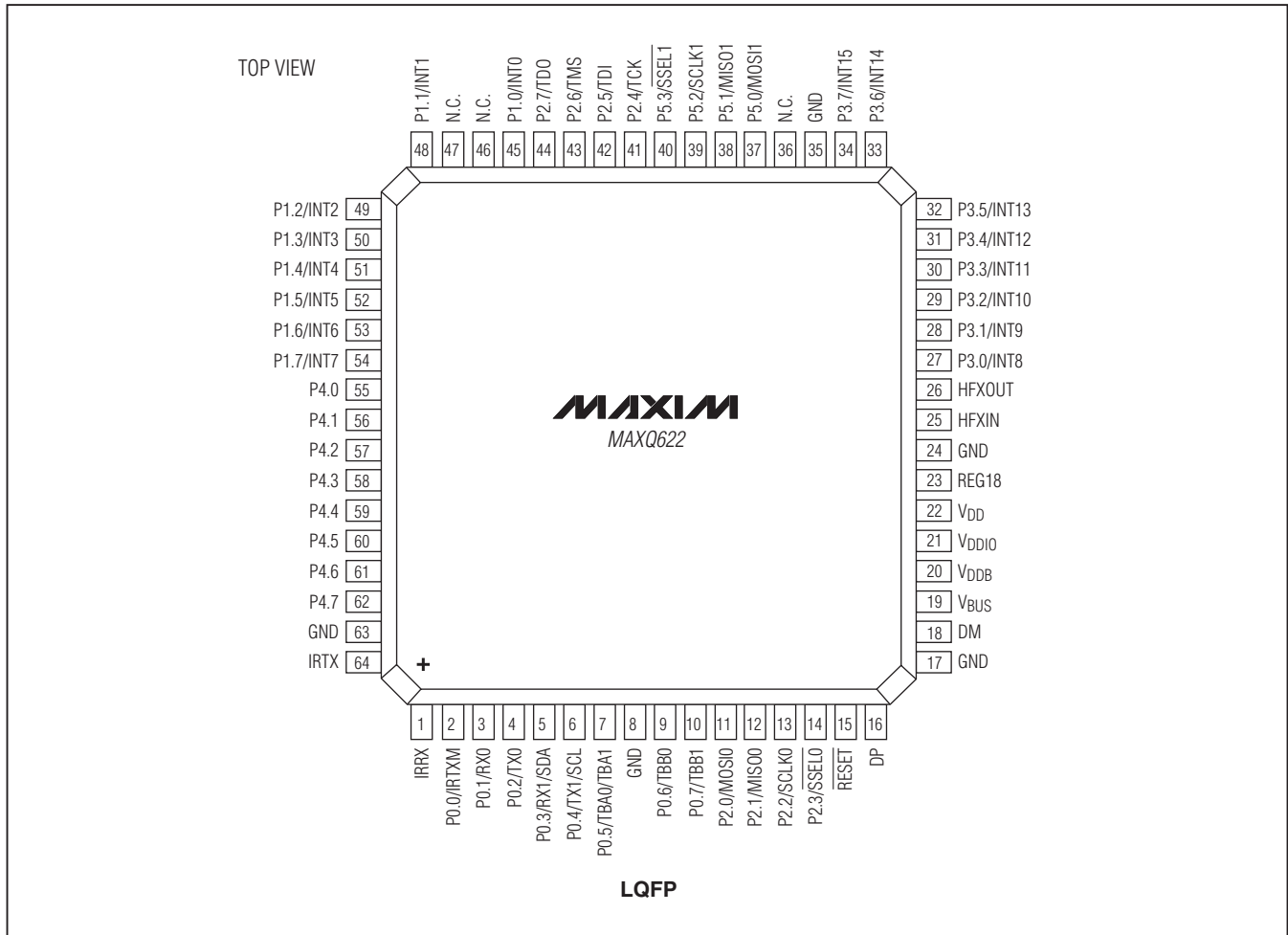
MAXQ612/MAXQ622



16-Bit Microcontrollers with Infrared Module and Optional USB

Pin Configurations (continued)

MAXQ612/MAXQ622



Pin Description

PIN			NAME	FUNCTION
MAXQ612 TQFN-EP	MAXQ612 LQFP	MAXQ622 LQFP		
POWER PINS				
13	22	22	VDD	Supply Voltage
15, 28, 41	8, 24, 35, 63	8, 17, 24, 35, 63	GND	Ground
14	23	23	REG18	Regulator Capacitor. This pin must be connected to ground through a 1.0µF external ceramic-chip capacitor. The capacitor must be placed as close to this pin as possible. No external devices other than the capacitor should be connected to this pin.
—	—	—	EP	Exposed Pad (TQFN Only). Connect EP to the ground plane.

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MAXQ612/MAXQ622

Pin Description (continued)

PIN			NAME	FUNCTION
MAXQ612 TQFN-EP	MAXQ612 LQFP	MAXQ622 LQFP		
RESET PINS				
12	15	15	$\overline{\text{RESET}}$	Digital, Active-Low, Reset Input/Output. The CPU is held in reset when this pin is low and begins executing from the reset vector when released. The pin includes pullup current source and should be driven by an open-drain, external source capable of sinking in excess of 4mA. This pin is driven low as an output when an internal reset condition occurs.
CLOCK PINS				
16	25	25	HFXIN	High-Frequency Crystal Input. Connect an external crystal or resonator between HFXIN and HFXOUT as the high-frequency system clock. Alternatively, HFXIN is the input for an external, high-frequency clock source when HFXOUT is shorted to ground during POR.
17	26	26	HFXOUT	
USB FUNCTION PINS				
—	—	19	V _{BUS}	USB V _{BUS} Supply Voltage. Connect V _{BUS} to a positive 5.0V power supply. Bypass V _{BUS} to ground with a 1.0μF ceramic capacitor as close to the V _{BUS} pin as possible.
—	—	16	DP	USB D+ Signal. This bidirectional pin carries the positive differential data or single-ended data. Connect this pin to a USB “B” connector. This pin is weakly pulled high internally when the USB is disabled.
—	—	18	DM	USB D- Signal. This bidirectional pin carries the negative differential data or single-ended data. Connect this pin to a USB “B” connector. This pin is weakly pulled high internally when the USB is disabled.
—	—	20	V _{DDB}	USB Transceiver Supply Voltage. This is the power output of the internal voltage regulator that is used for the USB transceiver (3.3V) block. This pin is bypassed to ground with a 1.0μF capacitor as close as possible to the package. No external circuitry should be powered from this pin.
—	—	21	V _{DDIO}	Switched 3V Power Supply. This is the power output after selection between V _{BUS} and V _{DD} . Must be connected to an external ceramic chip capacitor. The capacitor must be placed as close to this pin as possible. No external devices other than the capacitor should be connected to this pin.
IR FUNCTION PINS				
42	64	64	IRTX	IR Transmit Output. Active-low IR transmit pin capable of sinking 25mA. This pin defaults to three-state input with the weak pullup disabled during all forms of reset. Software must configure this pin after release from reset to remove the three-state input condition.
43	1	1	IRRX	IR Receive Input

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Pin Description (continued)

PIN			NAME	FUNCTION				
MAXQ612 TQFN-EP	MAXQ612 LQFP	MAXQ622 LQFP						
GENERAL-PURPOSE I/O AND SPECIAL FUNCTION PINS								
44, 1–7	2–7, 9, 10	2–7, 9, 10	P0.0–P0.7; IRTXM, RX0, TX0, RX1, TX1, SDA, SCL, TBA0, TBA1, TBB0, TBB1	General-Purpose, Digital, I/O, Type C Port. These port pins function as bidirectional I/O pins. All port pins default to three-state mode after a reset. All alternate functions must be enabled from software.				
				MAXQ612 TQFN-EP	MAXQ612 LQFP	MAXQ622 LQFP	PORT	SPECIAL FUNCTION
				44	2	2	P0.0	IRTXM
				1	3	3	P0.1	RX0
				2	4	4	P0.2	TX0
				3	5	5	P0.3	RX1/SDA
				4	6	6	P0.4	TX1/SCL
				5	7	7	P0.5	TBA0/TBA1
				6	9	9	P0.6	TBB0
7	10	10	P0.7	TBB1				
33–40	45, 48–54	45, 48–54	P1.0–P1.7; INT0–INT7	General-Purpose, Digital, I/O, Type D Port; External Edge-Selectable Interrupt. These port pins function as bidirectional I/O pins or as interrupts. All port pins default to three-state mode after a reset. All interrupt functions must be enabled from software.				
				MAXQ612 TQFN-EP	MAXQ612 LQFP	MAXQ622 LQFP	PORT	SPECIAL FUNCTION
				33	45	45	P1.0	INT0
				34	48	48	P1.1	INT1
				35	49	49	P1.2	INT2
				36	50	50	P1.3	INT3
				37	51	51	P1.4	INT4
				38	52	52	P1.5	INT5
				39	53	53	P1.6	INT6
40	54	54	P1.7	INT7				

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Pin Description (continued)

PIN			NAME	FUNCTION				
MAXQ612 TQFN-EP	MAXQ612 LQFP	MAXQ622 LQFP						
8–11, 29–32	11–14, 41–44	11–14, 41–44	P2.0–P2.7; MOSIO, MISO0, SCLK0, SSEL0, TCK, TDI, TMS, TDO	General-Purpose, Digital, I/O, Type C Port. These port pins function as bidirectional I/O pins. P2.0 to P2.3 default to three-state mode after a reset. All alternate functions must be enabled from software. Enabling the pin's special function disables the general-purpose I/O on the pin. The JTAG pins (P2.4 to P2.7) default to their JTAG function with weak pullups enabled after a reset. The JTAG function can be disabled using the TAP bit in the SC register. P2.7 functions as the JTAG test-data output on reset and defaults to an input with a weak pullup. The output function of the test data is only enabled during the TAP's shift_IR or shift_DR states.				
				MAXQ612 TQFN-EP	MAXQ612 LQFP	MAXQ622 LQFP	PORT	SPECIAL FUNCTION
				8	11	11	P2.0	MOSIO
				9	12	12	P2.1	MISO0
				10	13	13	P2.2	SCLK0
				11	14	14	P2.3	SSEL0
				29	41	41	P2.4	TCK
				30	42	42	P2.5	TDI
				31	43	43	P2.6	TMS
			32	44	44	P2.7	TDO	
18–25	27–34	27–34	P3.0–P3.7; INT8–INT15	General-Purpose, Digital, I/O, Type D Port; External Edge-Selectable Interrupt. These port pins function as bidirectional I/O pins or as interrupts. All port pins default to three-state mode after a reset. All interrupt functions must be enabled from software.				
				MAXQ612 TQFN	MAXQ612 LQFP	MAXQ622 LQFP	PORT	SPECIAL FUNCTION
				18	27	27	P3.0	INT8
				19	28	28	P3.1	INT9
				20	29	29	P3.2	INT10
				21	30	30	P3.3	INT11
				22	31	31	P3.4	INT12
				23	32	32	P3.5	INT13
				24	33	33	P3.6	INT14
			25	34	34	P3.7	INT15	

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Pin Description (continued)

MAXQ612/MAXQ622

PIN			NAME	FUNCTION				
MAXQ612 TQFN-EP	MAXQ612 LQFP	MAXQ622 LQFP		MAXQ612 TQFN-EP	MAXQ612 LQFP	MAXQ622 LQFP	PORT	SPECIAL FUNCTION
—	55-62	55-62	P4.0-P4.7	General-Purpose, Digital, I/O, Type C Port. These port pins function as bidirectional I/O pins. All port pins default to three-state mode after a reset.				
				—	55	55	P4.0	—
				—	56	56	P4.1	—
				—	57	57	P4.2	—
				—	58	58	P4.3	—
				—	59	59	P4.4	—
				—	60	60	P4.5	—
				—	61	61	P4.6	—
—	37-40	37-40	P5.0-P5.3; MOSI1, MISO1, SCLK1, SSEL1	General-Purpose, Digital, I/O, Type C Port. These port pins function as bidirectional I/O pins. All port pins default to three-state mode after a reset. All alternate functions must be enabled from software. Enabling the pin's special function disables the general-purpose I/O on the pin.				
				—	37	37	P5.0	MOSI1
				—	38	38	P5.1	MISO1
				—	39	39	P5.2	SCLK1
				—	40	40	P5.3	SSEL1
NO CONNECTION PINS								
26, 27	16-21, 36, 46, 47	36, 46, 47	N.C.	No Connection. Reserved for future use. Leave these pins unconnected.				

Detailed Description

The MAXQ612/MAXQ622 provide integrated, low-cost solutions that simplify the design of IR communications equipment such as universal remote controls. Standard features include the highly optimized, single-cycle, MAXQ, 16-bit RISC core; 128KB of flash memory; 6KB data RAM; soft stack; 16 general-purpose registers; and three data pointers. The MAXQ core has the industry's best MIPS/mA rating, allowing developers to achieve the same performance as competing microcontrollers at substantially lower clock rates. Lower active-mode current combined with the even lower MAXQ612/MAXQ622 stop-mode current results in increased battery life. IR application-specific peripherals include flexible timers

for generating IR carrier frequencies and modulation. A high-current, 25mA, IR drive pin and output pins capable of sinking up to 5mA support IR applications. It also includes a USB slave interface compatible with existing host HID device drivers, I²C, dual SPI, dual USARTs, up to 56 general-purpose I/O pins ideal for keypad matrix input, and a power-fail-detection circuit to notify.

Operating from DC to 12MHz, almost all instructions execute in a single clock cycle (83.3ns at 12MHz), enabling nearly 12MIPS true-code operation. When active device operation is not required, an ultra-low-power stop mode can be invoked from software, resulting in quiescent current consumption of less than 300nA typical and 3μA maximum. The combination of high-performance instructions and ultra-low

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stop-mode current increases battery life over competing microcontrollers. An integrated POR circuit with brownout support resets the device to a known condition following a power-up cycle or brownout condition. Additionally, a power-fail warning flag is set, and a power-fail interrupt can be generated when the system voltage falls below the power-fail warning voltage, V_{PFW} . The power-fail warning feature allows the application to notify the user that the system supply is low and appropriate action should be taken.

Microprocessor

The MAXQ612/MAXQ622 are based on Maxim's MAXQ20 core, which is a low-power implementation of the new 16-bit MAXQ family of RISC cores. The core supports the Harvard memory architecture with separate internal 16-bit program and data address buses. A fixed 16-bit instruction word is standard, but data can be arranged in 8 or 16 bits. The MAXQ core is a pipelined processor with performance approaching 1MIPS per MHz. The 16-bit data path is implemented around register modules, and each register module contributes specific functions to the core. The accumulator module consists of sixteen 16-bit registers and is tightly coupled with the arithmetic logic unit (ALU). Program flow is supported by a configurable soft stack.

Execution of instructions is triggered by data transfer between functional register modules or between a functional register module and memory. Because data movement involves only source and destination modules, circuit switching activities are limited to active modules only. For power-conscious applications, this approach localizes power dissipation and minimizes switching noise. The modular architecture also provides a maximum of flexibility and reusability that are important for a microprocessor used in embedded applications.

The MAXQ instruction set is highly orthogonal. All arithmetical and logical operations can use any register in conjunction with the accumulator. Data movement is supported from any register to any other register.

Memory is accessed through specific data-pointer registers with autoincrement/decrement support.

Memory

The microcontroller incorporates several memory types:

- 128KB program flash memory
- 6KB SRAM data memory
- 6KB utility ROM
- Soft stack

Memory Protection

The optional memory-protection feature separates code memory into three areas: system, user loader, and user application. Code in the system area can be kept confidential. Code in the user areas can be prevented from reading and writing system code. The user loader can also be protected from user application code.

Memory protection is implemented using privilege levels for code. Each area has an associated privilege level. RAM/ROM are assigned privilege levels as well. Refer to the *MAXQ622 User's Guide* for a more thorough explanation of the topic.

Stack Memory

A 16-bit-wide internal stack provides storage for program return addresses and can also be used for general-purpose data storage. The stack is used automatically by the processor when the CALL, RET, and RETI instructions are executed and when an interrupt is serviced. An application can also store values in the stack explicitly by using the PUSH, POP, and POPI instructions.

On reset, the stack pointer, SP, initializes to the top of the stack (BF0h). The CALL, PUSH, and interrupt-vectoring operations decrement SP, then store a value at the location pointed to by SP. The RET, RETI, POP, and POPI operations retrieve the value at SP and then increment SP.

Utility ROM

The utility ROM is a 6KB block of internal ROM memory that defaults to a starting address of 8000h. The utility

Table 1. Memory Areas and Associated Maximum Privilege Levels

AREA	PAGE ADDRESS	MAXIMUM PRIVILEGE LEVEL
System	0 to ULDR-1	High
User Loader	ULDR to UAPP-1	Medium
User Application	UAPP to top	Low
Utility ROM	N/A	High
Other (RAM)	N/A	Low

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ROM consists of subroutines that can be called from application software. These include the following:

- In-system programming (bootstrap loader) using JTAG interface
- In-circuit debug routines
- Test routines (internal memory tests, memory loader, etc.)
- User-callable routines for in-application flash memory programming and fast table lookup

Following any reset, execution begins in the utility ROM. The ROM software determines whether the program execution should immediately jump to location 0000h, the start of system code, or to one of the special routines mentioned. Routines within the utility ROM are user accessible and can be called as subroutines by the application software. More information on the utility ROM functions is contained in the *MAXQ622 User's Guide*.

Some applications require protection against unauthorized viewing of program code memory. For these applications, access to in-system programming, in-application programming, or in-circuit debugging functions is prohibited until a password has been supplied. The password is defined as the 16 words of physical program memory at addresses 0010h to 001Fh.

Three password locks protect three different program memory segments. When the PWL is set to one (power-on reset default) and the contents of the memory at addresses 0010h to 001Fh are any value other than FFh or 00h, the password is required to access the utility ROM, including in-circuit debug and in-system programming routines that allow reading or writing of internal memory. When PWL is cleared to zero, these utilities are fully accessible without password. The PWLS bit uses a password that is at ULDR + 0010 to ULDR + 001F, and the PWLL uses a password at UAPP + 0010 to UAPP + 001F. The password is automatically set to all ones following a mass erase.

Watchdog Timer

The internal watchdog timer greatly increases system reliability. The timer resets the device if software execution is disturbed. The watchdog timer is a free-running counter designed to be periodically reset by the application software. If software is operating correctly, the counter is periodically reset and never reaches its maximum count. However, if software operation is interrupted, the timer does not reset, triggering a system reset and optionally a watchdog timer interrupt. This protects the system against electrical noise or electrostatic discharge (ESD) upsets that could cause uncontrolled processor operation. The internal watchdog timer is an upgrade to older designs with external watchdog devices, reducing system cost and simultaneously increasing reliability.

The watchdog timer functions as the source of both the watchdog timer timeout and the watchdog timer reset. The timeout period can be programmed in a range of 2^{15} to 2^{24} system clock cycles. An interrupt is generated when the timeout period expires if the interrupt is enabled. All watchdog timer resets follow the programmed interrupt timeouts by 512 system clock cycles. If the watchdog timer is not restarted for another full interval in this time period, a system reset occurs when the reset timeout expires.

IR Carrier Generation and Modulation Timer

The dedicated IR timer/counter module simplifies low-speed infrared (IR) communication. The IR timer implements two pins (IRTX and IRRX) for supporting IR transmit and receive, respectively. The IRTX pin has no corresponding port pin designation, so the standard PD, PO, and PI port control status bits are not present. However, the IRTX pin output can be manipulated high or low using the PWCN.IRTXOUT and PWCN.IRTXOE bits when the IR timer is not enabled (i.e., IREN = 0).

Table 2. Watchdog Interrupt Timeout (Sysclk = 12MHz, CD[1:0] = 00)

WD[1:0]	WATCHDOG CLOCK	WATCHDOG INTERRUPT TIMEOUT	WATCHDOG RESET AFTER WATCHDOG INTERRUPT (μs)
00	Sysclk/2 ¹⁵	2.7ms	42.7
01	Sysclk/2 ¹⁸	21.9ms	42.7
10	Sysclk/2 ²¹	174.7ms	42.7
11	Sysclk/2 ²⁴	1.4s	42.7

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The IR timer is composed of a carrier generator and a carrier modulator. The carrier generation module uses the 16-bit IR carrier register (IRCA) to define the high and low time of the carrier through the IR carrier high byte (IRCAH) and IR carrier low byte (IRCAL). The carrier modulator uses the IR data bit (IRDATA) and IR modulator time register (IRMT) to determine whether the carrier or the idle condition is present on IRTX.

Carrier Generation Module

The IRCAH byte defines the carrier high time in terms of the number of IR input clocks, whereas the IRCAL byte defines the carrier low time.

- IR Input Clock (f_{IRCLK}) = $f_{SYS}/2^{IRDIV[1:0]}$
- Carrier Frequency ($f_{CARRIER}$) = $f_{IRCLK}/(IRCAH + IRCAL + 2)$
- Carrier High Time = $IRCAH + 1$
- Carrier Low Time = $IRCAL + 1$
- Carrier Duty Cycle = $(IRCAH + 1)/(IRCAH + IRCAL + 2)$

During transmission, the IRCA register is latched for each IRV downcount interval, and is sampled along with the IRTXPOL and IRDATA bits at the beginning of each new IRV downcount interval so that duty-cycle variation and frequency shifting is possible from one interval to the next. The starting/idle state and the carrier polarity of the IRTX pin can be configured when the IR timer is enabled.

IR Transmission

During IR transmission ($IRMODE = 1$), the carrier generator creates the appropriate carrier waveform, while the carrier modulator performs the modulation. The carrier modulation can be performed as a function of carrier cycles or IRCLK cycles dependent on the setting of the IRCFME bit. When $IRCFME = 0$, the IRV down counter is clocked by the carrier frequency and thus the modulation is a function of carrier cycles. When $IRCFME = 1$, the IRV down counter is clocked by IRCLK, allowing carrier modulation timing with IRCLK resolution.

The IRTXPOL bit defines the starting/idle state as well as the carrier polarity for the IRTX pin. If $IRTXPOL = 1$, the IRTX pin is set to a logic-high when the IR timer module is enabled. If $IRTXPOL = 0$, the IRTX pin is set to a logic-low when the IR timer is enabled.

A separate register bit, IR data (IRDATA), is used to determine whether the carrier generator output is output to the IRTX pin for the next IRMT carrier cycles. When $IRDATA = 1$, the carrier waveform (or inversion of this waveform if $IRTXPOL = 1$) is output on the IRTX pin during the next IRMT cycles. When $IRDATA = 0$, the idle

condition, as defined by IRTXPOL, is output on the IRTX pin during the next IRMT cycles.

The IR timer acts as a down counter in transmit mode. An IR transmission starts when the IREN bit is set to 1 when $IRMODE = 1$; when the IREN bit is set to 1 when $IRMODE = 1$; or when IREN and IREN are both set to 1 in the same instruction. The IRMT and IRCA registers, along with the IRDATA and IRTXPOL bits, are sampled at the beginning of the transmit process and every time the IR timer value reload its value. When the IRV reaches 0000h value, on the next carrier clock, it does the following:

- 1) Reloads IRV with IRMT.
- 2) Samples IRCA, IRDATA, and IRTXPOL.
- 3) Generates IRTX accordingly.
- 4) Sets IRIF to 1.
- 5) Generates an interrupt to the CPU if enabled ($IRIE = 1$).

IR Transmit—Independent External Carrier and Modulator Outputs

The normal transmit mode modulates the carrier based upon the IRDATA bit. However, the user has the option to input the modulator (envelope) on an external pin if desired. The IRDATA bit is output directly to the IRTXM pin (if $IRTXPOL = 0$) on each IRV downcount interval boundary just as if it were being used to internally modulate the carrier frequency. If $IRTXPOL = 1$, the inverse of the IRDATA bit is output to the IRTXM pin on the IRV interval downcount boundaries. When the envelope mode is enabled, it is possible to output either the modulated ($IRENV[1:0] = 01b$) or unmodulated ($INENV[1:0] = 10b$) carrier to the IRTX pin.

IR Receive

When configured in receive mode ($IRMODE = 0$), the IR hardware supports the IRRX capture function. The IRRXSEL[1:0] bits define which edge(s) of the IRRX pin should trigger the IR timer capture function. Once started, the IR timer (IRV) starts up counting from 0000h when a qualified capture event as defined by IRRXSEL happens. The IRV register is, by default, counting carrier cycles as defined by the IRCA register. However, the IR carrier frequency detect (IRCFME) allows clocking of the IRV register directly with the IRCLK for finer resolution. When $IRCFME = 0$, the IRCA defined carrier is counted by IRV. When $IRCFME = 1$, the IRCLK clocks the IRV register.

On the next qualified event, it does the following:

- 1) Captures the IRRX pin state and transfers its value to IRDATA. If a falling edge occurs, $IRDATA = 0$. If a rising edge occurs, $IRDATA = 1$.

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- 2) Transfers its current IRV value to the IRMT.
- 3) Resets IRV content to 0000h (if IRXRL = 1).
- 4) Continues counting again until the next qualified event.

If the IR timer value rolls over from 0FFFFh to 0000h before a qualified event happens, the IR timer overflow (IROV) flag is set to 1 and an interrupt is generated, if enabled. The IR module continues to operate in receive mode until it is stopped by switching into transmit mode or clearing IREN = 0.

Carrier Burst-Count Mode

A special mode reduces the CPU processing burden when performing IR learning functions. Typically, when operating in an IR learning capacity, some number of carrier cycles are examined for frequency determination. Once the frequency has been determined, the IR receive function can be reduced to counting the number of carrier pulses in the burst and the duration of the combined mark-space time within the burst. To simplify this process, the receive burst-count mode can be used. When RXBCNT = 0, the standard IR receive capture functionality is in place. When RXBCNT = 1, the IRV capture operation is disabled and the interrupt flag associated with the capture no longer denotes a capture. In the carrier burst-count mode, the IRMT register only counts qualified edges. The IRIF interrupt flag now sets if two IRCA cycles elapse without getting a qualified edge. The IRIF interrupt flag thus denotes absence of the carrier and the beginning of a space in the receive signal. The IRCFME bit is still used to define whether the IRV register is counting system IRCLK clocks or IRCA-defined carrier cycles. The IRXRL bit defines whether the IRV register is reloaded with 0000h on detection of a qualified edge (per the IRXSEL[1:0] bits).

16-Bit Timers/Counters

The microcontroller provides two general-purpose timers/counters that support the following functions:

- 16-bit timer/counter
- 16-bit up/down autoreload
- Counter function of external pulse

- 16-bit timer with capture
- 16-bit timer with compare
- Input/output enhancements for pulse-width modulation
- Set/reset/toggle output state on comparator match
- Prescaler with 2ⁿ divider (for n = 0, 2, 4, 6, 8, 10)

General-Purpose I/O

The microcontroller provides port pins for general-purpose I/O that have the following features:

- CMOS output drivers
- Schmitt trigger inputs
- Optional weak pullup to V_{DD} when operating in input mode

While the microcontroller is in a reset state, all port pins become three-state with both weak pullups and input buffers disabled, unless otherwise noted.

From a software perspective, each port appears as a group of peripheral registers with unique addresses. Special function pins can also be used as general-purpose I/O pins when the special functions are disabled. For a detailed description of the special functions available for each pin, refer to the IC-specific user's guide, e.g., the *MAXQ622 User's Guide* describes all special functions available on the MAXQ612/MAXQ622.

Serial Peripherals

The microcontroller supports two independent USARTs, two SPI master/slave communications ports, and an I²C bus.

USART

The USART units are implemented with the following characteristics:

- 2-wire interface
- Full-duplex operation for asynchronous data transfers
- Half-duplex operation for synchronous data transfers
- Programmable interrupt for receive and transmit
- Independent baud-rate generator

Table 3. USART Mode Details

MODE	TYPE	START BITS	DATA BITS	STOP BITS
Mode 0	Synchronous	N/A	8	N/A
Mode 1	Asynchronous	1	8	1
Mode 2	Asynchronous	1	8 + 1	1
Mode 3	Asynchronous	1	8 + 1	1

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- Programmable 9th bit parity support
- Start/stop bit support

Serial Peripheral Interface (SPI)

The dual-integrated SPI interfaces provide independent serial communication channels that communicate synchronously with peripheral devices in a multiple master or multiple slave system. The interface allows access to a 4-wire, full-duplex serial bus, and can be operated in either master mode or slave mode. Collision detection is provided when two or more masters attempt a data transfer at the same time.

The maximum SPI master transfer rate is $\text{Sysclk}/2$. When operating as an SPI slave, the MAXQ612/MAXQ622 can support up to $\text{Sysclk}/4$ SPI transfer rate. Data is transferred as an 8-bit or 16-bit value, MSB first. In addition, the SPI module supports configuration of an active SSEL state through the slave active select. Separate pins and registers are used to differentiate between the two SPI ports.

I²C Bus

The microcontroller integrates an internal I²C bus master/slave for communication with a wide variety of other I²C-enabled peripherals. The I²C bus is a 2-wire, bidirectional bus using two bus lines—the serial data line (SDA) and the serial clock line (SCL)—and a ground line. Both the SDA and SCL lines must be driven as open-collector/drain outputs. External resistors are required as shown in Figure 1 to pull the lines to a logic-high state.

The device supports both the master and slave protocols. In the master mode, the device has ownership of the I²C bus, drives the clock, and generates the START and STOP signals. This allows it to send data to a slave or receive data from a slave as required. In slave mode, the device relies on an externally generated clock to drive SCL and responds to data and commands only when requested by the I²C master device.

USB Controller (MAXQ622 Only)

The integrated USB controller is compliant with the USB 2.0 specification, providing full-speed operation with the newest generation of USB peripherals. The USB controller functions as a full-speed USB peripheral device. Integrating the USB physical interface (PHY) allows direct connection to the USB cable, reducing board space and overall system cost. A system interrupt can be enabled to signal that the USB needs to be serviced. The CPU communicates to the USB controller module through the SFR interface. The microcontroller is seen

by a USB host as a peripheral, characterized by the following endpoints:

- EP0: Bidirectional CONTROL endpoint with a 64-byte data storage.
- EP1-OUT: BULK (or INT) OUT endpoint. Double-buffered 64 bytes data storage.
- EP2-IN: BULK (or INT) IN endpoint. Double-buffered 64 bytes data storage.
- EP3-IN: BULK (or INT) IN endpoint. Single-buffered 64 bytes data storage.

The choice to use EP1, EP2, and EP3 as BULK or INTERRUPT endpoints is strictly a function of the endpoint descriptors that the USB controller returns to the USB host during enumeration.

The USB controller communicates to a total of 384 bytes of endpoint data memory (2 x 64 bytes for each data moving endpoint EP1 and EP2), 64 bytes for the CONTROL endpoint, and 64 bytes for endpoint EP3.

Double-buffering EP1 and EP2 improves throughput by allowing the CPU to read or load the next packet while the USB controller is moving the current packet over USB. EP3-IN is intended to serve as a large interrupt endpoint for various USB class specifications such as the Still Image Capture Device. It can also be used as a second BULK IN endpoint.

On-Chip Oscillator

An external quartz crystal or a ceramic resonator can be connected between HFXIN and HFXOUT, as illustrated in Figure 3.

To operate the core from an external clock, connect the clock source to the HFXIN pin and connect the HFXOUT

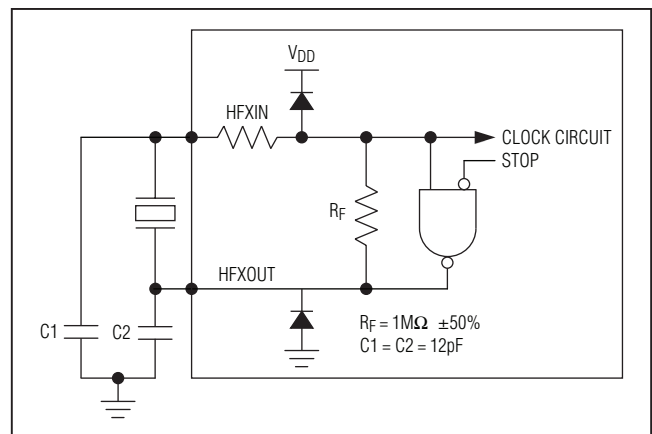


Figure 3. On-Chip Oscillator

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pin to GND. The clock source should be driven through a CMOS driver. If the clock driver is a TTL gate, its output must be connected to VDD through a pullup resistor to ensure a satisfactory logic level for active clock pulses. To minimize system noise on the clock circuitry, the external clock source must meet the maximum rise and fall times and the minimum high and low times specified for the clock source. The external noise can affect the clock generation circuit if these parameters do not meet the specification.

Noise at HFXIN and HFXOUT can adversely affect on-chip clock timing. It is good design practice to place the crystal and capacitors as near the oscillator circuitry as possible with a direct short trace. The typical values of external capacitors vary with the type of crystal to be used.

ROM Loader

The ROM loader loads program memory and configures loader-specific configuration features. To increase the security of the system, the loader denies access to the system, user loader, or user-application memories unless an area-specific password is provided.

Loading Flash Memory

An internal bootstrap loader allows reloading over a simple JTAG interface. As a result, software can be upgraded in-system, eliminating the need for a costly hardware retrofit when updates are required. Remote software uploads are possible that enable physically inaccessible applications to be frequently updated. The interface hardware can be a JTAG connection to another microcontroller, or a connection to a PC serial port using a USB-to-JTAG converter such as the MAXQUSBKIT#, available from Maxim. If in-system programmability is not required, a commercial gang programmer can be used for mass programming. Activating the JTAG interface and loading the test access port (TAP) with the system programming instruction invokes the bootstrap loader. Setting the SPE bit to one during reset through the JTAG interface executes the bootstrap-loader mode program that resides in the utility ROM. When programming is complete, the bootstrap loader can clear the SPE bit and reset the device, allowing the device to bypass the utility ROM and begin execution of the application software.

In addition, the ROM loader also enforces the memory-protection policies. Passwords that are 16 words are required to access the ROM loader interface.

In-Application Flash Programming

From user-application code, flash memory can be programmed using the ROM utility functions from either C or assembly language. The function declarations below show examples of some of the ROM utility functions provided for in-application flash memory programming:

```
/* Write one 16-bit word to code address 'dest'.
 * Dest must be aligned to 16 bits.
 * Returns 0 = failure, 1 = OK.
 */
int flash_write (uint16_t dest, uint16_t data);
To erase, the following function would be used:
/* Erase the given Flash page
 * addr: Flash offset (anywhere within page)
 */
int flash_erasepage(uint16_t addr);
```

The in-application flash memory programming must call ROM utility functions to erase and program any of the flash memory. Memory protection is enforced by the ROM utility functions.

In-Circuit Debug and JTAG Interface

Embedded debug hardware and software are developed and integrated to provide full in-circuit debugging capability in a user-application environment. These hardware and software features include the following:

- Debug engine
- Set of registers providing the ability to set breakpoints on register, code, or data using debug service routines stored in ROM

Collectively, these hardware and software features support two modes of in-circuit debug functionality:

- Background mode:
 - CPU is executing the normal user program
 - Allows the host to configure and set up the in-circuit debugger
- Debug mode:
 - Debugger takes over the control of the CPU
 - Read/write accesses to internal registers and memory
 - Single-step of the CPU for trace operation

The interface to the debug engine is the TAP controller. The interface allows for communication with a bus

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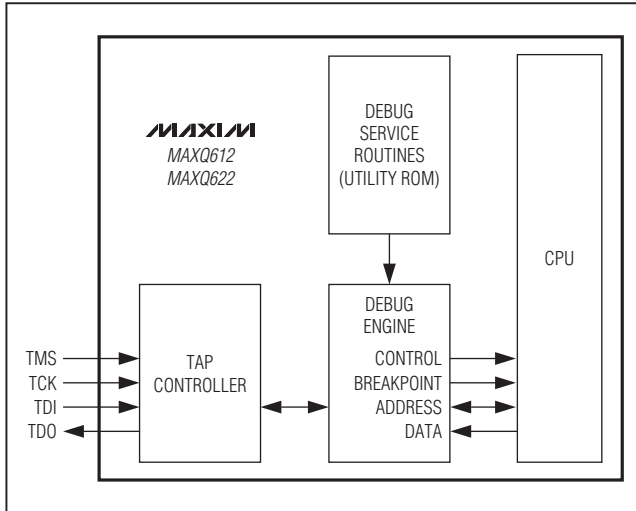


Figure 4. In-Circuit Debugger

master that can either be automatic test equipment or a component that interfaces to a higher level test bus as part of a complete system. The communication operates across a 4-wire serial interface from a dedicated TAP that is compatible with the JTAG IEEE Standard 1149. The TAP provides an independent serial channel to communicate synchronously with the host system.

To prevent unauthorized access of the protected memory regions through the JTAG interface, the debug engine prevents modification of the privilege registers and disallows all access to system memory, unless memory protection is disabled. In addition, all services (such as register display or modification) are denied when code is executing inside the system area.

Operating Modes

Power-Supply Selection

For maximum flexibility the microcontroller can be powered by either the USB (VBUS) or VDD. When a USB connection is made to a valid VBUS power source, an internal voltage regulator generates a 3.3V supply voltage. When the internal voltage is at an adequate level, it automatically powers itself from the USB supply. This is especially beneficial in systems where the VDD supply is from a battery. In either case, the chip is fully functional when operating from either the battery or the VBUS.

The power monitor is attached to the switched supply, VDDIO. This supply is equivalent to the higher of VDDDB or VDD. This can be expressed as follows:

$$\text{If } (V_{DDDB} > 3.0V \text{ or } V_{DDDB} > V_{DD})$$

then ($V_{DDIO} = V_{DDDB}$)

else ($V_{DDIO} = V_{DD}$)

This means that if there is a power-fail event on VDD and the device is not powered from VBUS, it causes a power-fail interrupt (PFI) if enabled. If the device is powered by VBUS and there is a supply on VDD, then no power-fail event is triggered. If the device is powered by VBUS and there is no supply on VDD and VBUS fails, the chip attempts to switch to VDD, detects a power-fail event, and a PFI occurs. Some specific examples are given below:

- **Case 1: The device is powered from VDD and the batteries are removed.** Power decays until the power-fail-reset trip point is hit, then the part goes into low-power mode.
- **Case 2: The device is set to be powered from VDD only, it is connected to USB, and the batteries are removed.** Response is identical to Case 1.
- **Case 3: The device is set to be powered from either VDD or VBUS, it is connected to USB, and the batteries are removed.** Because the part is already powered from VBUS, nothing changes. If the USB port is subsequently disconnected, power switches over to VDD, the supply decays to the power-fail-reset trip point, and the part goes into low-power mode. As long as there is sufficient charge on the VDD bypass capacitor, it supports the part in power-fail. The hold-up time is similar to the MAXQ610 since the USB port is powered only by VBUS. Note that if the part is powered from VBUS and no battery has been present for a long time ($V_{DD} = 0$), then upon USB port disconnection, the power collapses to ground in less than a second.

Stop Mode

The lowest power mode of operation is stop mode. In this mode, CPU state and memories are preserved, but the CPU is not actively running. Wake-up sources include external I/O interrupts, the power-fail warning interrupt, wake-up timer, or a power-fail reset. Any time the microcontroller is in a state where code does not need to be executed, the user software can put the microcontroller into stop mode. The nanopower ring oscillator is an internal ultra-low-power (400nA) 8kHz ring oscillator that can be used to drive a wake-up timer that exits stop mode. The wake-up timer is programmable by software in steps of 125μs up to approximately 8s.

The power-fail monitor is always on during normal operation. However, it can be selectively disabled during stop

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Table 4. Power-Fail Warning Level Selection

PWCN.PFWARNCN[1:0]	PFW THRESHOLD (V)
00	1.8
01	1.9
10	2.55
11	2.75

mode to minimize power consumption. This feature is enabled using the power-fail monitor disable (PFD) bit in the PWCN register. The reset default state for the PFD bit is 1, which disables the power-fail monitor function during stop mode. If power-fail monitoring is disabled (PFD = 1) during stop mode, the circuitry responsible for generating a power-fail warning or reset is shut down and neither condition is detected. Thus, the $V_{DD} < V_{RST}$ condition does not invoke a reset state. However, in the event that V_{DD} falls below the POR level, a POR is generated. The power-fail monitor is enabled prior to stop mode exit and before code execution begins. If a power-fail warning condition ($V_{DD} < V_{PFW}$) is then detected, the power-fail interrupt flag is set on stop mode exit. If a power-fail reset condition is detected ($V_{DD} < V_{RST}$), the CPU goes into reset.

Power-Fail Warning

The power-fail monitor can assert an interrupt if the voltage falls below a configurable threshold between the operating voltage and the reset voltage. This, if enabled, can allow the firmware to perform housekeeping tasks if the voltage level decays below the warning threshold. The power-fail threshold value should only be changed when the power-fail warning interrupt is disabled (CKCN.PFIE = 0) to prevent unintended triggering of the power-fail warning condition.

The power-fail warning threshold is reset to 1.8V by a POR and is not affected by other resets. See Table 4.

Power-Fail Detection

Figures 5, 6, and 7 show the power-fail detection and response during normal and stop-mode operation.

If a reset is caused by a power-fail, the power-fail monitor can be set to one of the following intervals:

- Always on—continuous monitoring
- 2^{11} nanopower ring oscillator clocks (~256ms)
- 2^{12} nanopower ring oscillator clocks (~512ms)
- 2^{13} nanopower ring oscillator clocks (~1.024s)

In the case where the power-fail circuitry is periodically turned on, the power-fail detection is turned on for two

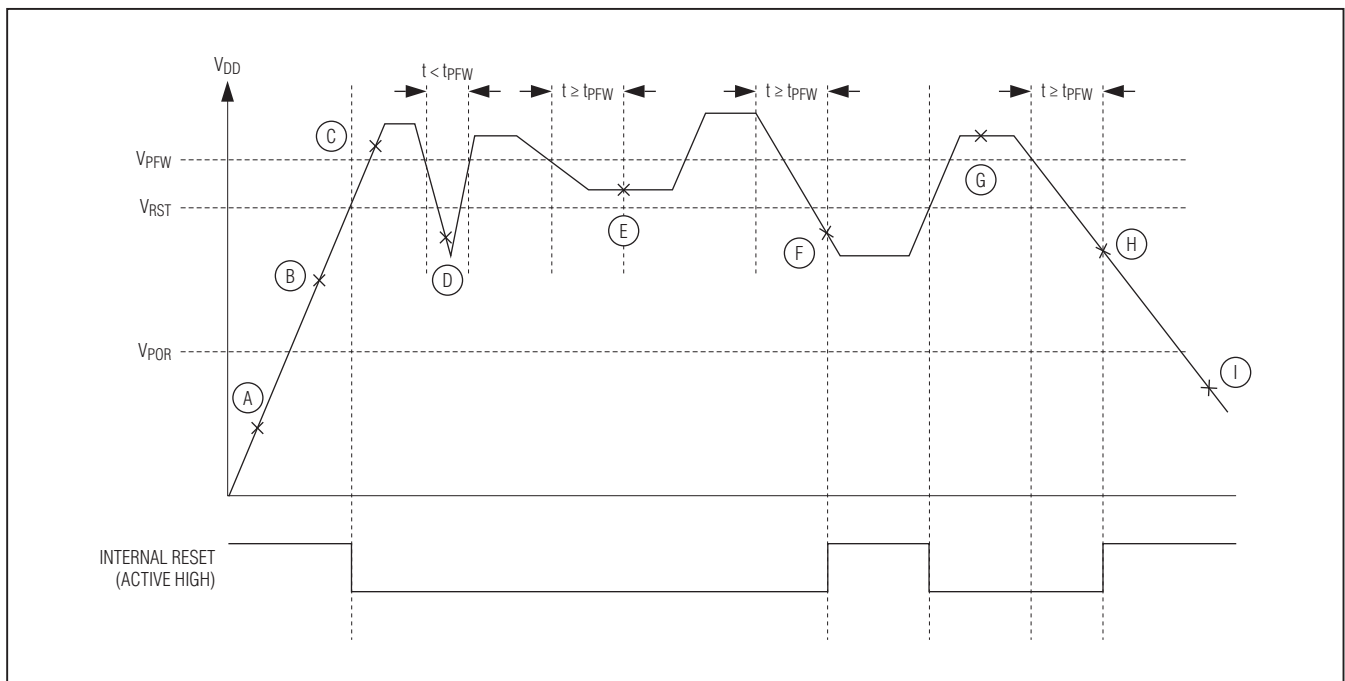


Figure 5. Power-Fail Detection During Normal Operation

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Table 5. Power-Fail Detection States During Normal Operation

STATE	POWER-FAIL	INTERNAL REGULATOR	CRYSTAL OSCILLATOR	SRAM RETENTION	COMMENTS
A	On	Off	Off	—	$V_{DD} < V_{POR}$.
B	On	On	On	—	$V_{POR} < V_{DD} < V_{RST}$. Crystal warmup time, t_{XTAL_RDY} . CPU held in reset.
C	On	On	On	—	$V_{DD} > V_{RST}$. CPU normal operation.
D	On	On	On	—	Power drop too short. Power-fail not detected.
E	On	On	On	—	$V_{RST} < V_{DD} < V_{PFW}$. PFI is set when $V_{RST} < V_{DD} < V_{PFW}$ and maintains this state for at least t_{PFW} , at which time a power-fail interrupt is generated (if enabled). CPU continues normal operation.
F	On (Periodically)	Off	Off	Yes	$V_{POR} < V_{DD} < V_{RST}$. Power-fail detected. CPU goes into reset. Power-fail monitor turns on periodically.
G	On	On	On	—	$V_{DD} > V_{RST}$. Crystal warmup time, t_{XTAL_RDY} . CPU resumes normal operation from 8000h.
H	On (Periodically)	Off	Off	Yes	$V_{POR} < V_{DD} < V_{RST}$. Power-fail detected. CPU goes into reset. Power-fail monitor turns on periodically.
I	Off	Off	Off	—	$V_{DD} < V_{POR}$. Device held in reset. No operation allowed.

nanopower ring-oscillator cycles. If $V_{DD} > V_{RST}$ during detection, V_{DD} is monitored for an additional nanopower ring-oscillator period. If V_{DD} remains above V_{RST} for the third nanopower ring period, the CPU exits the reset state and resumes normal operation from utility ROM at 8000h after satisfying the crystal warmup period.

If a reset is generated by any other event, such as the $\overline{\text{RESET}}$ pin being driven low externally or the watchdog timer, the power-fail, internal regulator, and crystal remain on during the CPU reset. In these cases, the CPU exits the reset state in less than 20 crystal cycles after the reset source is removed.

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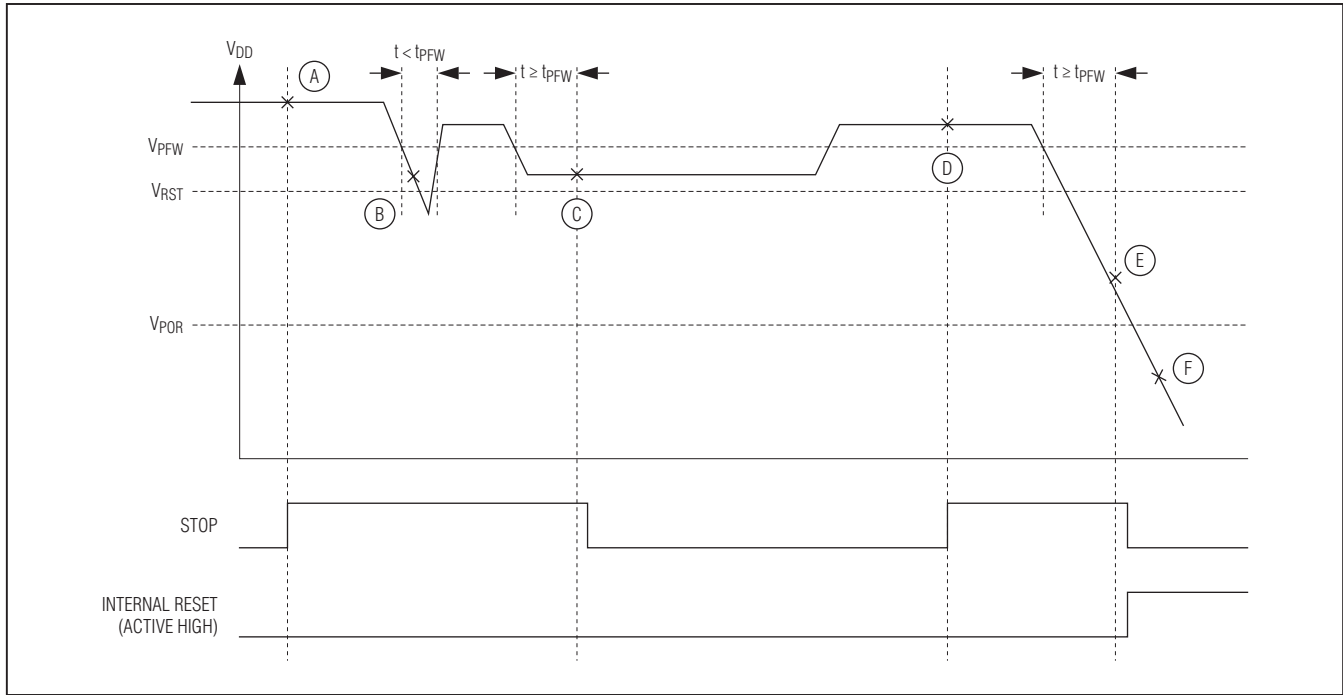


Figure 6. Stop Mode Power-Fail Detection States with Power-Fail Monitor Enabled

Table 6. Stop Mode Power-Fail Detection States with Power-Fail Monitor Enabled

STATE	POWER-FAIL	INTERNAL REGULATOR	CRYSTAL OSCILLATOR	SRAM RETENTION	COMMENTS
A	On	Off	Off	Yes	Application enters stop mode. VDD > VRST. CPU in stop mode.
B	On	Off	Off	Yes	Power drop too short. Power-fail not detected.
C	On	On	On	Yes	VRST < VDD < VPFW. Power-fail warning detected. Turn on regulator and crystal. Crystal warmup time, tXTAL_RDY. Exit stop mode.
D	On	Off	Off	Yes	Application enters stop mode. VDD > VRST. CPU in stop mode.
E	On (Periodically)	Off	Off	Yes	VPOR < VDD < VRST. Power-fail detected. CPU goes into reset. Power-fail monitor turns on periodically.
F	Off	Off	Off	—	VDD < VPOR. Device held in reset. No operation allowed.

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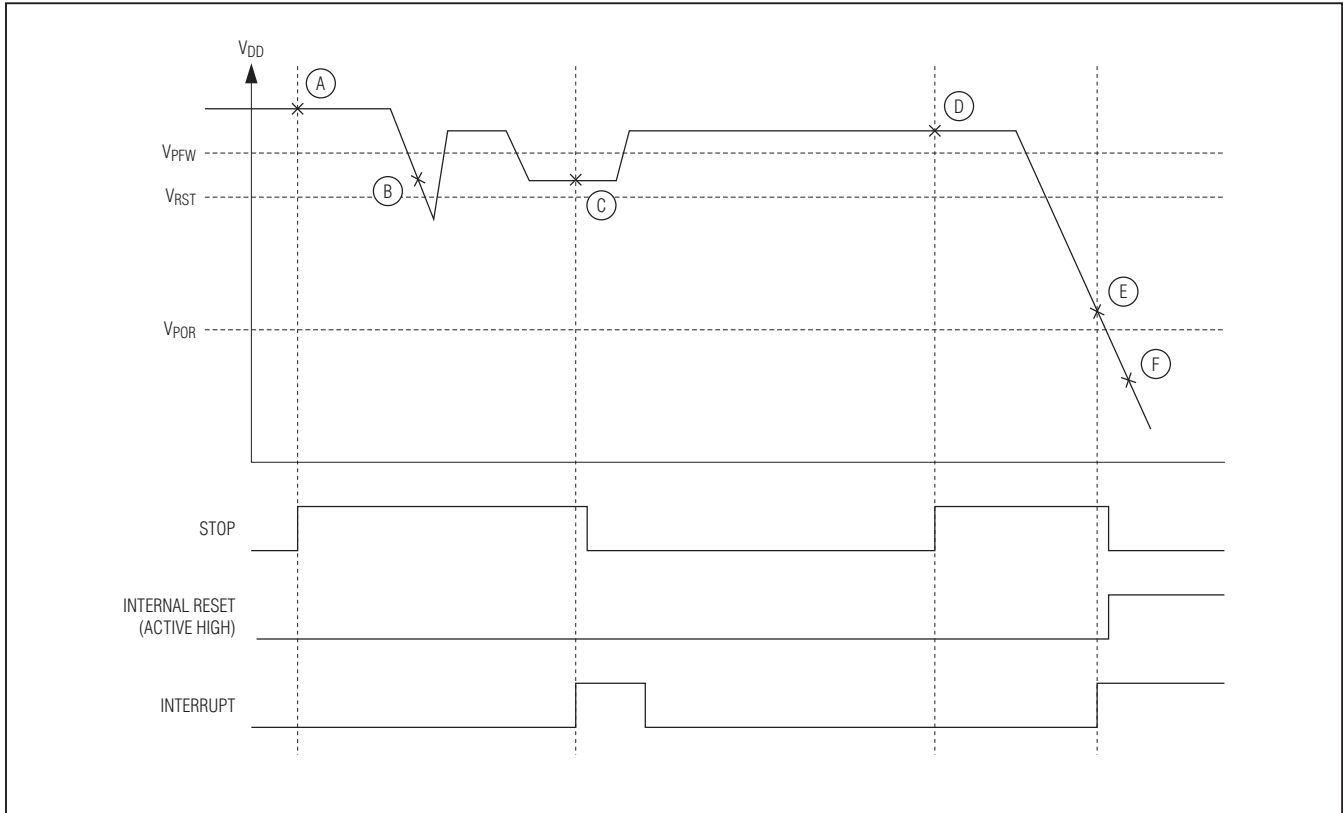


Figure 7. Stop Mode Power-Fail Detection with Power-Fail Monitor Disabled

Table 7. Stop Mode Power-Fail Detection States with Power-Fail Monitor Disabled

STATE	POWER-FAIL	INTERNAL REGULATOR	CRYSTAL OSCILLATOR	SRAM RETENTION	COMMENTS
A	Off	Off	Off	Yes	Application enters stop mode. $V_{DD} > V_{RST}$. CPU in stop mode.
B	Off	Off	Off	Yes	$V_{DD} < V_{PFW}$. Power-fail not detected because power-fail monitor is disabled.
C	On	On	On	Yes	$V_{RST} < V_{DD} < V_{PFW}$. An interrupt occurs that causes the CPU to exit stop mode. Power-fail monitor is turned on, detects a power-fail warning, and sets the power-fail interrupt flag. Turn on regulator and crystal. Crystal warmup time, t_{XTAL_RDY} . On stop mode exit, CPU vectors to the higher priority of power-fail and the interrupt that causes stop mode exit.

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Table 7. Stop Mode Power-Fail Detection States with Power-Fail Monitor Disabled (continued)

STATE	POWER-FAIL	INTERNAL REGULATOR	CRYSTAL OSCILLATOR	SRAM RETENTION	COMMENTS
D	Off	Off	Off	Yes	Application enters stop mode. $V_{DD} > V_{RST}$. CPU in stop mode.
E	On (Periodically)	Off	Off	Yes	$V_{POR} < V_{DD} < V_{RST}$. An interrupt occurs that causes the CPU to exit stop mode. Power-fail monitor is turned on, detects a power-fail, and puts CPU in reset. Power-fail monitor is turned on periodically.
F	Off	Off	Off	—	$V_{DD} < V_{POR}$. Device held in reset. No operation allowed.

Applications Information

The low-power, high-performance RISC architecture of this device makes it an excellent fit for many portable or battery-powered applications. It is ideally suited for applications such as universal remote controls that require the cost-effective integration of IR transmit/receive capability.

Grounds and Bypassing

Careful PCB layout significantly minimizes system-level digital noise that could interact with the microcontroller or peripheral components. The use of multilayer boards is essential to allow the use of dedicated power planes. The area under any digital components should be a continuous ground plane if possible. Keep bypass capacitor leads short for best noise rejection and place the capacitors as close to the leads of the devices as possible.

CMOS design guidelines for any semiconductor require that no pin be taken above V_{DD} or below GND. Violation of this guideline can result in a hard failure (damage to the silicon inside the device) or a soft failure (unintentional modification of memory contents). Voltage spikes above or below the device's absolute maximum ratings can potentially cause a devastating IC latchup.

Microcontrollers commonly experience negative voltage spikes through either their power pins or general-

purpose I/O pins. Negative voltage spikes on power pins are especially problematic as they directly couple to the internal power buses. Devices such as keypads can conduct electrostatic discharges directly into the microcontroller and seriously damage the device. System designers must protect components against these transients that can corrupt system memory.

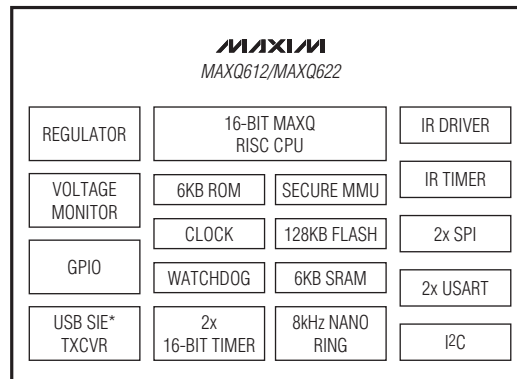
Additional Documentation

Designers must have the following documents to fully use all the features of this device. This data sheet contains pin descriptions, feature overviews, and electrical specifications. Errata sheets contain deviations from published specifications. The user's guides offer detailed information about device features and operation. The following documents can be downloaded from www.maxim-ic.com/microcontrollers.

- This MAXQ612/MAXQ622 data sheet, which contains electrical/timing specifications and pin descriptions.
- The MAXQ612/MAXQ622 revision-specific errata sheet (www.maxim-ic.com/errata).
- The *MAXQ622 User's Guide*, which contains detailed information on features and operation, including programming.

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Block Diagram



*MAXQ622 ONLY.

Development and Technical Support

Maxim and third-party suppliers provide a variety of highly versatile, affordably priced development tools for this microcontroller, including the following:

- Compilers
- In-circuit emulators
- Integrated Development Environments (IDEs)
- JTAG-to-serial converters for programming and debugging

A partial list of development tool vendors can be found at www.maxim-ic.com/MAXQ_tools.

For technical support, go to <https://support.maxim-ic.com/micro>.

Package Information

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
64 LQFP	C64+5	21-0083
44 TQFN-EP	T4477+2	21-0144

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