![Wolfson microelectronics logo]

WM5100

Low Power Audio System with Wolfson myZone™ Ambient Noise Cancellation and Echo Cancellation

DESCRIPTION

The WM5100 is a highly-integrated low-power audio system with exceptional levels of performance and signal processing capability. Digital effects, noise reduction, speech clarity and Ambient Noise Cancellation (ANC) algorithms are all supported, suitable for a wide variety of mobile and handheld devices.

The Wolfson myZone™ technology supports receive (RX) path and transmit (TX) path noise cancellation. Acoustic Echo Cancellation (AEC) algorithms are also supported. The WM5100 is ideal for mobile telephony applications, providing enhanced voice communication quality for near-end and far-end handset users.

The WM5100 digital core provides extensive capability for programmable signal processing algorithms. Equalisation and application-specific filters can be implemented, including digital effects to improve audibility and stereo imaging in small size loudspeakers. Highly flexible digital mixing, including multi-channel sample rate conversion between asynchronous clocking domains, provides use-case flexibility across a broad range of system architectures. Three independent digital audio interfaces are provided, each supporting a wide range of standard audio sample rates.

The integrated headphone drivers provide 3 stereo ground-referenced outputs. These can also be configured in mono differential (BTL) configuration. Noise levels as low as $3.2\mu V_{RMS}$ provide hi-fi quality output. Speakerphone applications can be supported using the Class D speaker driver or the integrated digital speaker (PDM) interface with an external PDM-input speaker amplifier.

The WM5100 supports up to eight analogue or digital microphone inputs. The Wolfson myZone™ ANC processor implements an enhanced filtering algorithm to consistently deliver the optimum noise cancellation performance using two or more microphone input channels. A smart digital microphone interface provides power regulation, low jitter clock output and decimation filters for digital microphones.

Microphone activity detection with interrupt is available. Impedance sensing and measurement is provided for external accessory and push-button detection.

The WM5100 is powered from a 1.8V external supply. A supply is also required for the Class D speaker drivers (typically 4.2V). Two integrated FLLs provide support for a wide range of system clock frequencies. The WM5100 is configured using a standard 2-wire serial control interface. Fully differential internal architecture and on-chip RF noise filters ensure a very high degree of noise immunity.
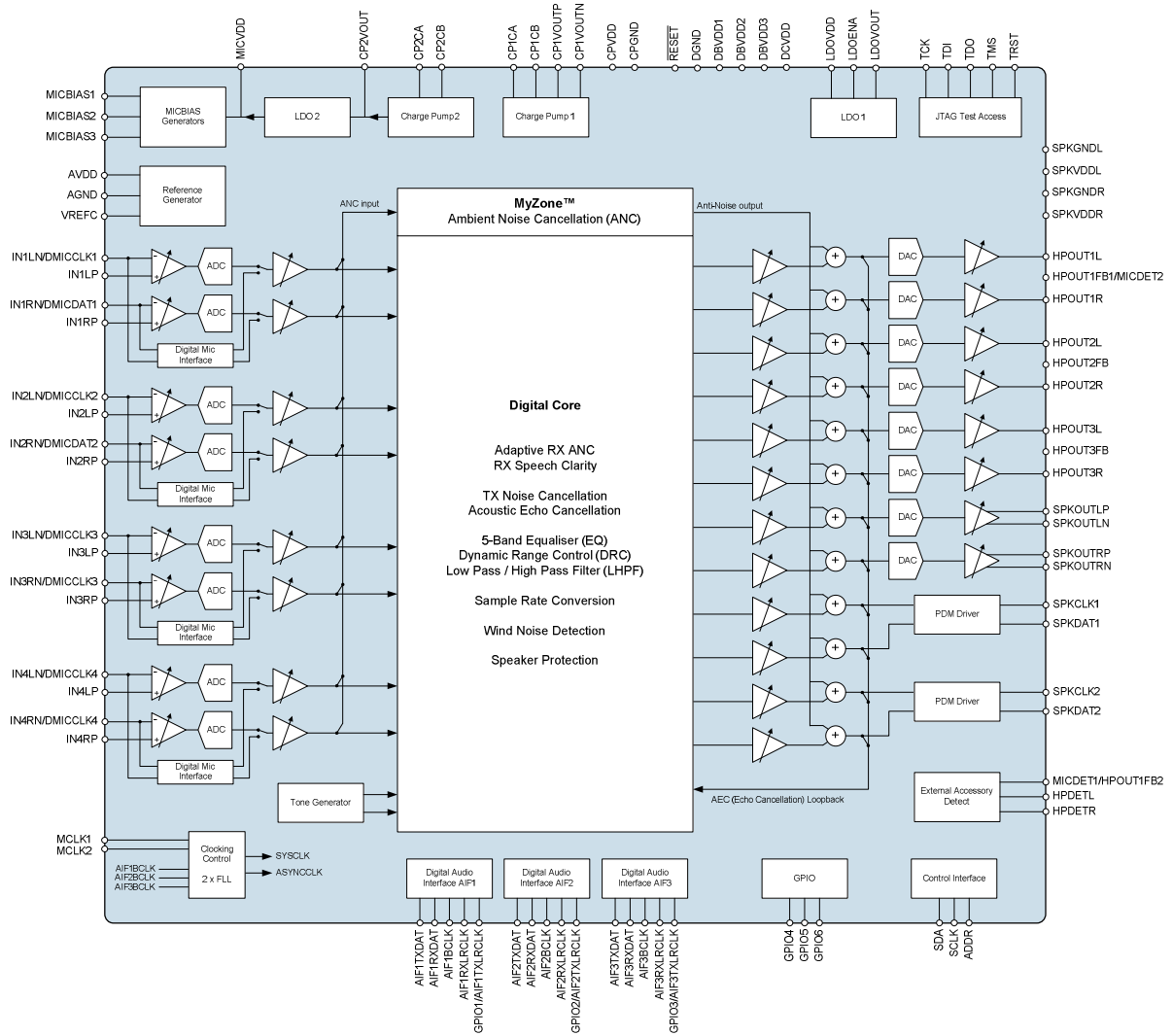
FEATURES

- Programmable DSP and Noise Cancellation functions
  - Wolfson myZone™ adaptive ambient noise cancellation
  - Transmit-path noise reduction and echo cancellation
  - Wind noise, sidetone and other programmable filters
  - Audio enhancements and voice processing functions
- Audio inputs
  - Up to 8 analogue or digital microphone inputs
  - Single-ended or differential analogue microphone input
  - Line input support (single-ended or differential)
- Multi-purpose headphone / earpiece / line output drivers
  - 3 stereo output paths
  - Integrated Charge Pump for ground referenced output
  - Mono differential (BTL) drive option on each output
  - Pop suppression functions
  - 30mW into 32Ω load at 1% THD+N
  - $3.2\mu V_{RMS}$ noise floor (A-weighted)
  - 4mW headphone playback power consumption
- 2 x 2W stereo Class D speaker output drivers
- Four-channel digital speaker (PDM) interface
- 3 full digital audio interfaces
  - Standard sample rates from 4kHz up to 768kHz
  - Ultrasonic accessory function support
  - TDM support on all AIFs
  - 8 channel input and output on AIF1
- Multi-channel sample rate conversion
  - Allows digital audio to be routed between different sample rates and between different clock reference domains
- Flexible system clocking
  - External clocking from 2 MCLK inputs or AIF BCLK
  - Dual FLLs support wide range of input clock reference frequencies, including down to 32kHz
- Configurable functions on 6 GPIO pins
- Advanced accessory detection functions
  - Up to 6 push-button accessory inputs
  - 'Switchable ground' support for different headset types
- Integrated power management
  - Two Charge Pumps and 2 LDO Regulators
  - Support for single 1.8V supply operation
- 155-ball W-CSP package
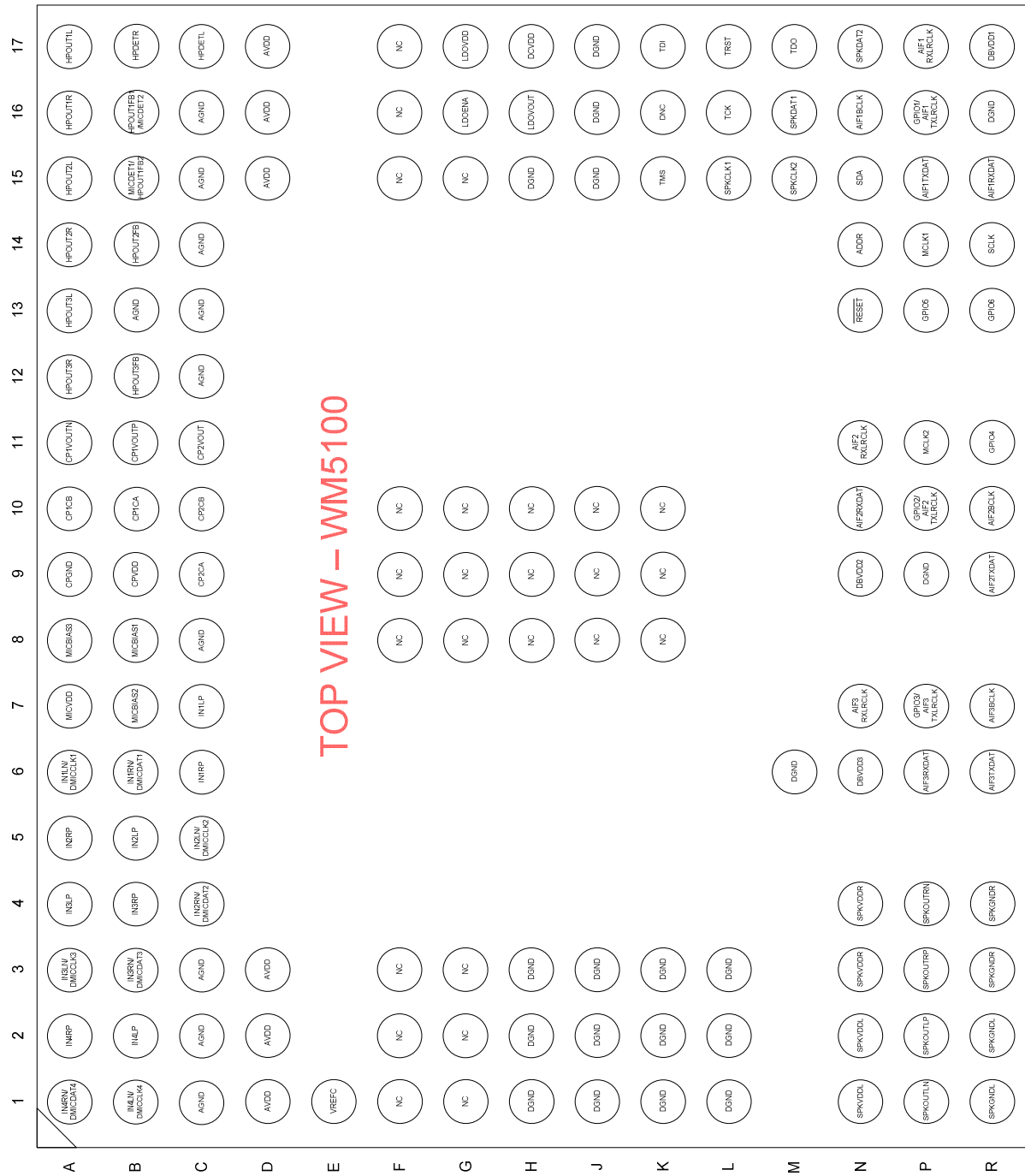 - 7.259 x 6.190 x 0.553mm, 0.4mm pitch

APPLICATIONS

- Smartphones
- Feature phones
- Tablets
- Portable Media Players (PMP)

BLOCK DIAGRAM

PIN CONFIGURATION

TOP VIEW – WM5100

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R
17	HPOUT1L	HPDETR	HPDETL	AVDD		NC	LDOVDD	DCVDD	DGND	TDI	TRST	TDO	SPKDAT2	AIF1 RXLRCLK	DBVDD1
16	HPOUT1R	HPOUT1FB/MICDET2	AGND	AVDD		NC	LDOENA	LDOVOUT	DGND	DNC	TCK	SPKDAT1	AIF1BCLK	GPIO1/AIF1 TXLRCLK	DGND
15	HPOUT2L	MICDET1/HPOUT1FB2	AGND	AVDD		NC	NC	DGND	DGND	TMS	SPKCLK1	SPKCLK2	SDA	AIF1TXDAT	AIF1RXDAT
14	HPOUT2R	HPOUT2FB	AGND										ADDR	MCLK1	SCLK
13	HPOUT3L	AGND	AGND										RESET	GPIO5	GPIO6
12	HPOUT3R	HPOUT3FB	AGND										AIF2 RXLRCLK	MCLK2	GPIO4
11	CP1VOUTN	CP1VOUTP	CP2VOUT										AIF2RXDAT	GPIO2/AIF2 TXLRCLK	AIF2BCLK
10	CP1CB	CP1CA	CP2CB			NC	NC	NC	NC	NC			AIF2RXDAT2	GPIO2/AIF2 TXLRCLK	AIF2BCLK
9	CPGND	CPVDD	CP2CA			NC	NC	NC	NC	NC			DBVDD2	DGND	AIF2TXDAT
8	MICBIAS3	MICBIAS1	AGND			NC	NC	NC	NC	NC					
7	MICVDD	MICBIAS2	IN1LP										AIF3 RXLRCLK	GPIO3/AIF3 TXLRCLK	AIF3BCLK
6	IN1LN/DMICCLK1	IN1RN/DMICDAT1	IN1RP									DGND	DBVDD3	AIF3RXDAT	AIF3TXDAT
5	IN3RP	IN2LP	IN2LN/DMICCLK2												
4	IN3LP	IN3RP	IN2RN/DMICDAT2										SPKVDDR	SPKOUTRN	SPKGNDR
3	IN3LN/DMICCLK3	IN3RN/DMICDAT3	AGND	AVDD		NC	NC	DGND	DGND	DGND	DGND		SPKVDDR	SPKOUTRP	SPKGNDR
2	IN4RP	IN4LP	AGND	AVDD		NC	NC	DGND	DGND	DGND	DGND		SPKVDDL	SPKOUTLP	SPKGNDL
1	IN4RN/DMICDAT4	IN4LN/DMICCLK4	AGND	AVDD	VREFC	NC	NC	DGND	DGND	DGND	DGND		SPKVDDL	SPKOUTLN	SPKGNDL

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ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM5100ECS/R	-40°C to +85°C	155-ball W-CSP (Pb-free, Tape and reel)	MSL1	260°C

Note:

Reel quantity = TBC

PIN DESCRIPTION

A description of each pin on the WM5100 is provided below.

Note that, where multiple pins share a common name, these pins should be tied together on the PCB.

PIN NO	NAME	TYPE	DESCRIPTION
N14	ADDR	Digital Input	2-wire (I2C) address select
C1, C2, C3, B13, C8, C12, C13, C14, C15, C16	AGND	Supply	Analogue ground (Return path for AVDD)
N16	AIF1BCLK	Digital Input / Output	Audio interface 1 bit clock
R15	AIF1RXDAT	Digital Input	Audio interface 1 RX digital audio data
P17	AIF1RXLRCLK	Digital Input / Output	Audio interface 1 RX left / right clock
P15	AIF1TXDAT	Digital Output	Audio interface 1 TX digital audio data
R10	AIF2BCLK	Digital Input / Output	Audio interface 2 bit clock
N10	AIF2RXDAT	Digital Input	Audio interface 2 RX digital audio data
N11	AIF2RXLRCLK	Digital Input / Output	Audio interface 2 RX left / right clock
R9	AIF2TXDAT	Digital Output	Audio interface 2 TX digital audio data
R7	AIF3BCLK	Digital Input / Output	Audio interface 3 bit clock
P6	AIF3RXDAT	Digital Input	Audio interface 3 RXdigital audio data
N7	AIF3RXLRCLK	Digital Input / Output	Audio interface 3 RX left / right clock
R6	AIF3TXDAT	Digital Output	Audio interface 3 TX digital audio data
D1, D2, D3, D15, D16, D17	AVDD	Supply	Analogue supply
B10	CP1CA	Analogue Output	Charge pump 1 fly-back capacitor pin
A10	CP1CB	Analogue Output	Charge pump 1 fly-back capacitor pin
A9	CPGND	Supply	Charge pump 1 & 2ground (Return path for CPVDD)
B9	CPVDD	Supply	Supply for Charge Pump 1 & 2
A11	CP1VOUTN	Analogue Output	Charge pump 1 negative output decoupling pin
B11	CP1VOUTP	Analogue Output	Charge pump 1 positive output decoupling pin
C9	CP2CA	Analogue Output	Charge pump 2 fly-back capacitor pin
C10	CP2CB	Analogue Output	Charge pump 2 fly-back capacitor pin
C11	CP2VOUT	Analogue Output	Charge pump 2 output decoupling pin / Supply for LDO2
R17	DBVDD1	Supply	Digital buffer (I/O) supply (core functions and Audio Interface 1)
N9	DBVDD2	Supply	Digital buffer (I/O) supply (for Audio Interface 2)
N6	DBVDD3	Supply	Digital buffer (I/O) supply (for Audio Interface 3)
H17	DCVDD	Supply	Digital core supply
H1, H2, H3, J1, J2, J3, K1, K2, K3, L1, L2, L3, M6, P9, H15, J15, J16, J17, R16	DGND	Supply	Digital ground (Return path for DCVDD, DBVDD1, DBVDD2 and DBVDD3)

PIN NO	NAME	TYPE	DESCRIPTION
P16	GPIO1/ AIF1TXLRCLK	Digital Input / Output	General Purpose pin GPIO1 / Audio interface 1 TX left / right clock
P10	GPIO2/ AIF2TXLRCLK	Digital Input / Output	General Purpose pin GPIO2 / Audio interface 2 TX left / right clock
P7	GPIO3/ AIF3TXLRCLK	Digital Input / Output	General Purpose pin GPIO3 / Audio interface 3 TX left / right clock
R11	GPIO4	Digital Input / Output	General Purpose pin GPIO4
P13	GPIO5	Digital Input / Output	General Purpose pin GPIO5
R13	GPIO6	Digital Input / Output	General Purpose pin GPIO6
C17	HPDETL	Analogue Input / Output	Headphone left (HPOUT1L) sense input
B17	HPDETR	Analogue Input / Output	Headphone right (HPOUT1R) sense input
B16	HPOUT1FB1/ MICDET2	Analogue Input	HPOUT1L and HPOUT1R ground feedback pin 1/ Microphone & accessory sense input 2
A17	HPOUT1L	Analogue Output	Left headphone 1 output
A16	HPOUT1R	Analogue Output	Right headphone 1 output
B14	HPOUT2FB	Analogue Input	HPOUT2L and HPOUT2R ground loop noise rejection feedback
A15	HPOUT2L	Analogue Output	Left headphone 2 output
A14	HPOUT2R	Analogue Output	Right headphone 2 output
B12	HPOUT3FB	Analogue Input	HPOUT3L and HPOUT3R ground loop noise rejection feedback
A13	HPOUT3L	Analogue Output	Left headphone 3 output
A12	HPOUT3R	Analogue Output	Right headphone 3 output
A6	IN1LN/ DMICCLK1	Analogue Input / Digital Output	Left channel single-ended MIC input / Left channel negative differential MIC input / Digital MIC clock output 1
C7	IN1LP	Analogue Input	Left channel line input / Left channel positive differential MIC input
B6	IN1RN/ DMICDAT1	Analogue input / Digital Input	Right channel single-ended MIC input / Right channel negative differential MIC input / Digital MIC data input 1
C6	IN1RP	Analogue Input	Right channel line input / Right channel positive differential MIC input
C5	IN2LN/ DMICCLK2	Analogue Input / Digital Output	Left channel single-ended MIC input / Left channel negative differential MIC input / Digital MIC clock output 2
B5	IN2LP	Analogue Input	Left channel line input / Left channel positive differential MIC input
C4	IN2RN/ DMICDAT2	Analogue input / Digital Input	Right channel single-ended MIC input / Right channel negative differential MIC input / Digital MIC data input 2
A5	IN2RP	Analogue Input	Right channel line input / Right channel positive differential MIC input
A3	IN3LN/ DMICCLK3	Analogue Input / Digital Output	Left channel single-ended MIC input / Left channel negative differential MIC input / Digital MIC clock output 3
A4	IN3LP	Analogue Input	Left channel line input / Left channel positive differential MIC input
B3	IN3RN/ DMICDAT3	Analogue input / Digital Input	Right channel single-ended MIC input / Right channel negative differential MIC input / Digital MIC data input 3
B4	IN3RP	Analogue Input	Right channel line input / Right channel positive differential MIC input
B1	IN4LN/ DMICCLK4	Analogue Input / Digital Output	Left channel single-ended MIC input / Left channel negative differential MIC input / Digital MIC clock output 4

PIN NO	NAME	TYPE	DESCRIPTION
B2	IN4LP	Analogue Input	Left channel line input / Left channel positive differential MIC input
A1	IN4RN/ DMICDAT4	Analogue input / Digital Input	Right channel single-ended MIC input / Right channel negative differential MIC input / Digital MIC data input 4
A2	IN4RP	Analogue Input	Right channel line input / Right channel positive differential MIC input
G16	LDOENA	Digital Input	Enable pin for LDO1
G17	LDOVDD	Supply	Supply for LDO1
H16	LDOVOUT	Analogue Output	LDO1 output
P14	MCLK1	Digital Input	Master clock 1
P11	MCLK2	Digital Input	Master clock 2
B8	MICBIAS1	Analogue Output	Microphone bias 1
B7	MICBIAS2	Analogue Output	Microphone bias 2
A8	MICBIAS3	Analogue Output	Microphone bias 3
B15	MICDET1/ HPOUT1FB2	Analogue Input	Microphone & accessory sense input 1/ HPOUT1L and HPOUT1R ground feedback pin 2
A7	MICVDD	Analogue Output	LDO2 output decoupling pin (generated internally by WM5100)
N13	RESET	Digital Input	Digital Reset input (active low)
R14	SCLK	Digital Input	Control interface clock input
N15	SDA	Digital Input / Output	Control interface data input and output / acknowledge output
L15	SPKCLK1	Digital Output	Digital speaker (PDM) 1 clock output
M15	SPKCLK2	Digital Output	Digital speaker (PDM) 2 clock output
M16	SPKDAT1	Digital Output	Digital speaker (PDM) 1 data output
N17	SPKDAT2	Digital Output	Digital speaker (PDM) 2 data output
R1, R2	SPKGNDL	Supply	Ground for Left speaker driver (Return path for SPKVDDL)
R3, R4	SPKGNDR	Supply	Ground for Right speaker driver (Return path for SPKVDDR)
P1	SPKOUTLN	Analogue Output	Left speaker negative output
P2	SPKOUTLP	Analogue Output	Left speaker positive output
P4	SPKOUTRN	Analogue Output	Right speaker negative output
P3	SPKOUTRP	Analogue Output	Right speaker positive output
N1, N2	SPKVDDL	Supply	Supply for Left speaker driver
N3, N4	SPKVDDR	Supply	Supply for Right speaker driver
L16	TCK	Digital Input	JTAG clock input
K17	TDI	Digital Input	JTAG data input
M17	TDO	Digital Output	JTAG data output
K15	TMS	Digital Input	JTAG mode select input
L17	TRST	Digital Input	JTAG Test Access Port reset input (active low, internal pull-down). This input should be logic 0 for normal WM5100 operation.
E1	VREFC	Analogue Output	Bandgap reference decoupling capacitor connection
K16	DNC	n/a	Do Not Connect
F1, F2, F3, G1, G2, G3, F8, F9, F10, G8, G9, G10, H8, H9, H10, J8, J9, J10, K8, K9, K10, F15, F16, F17, G15	NC	n/a	No Connection

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltages (DBVDD1, DBVDD2, DBVDD3)	-0.3V	+4.5V
Supply voltages (LDOVDD, AVDD, DCVDD)	-0.3V	+2.5V
Supply voltages (CPVDD)	-0.3V	+2.2V
Supply voltages (SPKVDDL, SPKVDDR)	-0.3V	+7.0V
Voltage range digital inputs (DBVDD1 domain)	DGND -0.3V	DBVDD1 +0.3V
Voltage range digital inputs (DBVDD2 domain)	DGND -0.3V	DBVDD2 +0.3V
Voltage range digital inputs (DBVDD3 domain)	DGND -0.3V	DBVDD3 +0.3V
Voltage range analogue inputs	AGND -0.3V	MICVDD +0.25V
Operating temperature range, T_A	-40ºC	+85ºC
Operating junction temperature, T_J	-40ºC	+125ºC
Storage temperature after soldering	-65ºC	+150ºC

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital supply range (Core) See note 1	DCVDD	1.14	1.2	1.89	V
Digital supply range (I/O)	DBVDD1, DBVDD2, DBVDD3	1.71	1.8	3.6	V
LDO supply range	LDOVDD	1.71	1.8	1.89	V
Charge Pump supply range	CPVDD	1.71	1.8	1.89	V
Speaker supply range	SPKVDDL, SPKVDDR	2.7	5.0	5.5	V
Analogue supply range	AVDD	1.71	1.8	1.89	V
Ground	DGND, AGND, CPGND, SPKGNDL, SPKGNDR		0		V

Notes:

1. An internal LDO (powered by LDOVDD) can be used to provide the DCVDD supply.
2. The grounds must always be within 0.3V of each other.
3. There is no power sequencing requirement; the supplies may be enabled in any order.
4. The MICVDD pin is not a supply pin; this power domain is generated internally by the WM5100; the MICVDD pin should not be connected to an external supply.

DESCRIPTION

The WM5100 is a low power, high quality audio codec designed to interface with a wide range of processors and digital audio components. The WM5100 incorporates the Wolfson MyZone™ Ambient Noise Cancellation (ANC) and additional configurable DSP for audio enhancement algorithms. A high level of mixed-signal integration in a very small footprint makes it ideal for portable applications such as mobile phones. Fully differential internal architecture and on-chip RF noise filters ensure a very high degree of noise immunity.

The WM5100 digital core provides extensive mixing and processing capabilities for multiple signal paths. The digital core provides parametric equalisation (EQ) functions, low-pass / high-pass filters, dynamic range control (DRC) and programmable DSP capability. The DSP can support functions such as wind noise, side-tone or other programmable filters, also dynamic range control and compression, or virtual surround sound and other audio enhancements. The ADCs and DACs are of hi-fi quality, using a 24-bit low-order oversampling architecture to deliver optimum performance.

The Wolfson myZone™ Ambient Noise Cancellation (ANC) processor within the WM5100 provides the capability to improve the intelligibility of a voice call by using destructive interference to reduce the acoustic energy of the ambient sound.

Eight digital microphone input channels are available to support advanced multi-microphone applications such as noise reduction. Up to eight analogue inputs can be connected, to allow interfacing to microphones or line level audio signals. The WM5100 supports single-ended and differential analogue input connections.

Six stereo output channels are available to support a wide variety of use cases. The output signal paths comprise analogue headphone drivers, Class D loudspeaker drivers and also a four channel digital (PDM) interface suitable for external speaker drivers. All outputs have integrated pop and click suppression features.

The headphone output drivers are ground-referenced, powered from an integrated charge pump, enabling high quality, power efficient headphone playback without any requirement for DC blocking capacitors. Ground loop feedback is incorporated, providing rejection of noise on the ground connections. A mono mode is available on each of the headphone outputs; this configures the drivers as differential (BTL) outputs, suitable for an earpiece or hearing aid coil.

The WM5100 provides three audio interfaces in order to provide independent and fully asynchronous connections to multiple processors - typically an application processor, baseband processor and wireless transceiver. Each interface supports a number of protocols, including I^2S, DSP or Left Justified, and can operate in master or slave modes. PCM operation is supported in the DSP mode.

Time division multiplexing (TDM) is available to allow multiple devices to stream data simultaneously on the same bus, saving space and power. Eight-channel input and output is supported using TDM on AIF1. Two-channel input and output is supported on AIF2 and AIF3.

Signal mixing between audio interfaces is possible. The WM5100 performs stereo full-duplex sample rate conversion between the audio interfaces as required.

The audio interfaces AIF1, AIF2 and AIF3 are referenced to DBVDD1, DBVDD2 and DBVDD3 respectively; this provides additional capability to interface between different sub-systems within an application.

A flexible clocking arrangement supports a wide variety of external clock references, including clocking derived from the digital audio interface. Two integrated Frequency Locked Loop (FLL) circuits provide additional flexibility. Typical portable system MCLK frequencies, and sample rates from 4kHz to 768kHz are all supported. A low frequency (eg. 32.768kHz) clock can also be used as the input reference to the FLLs, providing further flexibility.

The WM5100 uses a standard 2-wire control interface, providing full software control of all features, together with device register readback. It is an ideal partner for a wide range of industry standard microprocessors, controllers and DSPs. Unused circuitry can be disabled under software control, in order to save power; low leakage currents enable extended standby/off time in portable battery-powered applications.

Versatile GPIO functionality is provided, with support for button/accessory detect inputs, or for clock, system status, or programmable logic level output for control of additional external circuitry. Interrupt logic and status readback are supported within this functionality.

PACKAGE DIMENSIONS

B: 155 BALL W-CSP PACKAGE 7.259 x 6.190 x 0.553mm BODY, 0.40 mm BALL PITCH   DM099.A
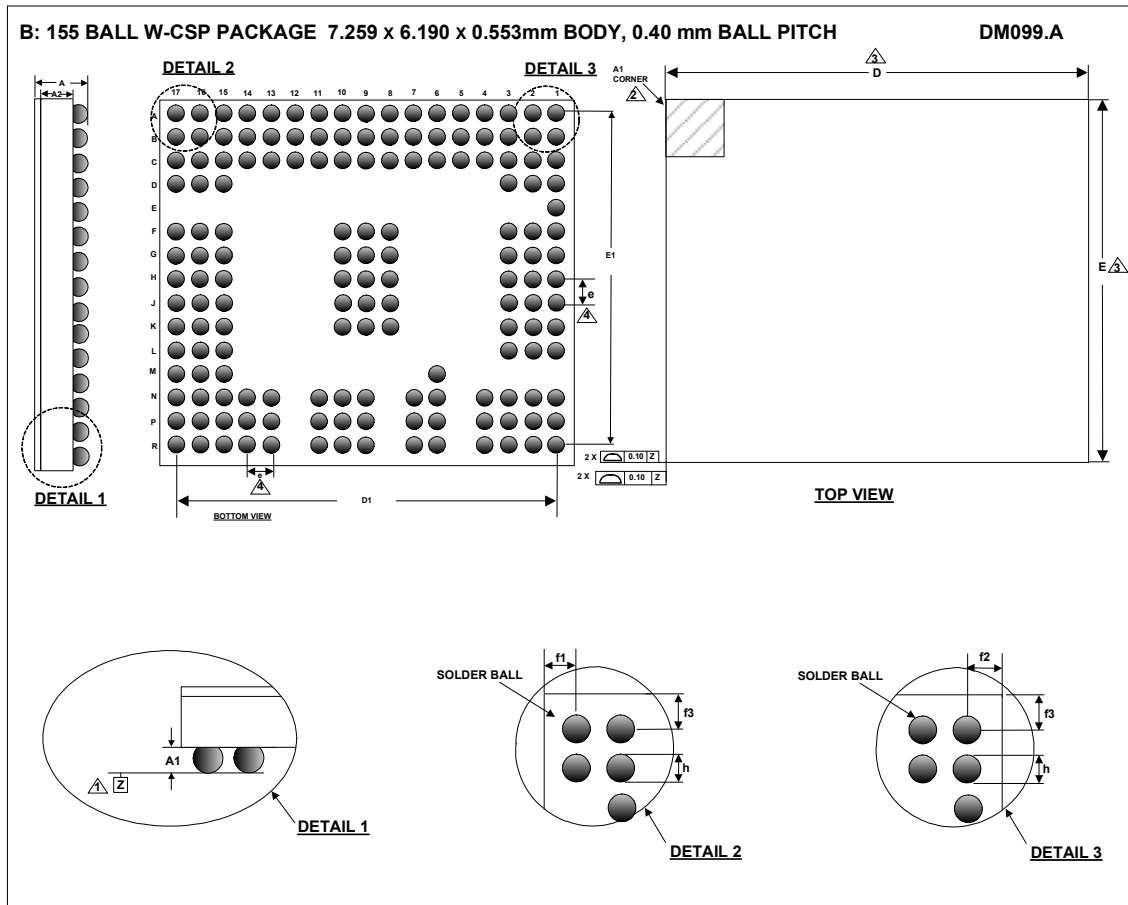
Symbols	Dimensions (mm)			
	MIN	**NOM**	**MAX**	**NOTE**
A	0.490	0.553	0.616	
A1	0.172	0.202	0.232	
A2		0.329		
D	7.214	7.259	7.304	
D1		6.400 BSC		
E	6.160	6.190	6.220	
E1		5.600 BSC		
e		0.400 BSC		4
f1	0.358			Bump centre to die edge
f2	0.456			Bump centre to die edge
f3	0.280			Bump centre to die edge
h	0.222	0.262	0.302	

NOTES:
1. PRIMARY DATUM -Z- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
2. A1 CORNER IS IDENTIFIED BY INK/LASER MARK ON TOP PACKAGE.
3. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.
4. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
5. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
6. FOLLOWS JEDEC DESIGN GUIDE MO-211-C

IMPORTANT NOTICE

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REVISION HISTORY

DATE	REV	DESCRIPTION OF CHANGES	PAGE	CHANGED BY
05/07/11	1.0	First Release		