



# Low Skew, ÷1, ÷2 LVCMOS/ LVTTTL Clock Generator w/Polarity Control

ICS8701I-01

## GENERAL DESCRIPTION



The ICS8701I-01 is a low skew, ÷1, ÷2 LVCMOS/ LVTTTL Clock Generator. The low impedance LVCMOS outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 20 to 40 by utilizing the ability of the outputs to drive two series terminated lines.

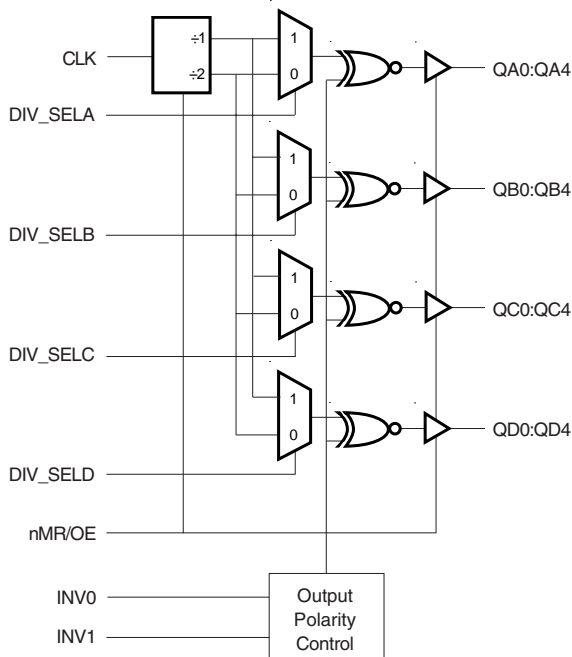
The divide select inputs, DIV\_SELx, control the output frequency of each bank. The outputs can be utilized in the ÷1, ÷2 or a combination of ÷1 and ÷2 modes. The master reset/output enable input, nMR/OE, resets the internal dividers and controls the active and high impedance states of all outputs. The output polarity inputs, INV0:1, control the polarity (inverting or non-inverting) of the outputs of each bank. Outputs QA0:QA4 are inverting for every combination of the INV0:1 input. The timing relationship between the inverting and non-inverting outputs at different frequencies is shown in the Timing Diagrams.

The ICS8701I-01 is characterized at 3.3V and mixed 3.3V input supply, and 2.5V output supply operating modes. Guaranteed bank, output and part-to-part skew characteristics make the ICS8701I-01 ideal for those clock distribution applications demanding well defined performance and repeatability.

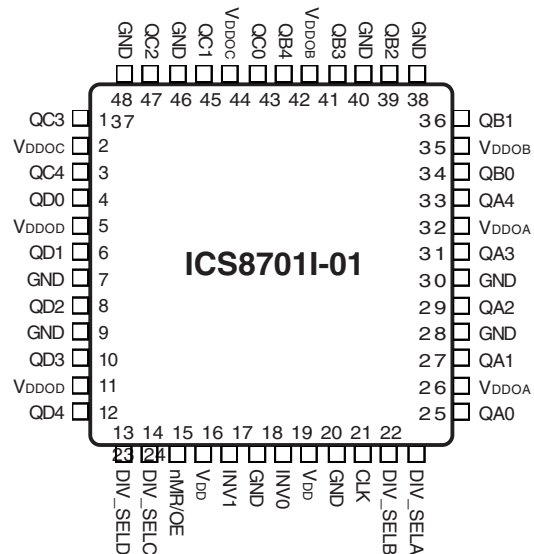
## FEATURES

- Twenty LVCMOS/LVTTTL outputs, 7Ω typical output impedance
- One LVCMOS/LVTTTL clock input
- Maximum output frequency: 250MHz
- Selectable inverting and non-inverting outputs
- Bank enable logic allows unused banks to be disabled in reduced fanout applications
- Output skew: 300ps (maximum)
- Part-to-part skew: 700ps (maximum)
- Bank skew: 250ps (maximum)
- Multiple frequency skew: 350ps (maximum)
- 3.3V or mixed 3.3V input, 2.5V output operating supply
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

## BLOCK DIAGRAM



## PIN ASSIGNMENT



**48-Pin LQFP**  
7mm x 7mm x 1.4mm package body  
**Y Package**  
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 3, 43, 45, 47	QC3, QC4, QC0, QC1, QC2	Output		Bank C outputs. LVCMOS interface levels. $7\Omega$ typical output impedance.
2, 44	$V_{DDOC}$	Power		Output Bank C supply pins.
4, 6, 8, 10, 12	QD0, QD1, QD2, QD3, QD4	Output		Bank D outputs. LVCMOS interface levels. $7\Omega$ typical output impedance.
5, 11	$V_{DDOD}$	Power		Output Bank D supply pins.
7, 9, 18, 21, 28, 30, 37, 39, 46, 48	GND	Power		Power supply ground.
13	DIV_SELD	Input	Pullup	Controls frequency division for Bank D outputs. LVCMOS interface levels.
14	DIV_SELC	Input	Pullup	Controls frequency division for Bank C outputs. LVCMOS interface levels.
15	nMR/OE	Input	Pullup	Master Reset and output enable. When HIGH, output drivers are enabled. When LOW, output drivers are in HiZ and dividers are reset. LVCMOS interface levels.
16, 20	$V_{DD}$	Power		Core supply pins.
17, 19	INV1, INV0	Input	Pullup	Determines polarity of outputs by banks. LVCMOS interface levels.
22	CLK	Input	Pullup	LVCMOS clock input.
23	DIV_SELB	Input	Pullup	Controls frequency division for Bank B outputs. LVCMOS interface levels.
24	DIV SELA	Input	Pullup	Controls frequency division for Bank A outputs. LVCMOS interface levels.
25, 27, 29, 31, 33	QA0, QA1, QA2, QA3, QA4	Output		Bank A outputs. LVCMOS interface levels. $7\Omega$ typical output impedance.
26, 32	$V_{DDOA}$	Power		Output Bank A supply pins.
34, 36, 38, 40, 42	QB0, QB1, QB2, QB3, QB4	Output		Bank B outputs. LVCMOS interface levels. $7\Omega$ typical output impedance.
35, 41	$V_{DDOB}$	Power		Output Bank B supply pins.

NOTE: Pullup refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$C_{IN}$	Input Capacitance			4		pF
$R_{PULLUP}$	Input Pullup Resistor			51		K $\Omega$
$C_{PD}$	Power Dissipation Capacitance (per output)	$V_{DD}, *V_{DDOx} = 3.465$			15	pF
$R_{OUT}$	Output Impedance		5	7	12	$\Omega$

\*NOTE:  $V_{DDOx}$  denotes  $V_{DDOA}$ ,  $V_{DDOB}$ ,  $V_{DDOC}$ , and  $V_{DDOD}$ .

TABLE 3. FUNCTION TABLE

Inputs				Outputs				
nMR/OE	DIV_SELx	INV1	INV0	Bank A	Bank B	Bank C	Bank D	Qx Frequency
0	X	X	X	Hi Z	Hi Z	Hi Z	Hi Z	zero
1	0	0	0	Inverting	Non-inverting	Non-inverting	Non-inverting	fIN/2
1	0	0	1	Inverting	Inverting	Non-inverting	Non-inverting	fIN/2
1	0	1	0	Inverting	Inverting	Inverting	Non-inverting	fIN/2
1	0	1	1	Inverting	Inverting	Inverting	Inverting	fIN/2
1	1	0	0	Inverting	Non-inverting	Non-inverting	Non-inverting	fIN
1	1	0	1	Inverting	Inverting	Non-inverting	Non-inverting	fIN
1	1	1	0	Inverting	Inverting	Inverting	Non-inverting	fIN
1	1	1	1	Inverting	Inverting	Inverting	Inverting	fIN

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5$ V
Outputs, $V_O$	-0.5V to $V_{DDO} + 0.5$ V
Package Thermal Impedance, $\theta_{JA}$	47.9°C/W (0 lfpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDOx} = 3.3V \pm 5\%$  OR  $2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDOx}$	Output Supply Voltage; NOTE 1		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
$I_{DD}$	Power Supply Current				95	mA
$I_{DDOx}$	Output Supply Current				32	mA

NOTE 1:  $V_{DDOx}$  denotes  $V_{DDOx}$ ,  $V_{DDOB}$ ,  $V_{DDOC}$ , and  $V_{DDOD}$ .

**TABLE 4B. LVCMOS/LVTTTL DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDOx} = 3.3V \pm 5\%$  OR  $2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	DIV_SELA, DIV_SELB, DIV_SELC, DIV_SELD, INV0, INV1, nMR/OE	2		$V_{DD} + 0.3$	V
		CLK	2		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage	DIV_SELA, DIV_SELB, DIV_SELC, DIV_SELD, INV0, INV1, nMR/OE	-0.3		0.8	V
		CLK	-0.3		1.3	V
$I_{IH}$	Input High Current	$V_{DD} = V_{IN} = 3.465\text{V}$ , $V_{DD} = V_{IN} = 2.625\text{V}$			5	$\mu\text{A}$
$I_{IL}$	Input Low Current	$V_{DD} = 3.465\text{V}$ , $V_{IN} = 0\text{V}$ , $V_{DD} = 2.625\text{V}$ , $V_{IN} = 0\text{V}$	-150			$\mu\text{A}$
$V_{OH}$	Output High Voltage; NOTE 1	* $V_{DDOx} = 3.465\text{V}$	2.6			V
		* $V_{DDOx} = 2.625\text{V}$	1.8			V
$V_{OL}$	Output Low Voltage; NOTE 1				0.5	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{DDOx}/2$ . See Parameter Measurement Information section, "3.3V Output Load Test Circuit".

\*NOTE:  $V_{DDOx}$  denotes  $V_{DDOx}$ ,  $V_{DDOB}$ ,  $V_{DDOC}$ ,  $V_{DDOD}$ .

**TABLE 5A. AC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDOX} = 3.3V \pm 5\%$  OR  $2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				250	MHz
$t_{PD}$	Propagation Delay; NOTE 1		2.0		3.5	ns
$t_{sk}(b)$	Bank Skew; NOTE 2, 7	Measured on the Falling Edge			250	ps
$t_{sk}(o)$	Output Skew; NOTE 3, 7	Measured on the Falling Edge			300	ps
$t_{sk}(w)$	Multiple Frequency Skew; NOTE 4, 7				350	ps
$t_{sk}(pp)$	Part to Part Skew; NOTE 5, 7				700	ps
$t_R / t_F$	Output Rise/Fall Time; NOTE 6	20% to 80%	150		800	ps
odc	Output Duty Cycle	$f \leq 133\text{MHz}$	46		54	%
		$f > 133\text{MHz}$	42		58	%
$t_{EN}$	Output Enable Time; NOTE 6				6	ns
$t_{DIS}$	Output Disable Time; NOTE 6				6	ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Measured from the  $V_{DD}/2$  of the input to  $V_{DDOX}/2$  of the output.

NOTE 2: Defined as skew within a bank with equal load conditions.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at  $V_{DDOX}/2$ .

NOTE 4: Defined as skew across banks of outputs switching in the same direction operating at different frequencies with the same supply voltages and equal load conditions. Measured at  $V_{DDOX}/2$ .

NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature and with equal load conditions. Using the same type of input on each device, the output is measured at  $V_{DDOX}/2$ .

NOTE 6: These parameters are guaranteed by characterization. Not tested in production.

NOTE 7: This parameter is defined in accordance with JEDEC Standard 65.

**TABLE 5A. AC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDOX} = 3.3V \pm 5\%$  OR  $2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

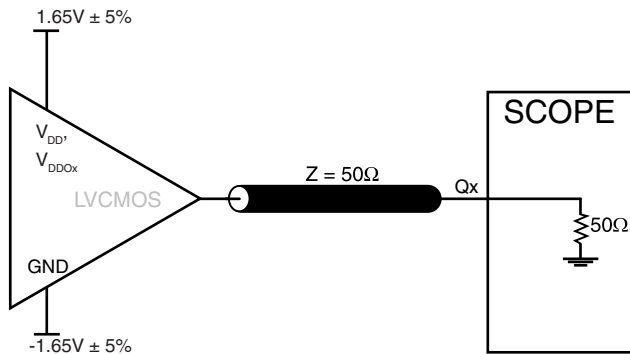
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$t_{sk}(inv)$	Inverting Skew; NOTE 1, 2	$f = 66.7\text{MHz}$			400	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

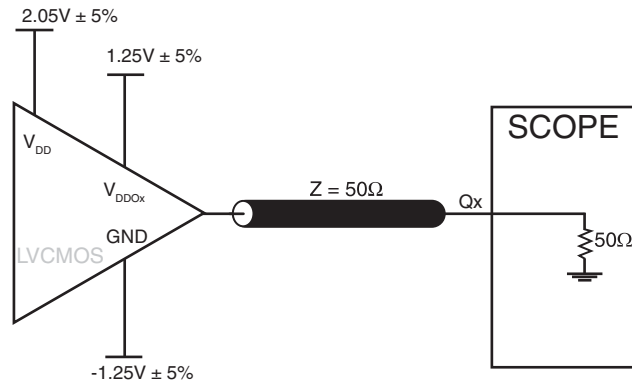
NOTE 1: Defined as skew across banks of outputs switching in opposite directions operating at the same frequency with the same supply voltages and equal load conditions. Measured at  $V_{DDOX}/2$ .

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

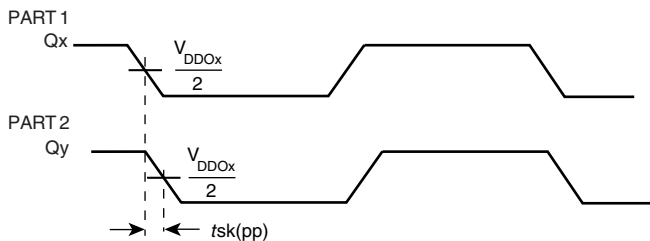
## PARAMETER MEASUREMENT INFORMATION



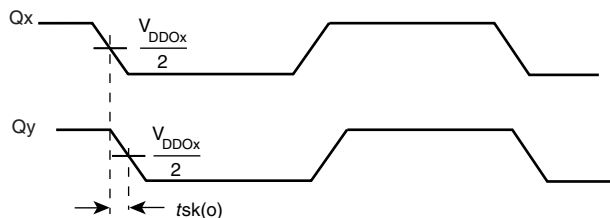
**3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT**



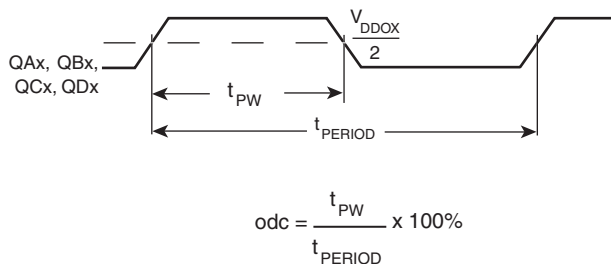
**3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT**



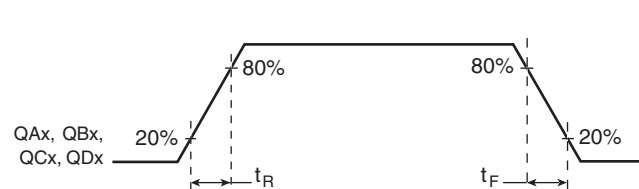
**PART-TO-PART SKEW**



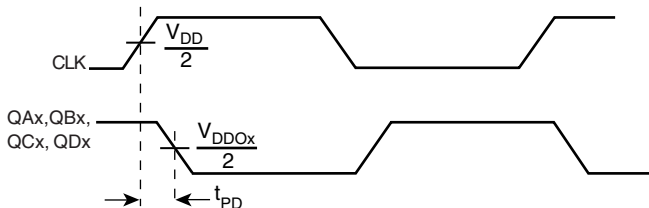
**OUTPUT SKEW**



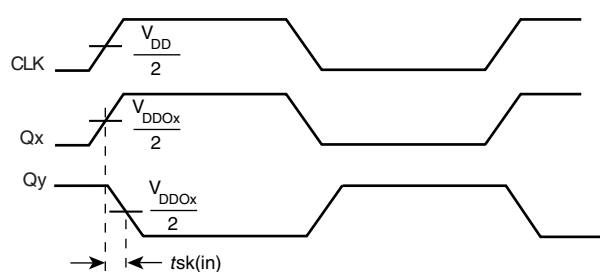
**OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**



**OUTPUT RISE/FALL TIME**



**PROPAGATION DELAY**



**INVERTING SKEW**

## RELIABILITY INFORMATION

**TABLE 6.  $\theta_{JA}$  vs. AIR FLOW TABLE FOR 48 LEAD LQFP**

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	<b>0</b>	<b>200</b>	<b>500</b>
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### TRANSISTOR COUNT

The transistor count for ICS8701I-01 is: 1819

PACKAGE OUTLINE - Y SUFFIX FOR 48 LEAD LQFP

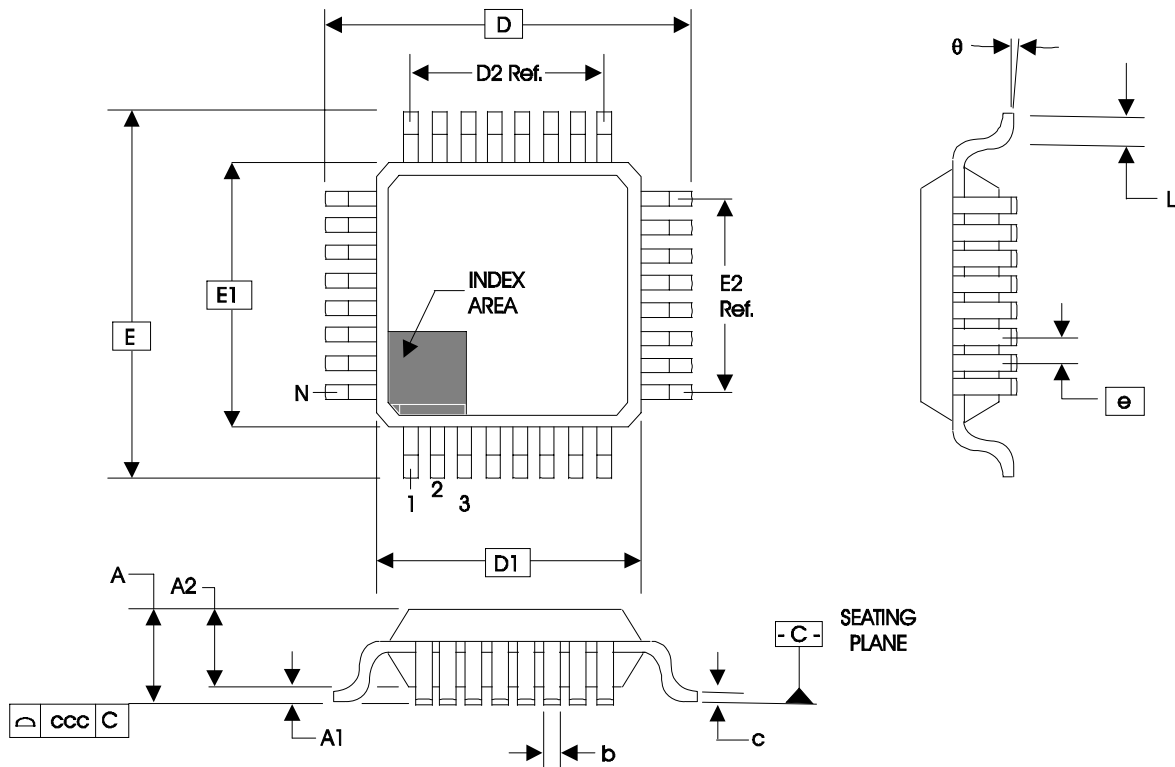


TABLE 7. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBC		
	MINIMUM	NOMINAL	MAXIMUM
N	48		
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	9.00 BASIC		
D1	7.00 BASIC		
D2	5.50 Ref.		
E	9.00 BASIC		
E1	7.00 BASIC		
E2	5.50 Ref.		
e	0.50 BASIC		
L	0.45	0.60	0.75
theta	0°	--	7°
ccc	--	--	0.08

Reference Document: JEDEC Publication 95, MS-026

**TABLE 8. ORDERING INFORMATION**

Part/Order Number	Marking	Package	Packaging	Temperature
8701AYI-01	ICS8701AYI-01	48 Lead LQFP	Tray	-40°C to 85°C
8701AYI-01T	ICS8701AYI-01	48 Lead LQFP	1000 Tape & Reel	-40°C to 85°C
8701AYI-01LF	ICS8701AI01L	Lead-Free, 48 Lead LQFP	Tray	-40°C to 85°C
8701AYI-01LFT	ICS8701AI01L	Lead-Free, 48 Lead LQFP	1000 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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REVISION HISTORY SHEET				
Rev	Table	Page	Description of Change	Date
A	T5A & T5B	4	AC Characteristics Tables - added Thermal note.	3/2/10
		5	Updated Parameter Measurement Information section.	
	7	Updated Package Outline.		
	8	Ordering Information Table - deleted "ICS" prefix. Added lead-free marking.		
	T8			



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