CYPRESS SEMICONDUCTOR

CYM1822

16K x 32 Static RAM Module with Separate I/O

Features

- High-density 512K-bit SRAM module
- High-speed CMOS SRAMs
  - Access time of 12 ns
- Low active power
  - 5.3W (max.)
- Hermetic SMD technology
- TTL-compatible inputs and outputs
- Low profile
  - Max. height of .52 in.
- Small PCB footprint
  - 1.0 sq. in.
- 2V data retention (L version)

Functional Description

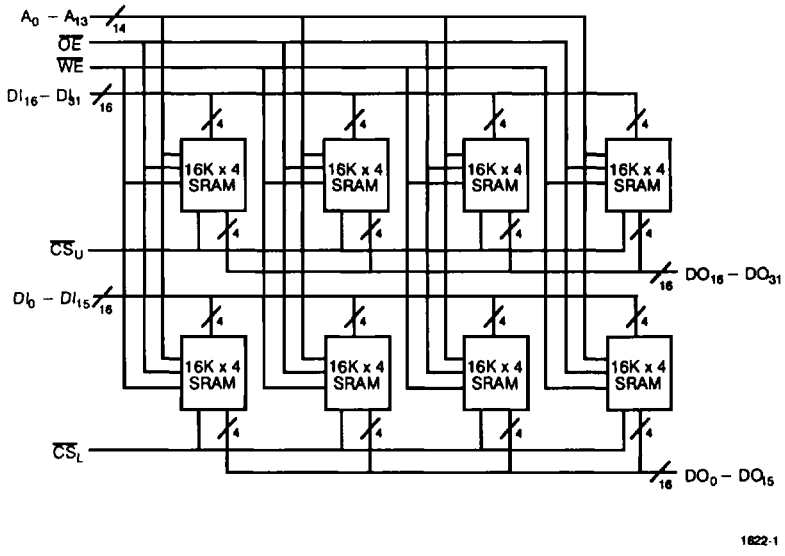
The CYM1822 is a high-performance 512-kbit static RAM module organized as 16K words by 32 bits. This module is constructed from eight 16K x 4 separate I/O SRAMs in leadless chip carriers mounted on a ceramic substrate with pins. Two chip selects ($\overline{CS}_U$ and $\overline{CS}_L$) are used to independently enable the upper and lower 16-bit data words.

Writing to the device is accomplished when the chip selects ($\overline{CS}_U$ and/or $\overline{CS}_L$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input pins (DI_X) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking the chip selects ($\overline{CS}_U$ and/or $\overline{CS}_L$) and output enable ($\overline{OE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data output pins (DO_X).

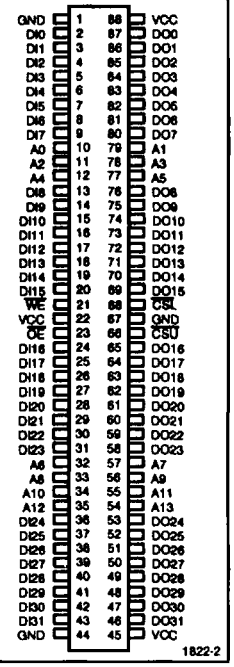
The output pins stay in the high-impedance state when write enable ($\overline{WE}$) is LOW, the appropriate chip selects are HIGH, or $\overline{OE}$ is HIGH.

Logic Block Diagram



Pin Configuration

VDIP



Selection Guide

	1822HV-12	1822HV-15	1822HV-20	1822HV-25	1822HV-30	1822HV-35	1822HV-45
Maximum Access Time (ns)	12	15	20	25	30	35	45
Maximum Operating Current	960	960	720	720	720	720	720
Maximum Standby Current	450	450	160	160	160	160	160

Shaded area contains preliminary information.

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Output Current into Outputs (Low) ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	1822HV-12 1822HV-15		1822HV-20 1822HV-25 1822HV-35 1822HV-45 1822HV-50		Units
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−20	+20	−20	+20	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−20	+20	−20	+20	µA
I_{OS}	Output Short Circuit Current [1]	V_{CC} = Max., V_{OUT} = GND		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA $\overline{CS}_L$, $\overline{CS}_U$ ≤ V_{IL}		960		720	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current [2]	Max. V_{CC}; $\overline{CS}_U$, $\overline{CS}_L$ ≥ V_{IH} Min. Duty Cycle = 100%		450		160	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current [2]	Max. V_{CC}; $\overline{CS}_U$, $\overline{CS}_L$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V		—		160	mA

Shaded area contains preliminary information.

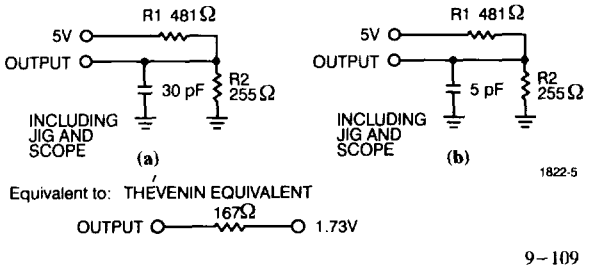
Capacitance [3]

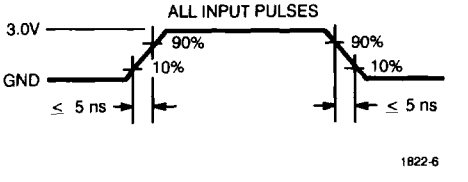
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	80	pF
C_{OUT}	Output Capacitance		15	pF
C_{INDATA}	Input Capacitance		15	pF

Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. A pull-up resistor to V_{CC} on the CE input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
3. Tested on a sample basis.

Ac Test Loads and Waveforms





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Switching Characteristics Over the Operating Range [4]

Parameters	Description	1822HV-12		1822HV-15		1822HV-20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	12		15		20		ns
t_{AA}	Address to Data Valid		12		15		20	ns
t_{OHA}	Data Hold from Address Change	2		2		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		12		15		20	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		10		15	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	2		2		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		8		8		8	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z [6]	3		3		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z [5, 6]		8		8		8	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		12		15		20	ns
WRITE CYCLE [7]								
t_{WC}	Write Cycle Time	12		15		20		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	10		12		15		ns
t_{AW}	Address Set-Up to Write End	10		12		15		ns
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		12		15		ns
t_{SD}	Data Set-Up to Write End	10		10		13		ns
t_{HD}	Data Hold from Write End	2		2		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [6]	3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [5, 6]	0	7	0	7	0	7	ns

Shaded area contains preliminary information.

Notes:

4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
6. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
7. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Characteristics Over the Operating Range (continued) [4]

Parameters	Description	1822HV-25		1822HV-30		1822HV-35		1822HV-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	25		30		35		45		ns
t_{AA}	Address to Data Valid		25		30		35		45	ns
t_{OHA}	Data Hold from Address Change	5		5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		25		30		35		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		15		20		25		30	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		5		5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		15		20		20		20	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z [6]	5		10		10		10		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z [5, 6]		10		15		15		20	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		25		30		35		45	ns
WRITE CYCLE [7]										
t_{WC}	Write Cycle Time	25		30		35		45		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		25		30		40		ns
t_{AW}	Address Set-Up to Write End	20		25		30		40		ns
t_{HA}	Address Hold from Write End	2		2		2		2		ns
t_{SA}	Address Set-Up to Write Start	2		2		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		25		30		ns
t_{SD}	Data Set-Up to Write End	13		20		20		25		ns
t_{HD}	Data Hold from Write End	3		3		3		3		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [6]	3		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [5, 6]	0	7	0	12	0	12	0	15	ns

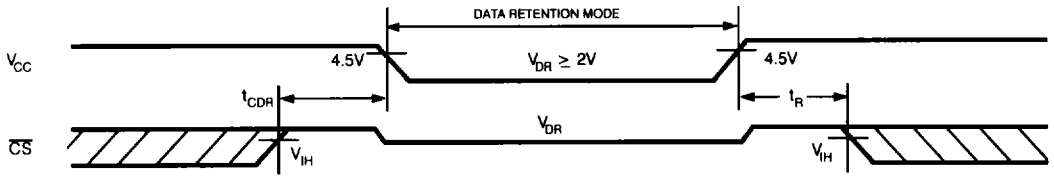
Data Retention Characteristics (L Version Only)

Parameter	Description	Test Conditions	CYM1822		Units
			Min.	Max.	
V_{DR}	V_{CC} for Retention Data	V_{CC} = 2.0V, $\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} > V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	2.0		V
I_{CCDR}	Data Retention Current			8	mA
t_{CDR} [8]	Chip Deselect to Data Retention Time		0		ns
t_R [8]	Operation Recovery Time		t_{RC} [9]		ns
I_{LI} [8]	Input Leakage Current			10	µA

Notes:

8. Guaranteed, not tested.
9. t_{RC} = Read Cycle Time.
10. Both $\overline{CS}_L$ and $\overline{CS}_U$ are represented by $\overline{CS}$ in the Switching Characteristics and Waveforms.
11. $\overline{WE}$ is HIGH for read cycle.
12. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{OE}$ = V_{IL}.
13. Address valid prior to or coincident with $\overline{CS}$ transition low.
14. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

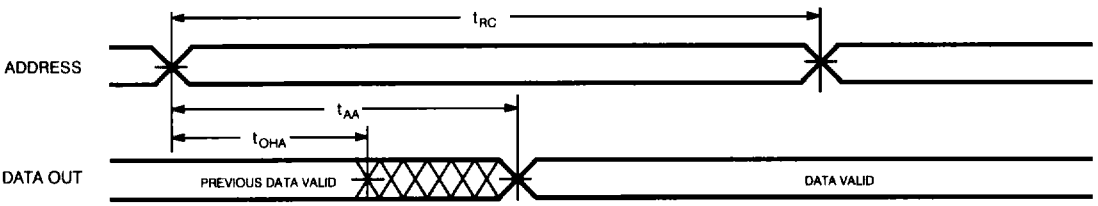
Data Retention Waveform



1822-7

Switching Waveforms [10]

Read Cycle No. 1 [11, 12]



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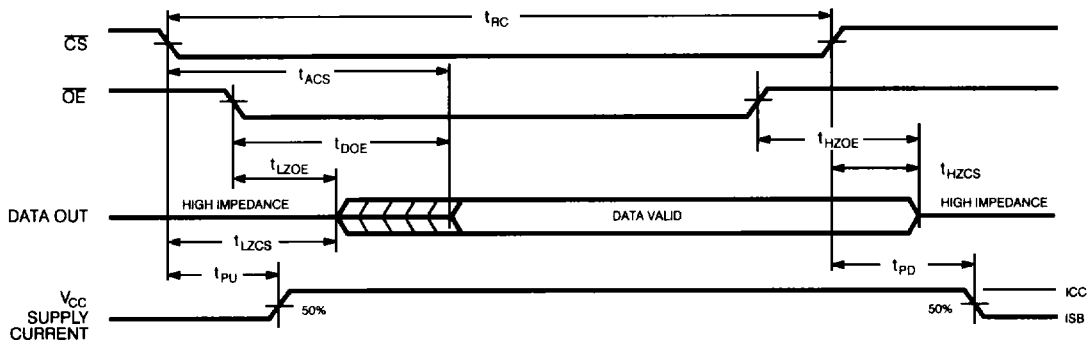
Read Cycle No. 2 [11, 13]



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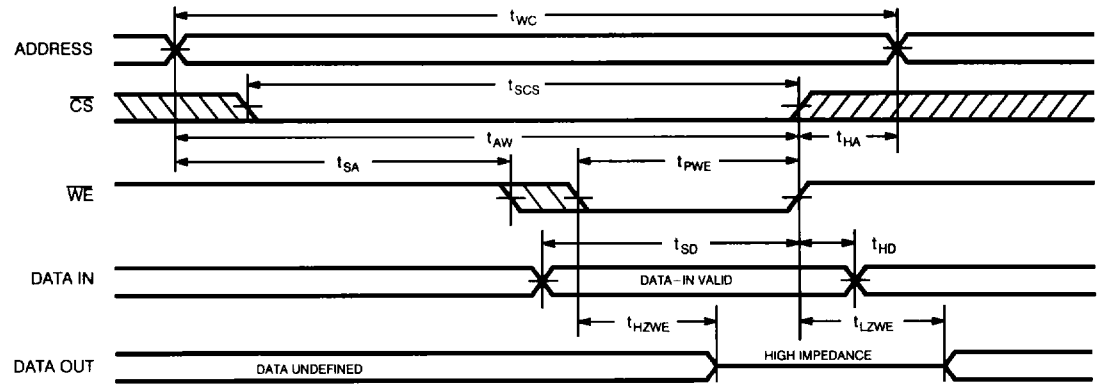
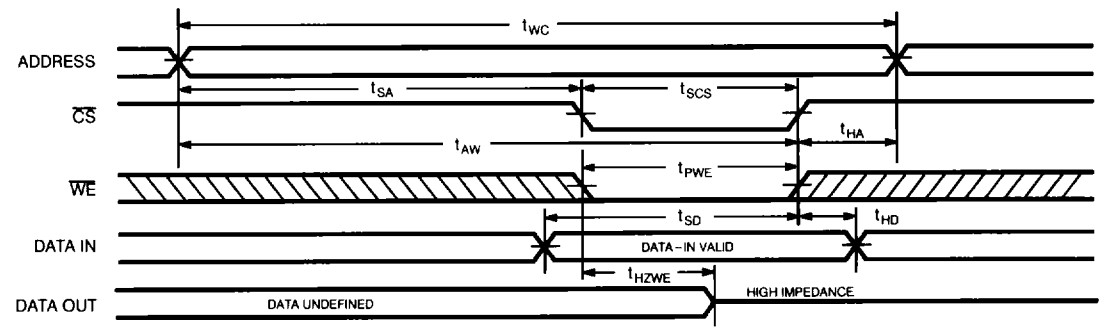
Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{WE}$ Controlled) [7]



Write Cycle No. 2 ($\overline{CS}$ Controlled) [7, 14]



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Truth Table

$\overline{CS_U}$	$\overline{CS_L}$	$\overline{OE}$	$\overline{WE}$	Input/Outputs	Mode
H	H	X	X	High Z	Deselect/Power-Down
L	L	L	H	Data Out $_{0-31}$	Read
H	L	L	H	Data Out $_{0-15}$	Read Lower Word
L	H	L	H	Data Out$_{16-31}$	Read Upper Word
L	L	X	L	Data In $_{0-31}$	Write
H	L	X	L	Data In $_{0-15}$	Write Lower Word
L	H	X	L	Data In $_{16-31}$	Write Upper Word
L	L	H	H	High Z	Deselect
H	L	H	H	High Z	Deselect
L	H	H	H	High Z	Deselect

Ordering Information

Speed	Ordering Code	Package Type	Operating Range
12	CYM1822HV-12C	HV02	Commercial
15	CYM1822HV-15C	HV02	Commercial
20	CYM1822HV-20C	HV02	Commercial
	CYM1822LHV-20C	HV02	
25	CYM1822HV-25C	HV02	Commercial
	CYM1822LHV-25C	HV02	
30	CYM1822HV-30C	HV02	Commercial
	CYM1822LHV-30C	HV02	
35	CYM1822HV-35C	HV02	Commercial
	CYM1822LHV-35C	HV02	
45	CYM1822HV-45C	HV02	Commercial
	CYM1822LHV-45C	HV02	

Document #: 38-M-00016-B