SPARCore™ CPU Module

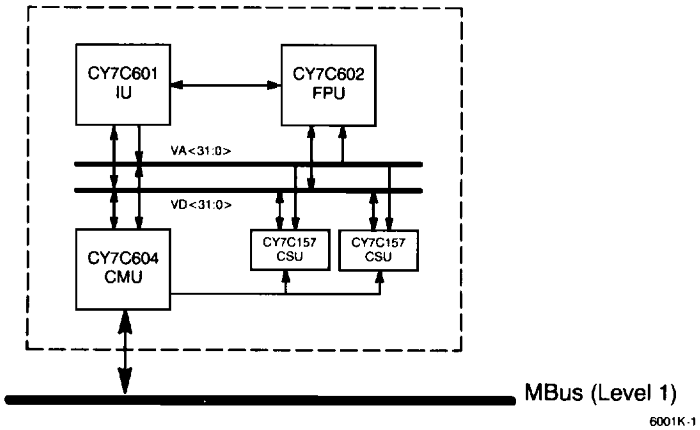
Features

- **Complete SPARC® CPU solution, including cache**
  - **— CY7C601 Integer Unit (IU)**
  - **— CY7C602 Floating-Point Unit (FPU)**
  - **— CY7C604 Cache Controller and Memory Management Unit (CMU)**
  - **— Two CY7C157 Cache Storage Units (CSU)**
- **SPARC compliant**
  - **— SPARC Instruction Set Architecture (ISA) compliant**
  - **— Conforms to SPARC Reference MMU Architecture**
  - **— Conforms to SPARC Level 1 MBus Module Specification (Revision 1.2)**
- **High performance**
  - **— 32 MIPS (sustained)**
  - **— 7 MFLOPS [SP], 5 MFLOPS [DP] (sustained)**
  - **— 28 SPECmarks**
- **Available at 25, 33, and 40 MHz**
- **Each SPARCore module features:**
  - **— SPARC integer and floating-point processing**
  - **— Zero-wait-state, 64-Kbyte cache**
  - **— Demand-paged virtual memory management**
  - **— Surface-mount packaging for more compact design**
  - **— Provides CPU upgrade path at module level**
- **Module design**
  - **— Two power and two ground planes**
  - **— Minimum-skew clock distribution**
  - **— MBus-standard form factor: 3.30″ (8.34 cm) x 5.78″ (14.67 cm)**
- **SPARCore MBus connector**
  - **— SPARC-standard**
  - **— Separate power and ground blades (100 active pins)**
  - **— Designed for high frequency (low capacitance, low inductance)**

Functional Description

The CYM6001K SPARCore Module is a complete SPARC CPU board. It is packaged as a compact PCB and interfaces to the remainder of the system via a SPARC-standard MBus connector. The CPU on the CYM6001K consists of a high-speed integer unit (CY7C601), floating-point unit (CY7C602), cache controller and memory management unit (CY7C604), and two 16K x 16 CY7C157 cache storage units (providing a 64-Kbyte cache for the CPU). The CYM6001K delivers sustained performance of 32 MIPS and 7/5 (single precision/double precision) MFLOPS at an operating frequency of 40 MHz. The CYM6001K achieves an overall SPECmark rating of 28. IC components are surface mounted for a compact footprint. The CYM6001K fits within the clearance envelope for MBus modules per the SPARC MBus Specification.

Logic Block Diagram



Selection Guide

		6001K−40	6001K−33	6001K−25
Operating Frequency (MHz)		40	33	25
Typical Supply Current (mA)	Commercial	1720	1555	1390
Maximum Supply Current (mA)	Commercial	2600	2350	2100
Required Ambient Airflow – Module Top Side (LFM)		250	250	250

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Functional Description (continued)

The CYM6001K interfaces to the rest of the system via the SPARC MBus and conforms to the SPARC Reference MMU. This standardizationallows the CYM6001K to be replaced by other Cypress SPARC MBus-based CPU modules without having to modify any portion of the memory system or I/O. This CPU "building block" strategy not only decreases the user's time to market, but also provides a mechanism for upgrading in the field. For a more complete description of the individual SPARC components used in the CYM6001K (i.e., the CY7C601 IU, the CY7C602 FPU, the CY7C604 CMU, and the CY7C157 CSUs), please refer to the *Cypress SPARC RISC User's Guide*.

Module Design

Clock Distribution

The CYM6001K uses two module clock signals (MCLK0 and MCLK1) as defined in the MBus Specification. In order to minimize clock skew, traces have been carefully routed. All clock lines are routed on inner layers of the module PCB, and their impedances have been matched. All clock lines have diode termination to reduce signal undershoot and overshoot.

MBus Connector (Module)

The CYM6001K interface is via the 100-pin SPARC MBus connector, which is a two-row male connector with 0.050" spacing (AMP "microstrip" part number 121354–4). The connector is a controlled impedance-type (55Ω +10%) based on a microstrip configuration which provides a controlled characteristic impedance plus very low inductance and capacitance. Separate power and ground blades are provided for isolation to prevent noise. *Table 1* details the CYM6001K standard connector pinout.

Mating MBus Connector (System Interface Board)

The module connects to the system interface by means of a standard MBus female connector (AMP vertical receptacle assembly, part number 121340–4).

Reset and Interrupt Signals

A power-on reset signal is generated to the module from the MBus via the $\overline{\text{RSTIN}}$ signal. Level-sensitive interrupts (15 max) are generated to the CY7C601 via the IRL0[3:0] and lines from the MBus. A value of 0000b means that there is no interrupt while a value of 1111b means an NMI (Non-Maskable Interrupt) is being asserted. IRL values between 0 and 15 represent interrupt requests that can be masked by the processor.

Table 1. MBus Connector Pinout[1]

Pin #	Signal Name	Blade	Pin #	Signal Name
1	RES1	Blade #1	2	RES2
3	RES3	Ground	4	RES4
5	RES5		6	IRL0[1]
7	IRL0[0]	Ground	8	IRL0[3]
9	IRL0[2]		10	RES6
11	MAD[0]	Ground	12	MAD[1]
13	MAD[2]		14	MAD[3]
15	MAD[4]	Ground	16	MAD[5]
17	MAD[6]		18	MAD[7]
19	MAD[8]		20	MAD[9]
21	MAD[10]	Blade #2	22	MAD[11]
23	MAD[12]	+5V	24	MAD[13]
25	MAD[14]		26	MAD[15]
27	MAD[16]	+5V	28	MAD[17]
29	MAD[18]		30	MAD[19]
31	MAD[20]	+5V	32	MAD[21]
33	MAD[22]		34	MAD[23]
35	MAD[24]	+5V	36	MAD[25]
37	MAD[26]		38	MAD[27]
39	MAD[28]		40	MAD[29]
41	MAD[30]	Blade #3	42	MAD[31]
43	$\overline{\text{MBR[0]}}$	Ground	44	RES7
45	$\overline{\text{MBG[0]}}$		46	RES8
47	MCLK0	Ground	48	$\overline{\text{MRTY}}$
49	MCLK1		50	$\overline{\text{MRDY}}$
51	RES9	Ground	52	$\overline{\text{MERR}}$
53	RES10		54	$\overline{\text{MAS}}$
55	RES11	Ground	56	$\overline{\text{MBB}}$
57	RES12		58	SPARE1
59	MAD[32]		60	MAD[33]
61	MAD[34]	Blade #4	62	MAD[35]
63	MAD[36]	+5V	64	MAD[37]
65	MAD[38]		66	MAD[39]
67	MAD[40]	+5V	68	MAD[41]
69	MAD[42]		70	MAD[43]
71	MAD[44]	+5V	72	MAD[45]
73	MAD[46]		74	MAD[47]
75	MAD[48]	+5V	76	MAD[49]
77	MAD[50]		78	MAD[51]
79	MAD[52]		80	MAD[53]
81	MAD[54]	Blade #5	82	MAD[55]
83	MAD[56]	Ground	84	MAD[57]
85	MAD[58]		86	MAD[59]
87	MAD[60]	Ground	88	MAD[61]
89	MAD[62]		90	MAD[63]
91	SPARE2	Ground	92	RES13
93	RES14		94	RES15
95	RES16	Ground	96	$\overline{\text{AERR}}$
97	$\overline{\text{RSTIN}}$		98	RES17
99	RES18		100	RES19

Note:

1. RES pins are not used in the CYM6001K but are reserved for other MBus module upgrades (e.g., multiprocessing, dual CPUs, JTAG capabilities). See the System Design Considerations section for the assignments of these reserved pins per the SPARC MBus Specification.

Maximum Ratings[2]

(Provided as guidelines; not tested.)

Storage Temperature .... − 20°C to +75°C
Ambient Temperature with Power Applied .... 0°C to +50°C
Supply Voltage to Ground Potential .... − 0.5V to +7.0V
Input Voltage .... − 0.3V to +7.0V

Operating Range

Range	Ambient Temperature[3]	V_{CC}
Commercial	0°C to +50°C	5V ± 5%

DC Electrical Characteristics Over the Operating Range[4]

Parameters	Description	Test Conditions	Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 2.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.5	V
V_{IH}	Input HIGH Voltage		2.1	V_{CC}	V
V_{IL}	Input LOW Voltage		− 0.5	0.8	V
I_{IZ}	Input Leakage Current (non-clock pins)	V_{CC} = Max., $V_{SS} \leq V_{OUT} \leq V_{CC}$	− 10	+10	mA
I_{CLKZ}	Input Leakage Current (clock pins)	V_{CC} = Max., $V_{SS} \leq V_{OUT} \leq V_{CC}$	− 40	+40	mA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \leq V_{OUT} \leq V_{CC}$	− 15	+15	mA
I_{SC}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = 0V	− 30	− 350	mA

Capacitance[5]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	V_{CC} = 5.0V, T_A = 25°C, f = 1 MHz	10	pF
C_{OUT}	Output Capacitance		12	pF
C_{IO}	Input/Output Capacitance		15	pF
C_{INCLK}	Clock Input Capacitance		60	pF

Notes:

2. All power and ground pins must be connected to other pins of the same type before any power is applied to the module. At least one clock cycle must be applied to the module to setup the internal chip drivers properly.
3. Ambient temperature is the temperature of the air in immediate proximity of the module.
4. Not more than one output should be tested at one time. Duration of the short circuit should not be more than one second.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Electrical Characteristics Over the Operating Range[6, 7]

Synchronous Signals[8]

Parameter	Description	Signal Edge	CYM6001K-40 Min.	CYM6001K-40 Max.	CYM6001K-33 Min.	CYM6001K-33 Max.	CYM6001K-25 Min.	CYM6001K-25 Max.	Units
t_{CY}	Clock Cycle		25		30		40		ns
t_{CHL}	Clock High and Low		11.5	13.5	13.5	16.5	18.5	21.5	ns
t_R,t_F	Clock Rise and Fall (between 0.8V and 2.0V)		0.8		0.8		0.8		V/ns
t_{SKU}	Clock Skew[9]			1.0		2.0		2.0	ns
t_{MOD}	MAD(63:0) Output Delay	CLK+		20		22		30	ns
t_{MOH}	MAD(63:0) Output Valid	CLK+	4		4		4		ns
t_{MIS}	MAD(63:0) Input Set-Up	CLK+	3.5		5.5		7.5		ns
t_{MIH}	MAD(63:0) Input Hold	CLK+	4.5		4.5		4.5		ns
t_{COD}	MBus Bused Control Output Delay	CLK+		19		21		29	ns
t_{COH}	MBus Bused Control Output Valid	CLK+	4		4		4		ns
t_{CIS}	MBus Bused Control Input Set-Up	CLK+	5.5		8		10		ns
t_{CIH}	MBus Bused Control Input Hold	CLK+	4.5		4.5		4.5		ns
t_{POD}	MBus Point-to-Point Control Output Delay	CLK+		17		19		27	ns
t_{POH}	MBus Point-to-Point Control Output Valid	CLK+	3.5		3.5		3.5		ns
t_{PIS}	MBus Point-to-Point Control Input Set-Up	CLK+	7.5		9		11		ns
t_{PIH}	MBus Point-to-Point Control Input Hold	CLK+	4		4		4		ns
t_{RIS}	$\overline{POR}$ Input Setup	CLK+	5		5		5		ns
t_{RIH}	$\overline{POR}$ Input Hold	CLK+	6		6		6		ns
t_{IIS}	IRL Input Setup	CLK+	5		5		5		ns
t_{IIH}	IRL Input Hold	CLK+	7		7		7		ns

Asynchronous Signals[10, 11]

Parameter	Description	Signal Edge	CYM6001K-40 Min.	CYM6001K-40 Max.	CYM6001K-33 Min.	CYM6001K-33 Max.	CYM6001K-25 Min.	CYM6001K-25 Max.	Units
$\overline{RSTIN}$[12]	MBus Reset	Input	500		500		500		ms

Notes:

6. Test conditions assume signal transition times of 3 ns or less, a timing reference level of 1.5V, input levels of 0 to 3.0V, and output loading of 100-pF capacitance, not including the module itself (with the exception of $\overline{MBR}$, tested with an output loading of 40 pF).
7. All measurements made at MBus connector.
8. All timing parameters are guaranteed relative to MCLK0.
9. Measured between any two CLK signals. The relaxed skew requirements for 25 and 33 MHz should be considered carefully since upgrading to 40 MHz requires a 1.0-ns or shorter clock skew.
10. The module requires that the interrupt lines (IRL0[0:3]) remain valid until the interrupt is cleared by software with a minimum of two clock cycles.
11. The asynchronous error signal, $\overline{AERR}$ will remain asserted until the AFAR register in the CY7C604 is read by software.
12. Measured at room temperature.

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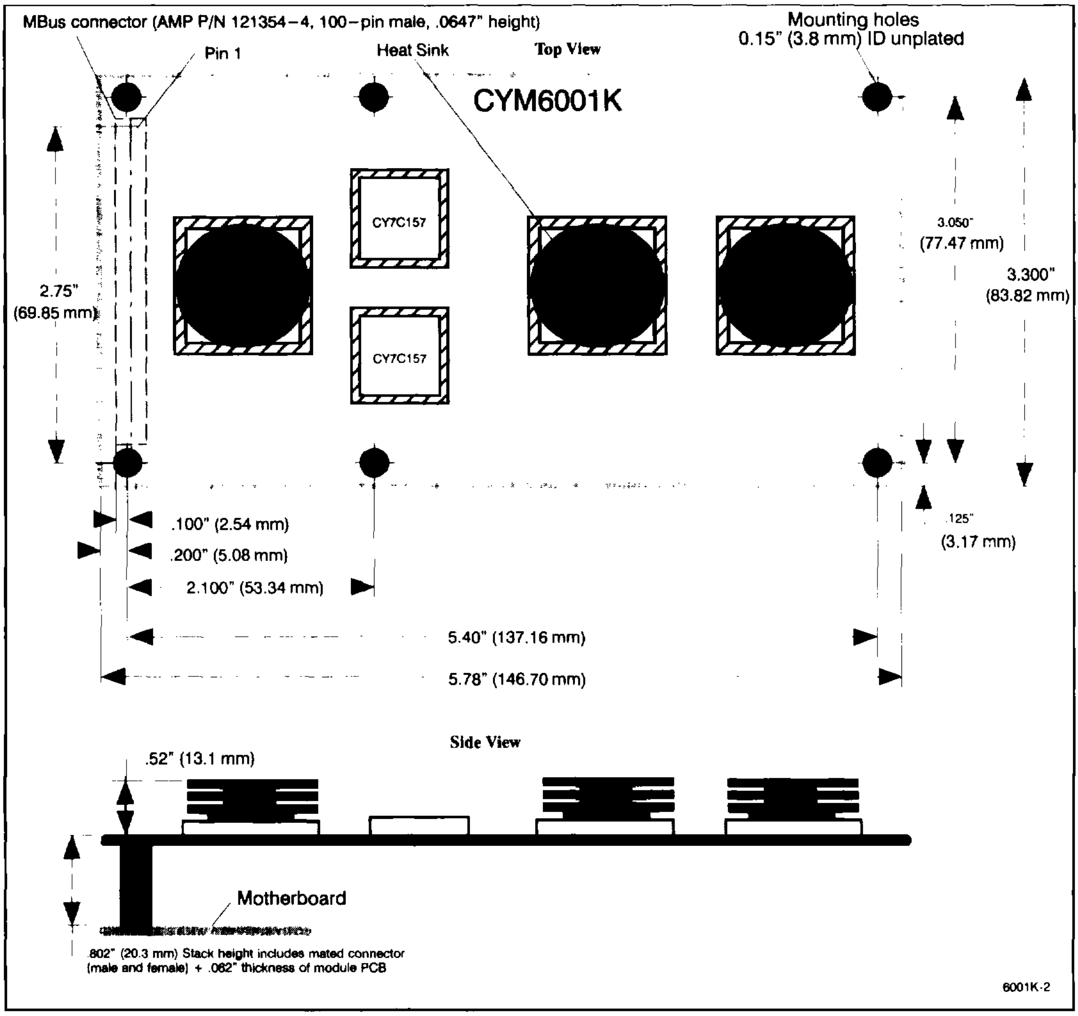
RISC

Mechanical Dimensions[13, 14, 15]

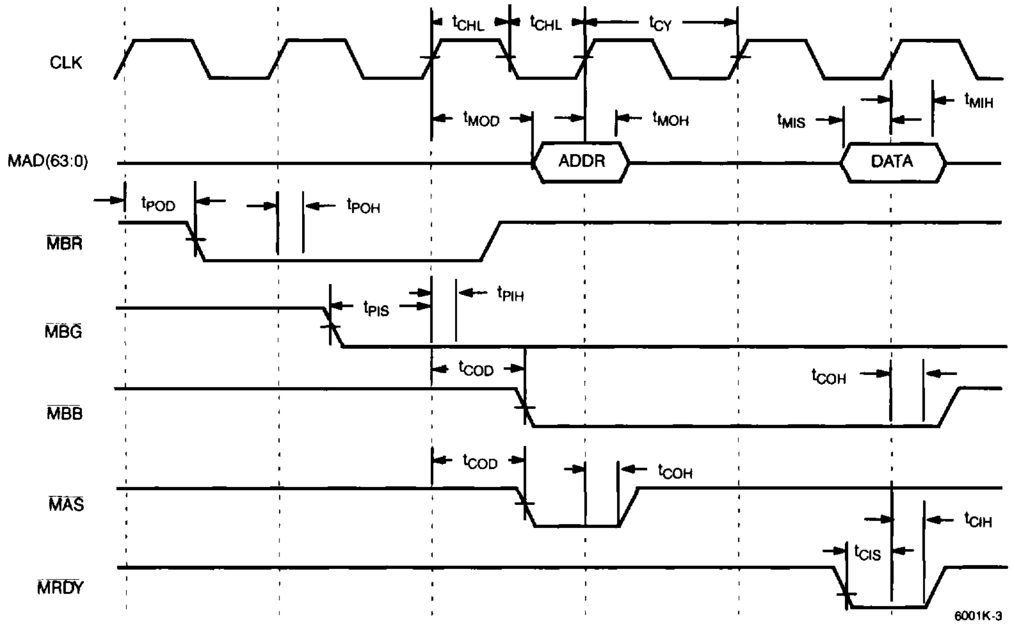


Notes:

13. Drawing is not to scale.
14. All tolerances are per ANSI/IPC–D–300G Specification (Class B).
15. These dimensions are CYM6001K-specific but are also within the mechanical limits specified for MBus modules. To ensure compliance with all future MBus modules, systems developers should design to the MBus module envelope per the SPARC MBus Specification.

MBus Timing Diagram

Single Read Transaction



System Design Considerations

The CYM6001K implements a subset of all possible MBus signals; signals that are optional and/or specifically for multiprocessing, dual CPUs, and JTAG test capabilities may not be supported. However, the MBus connector, per the SPARC MBus Specification, defines the assignments listed in *Table 2* for pins reserved on the CYM6001K. Systems designers should be aware of these assignments in order to more easily upgrade to other and future MBus modules.

Table 2. Pins Reserved on CYM6001K

Pin #	Signal Name	Pin #	Signal Name
1	SCANDI	2	SCANTMS1
3	SCANDO	4	SCANTMS2
5	SCANCLK	10	INTOUT
44	MSH	46	MIH
51	MCLK2	53	MCLK3
55	MBR1	57	MBG1
92	IRL1[0]	93	IRL1[1]
94	IRL[2]	95	IRL[3]
98	ID[1]	99	ID[2]
100	ID[3]		

All MAD, bused control, and point-to-point control signals use 8-mA drivers (with the exception of MAS, which uses a 16-mA driver). The AERR signal uses an open-drain driver.

The following pull-up resistors are recommended for the MBus signals: AERR is pulled up to 5V with a 1.5-kΩ resistor; all other MBus signals are pulled up to 5V with 10-kΩ resistors.

As the frequency of operation increases, transmission line effects play a bigger role. Care must be taken to keep skew between any two clock signals at the MBus connector within the specifications given in the Synchronous Signals table. MBus signal lines must be routed carefully to minimize crosstalk and interference. A thorough SPICE analysis of the motherboard design is recommended. For a discussion of the intricacies of high-frequency design, see the application note titled "High-Speed SPARC CMOS System Design" in the *Cypress Applications Handbook.*

Use of HH Smith #4387 (3/4" length by 1/4" OD) stand-offs on the motherboard or equivalent is recommended to support the module and prevent damage to the connector.

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