



3.3V LOW SKEW PLL-BASED CMOS CLOCK DRIVER (WITH 3-STATE)

IDT74FCT388915T
70/100/133/150

FEATURES:

- 0.5 MICRON CMOS Technology
- Input frequency range: 10MHz – f2Q Max. spec (FREQ_SEL = HIGH)
- Max. output frequency: 150MHz
- Pin and function compatible with FCT88915T, MC88915T
- 5 non-inverting outputs, one inverting output, one 2x output, one $\div 2$ output; all outputs are TTL-compatible
- 3-State outputs
- Duty cycle distortion < 500ps (max.)
- 32/–16mA drive at CMOS output voltage levels
- VCC = 3.3V \pm 0.3V
- Inputs can be driven by 3.3V or 5V components
- Available in 28 pin PLCC and SSOP packages

DESCRIPTION:

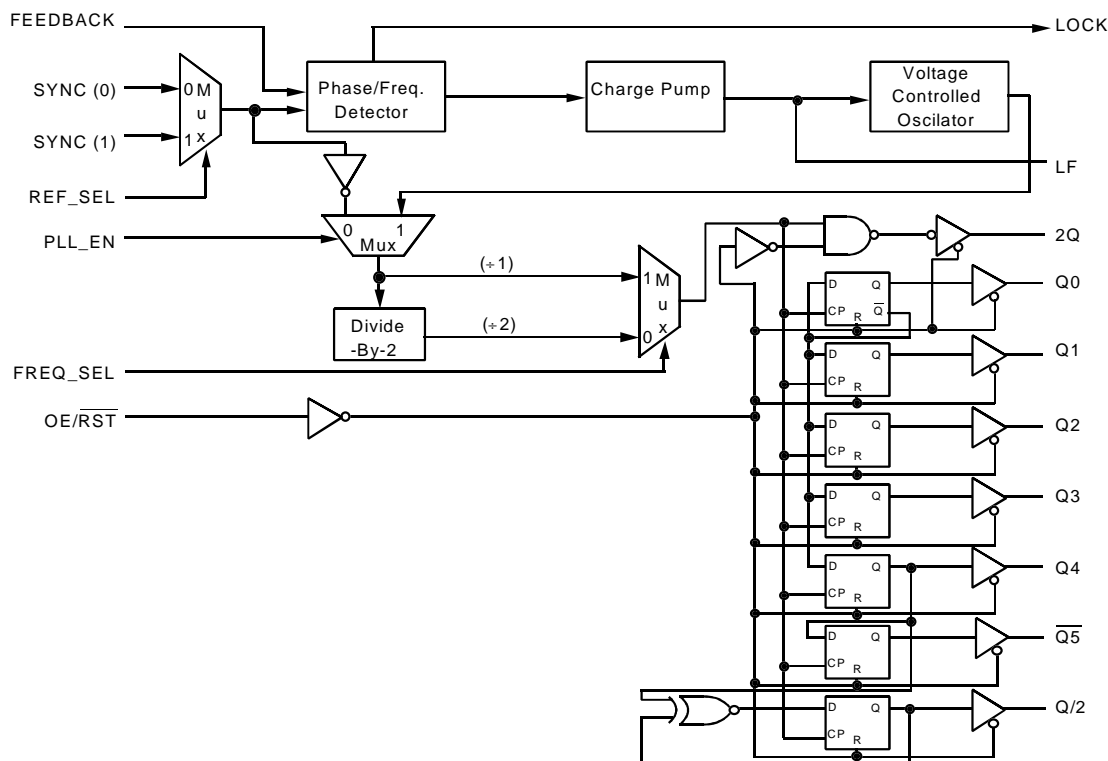
The FCT388915T uses phase-lock loop technology to lock the frequency and phase of outputs to the input reference clock. It provides low skew clock distribution for high performance PCs and workstations. One of the outputs is fed back to the PLL at the FEEDBACK input resulting in essentially zero delay across the device. The PLL consists of the phase/frequency detector, charge pump, loop filter and VCO. The VCO is designed for a 2Q operating frequency range of 40MHz to f2Q Max.

The FCT388915T provides 8 outputs, the $\overline{Q5}$ output is inverted from the Q outputs. The 2Q runs at twice the Q frequency and Q/2 runs at half the Q frequency.

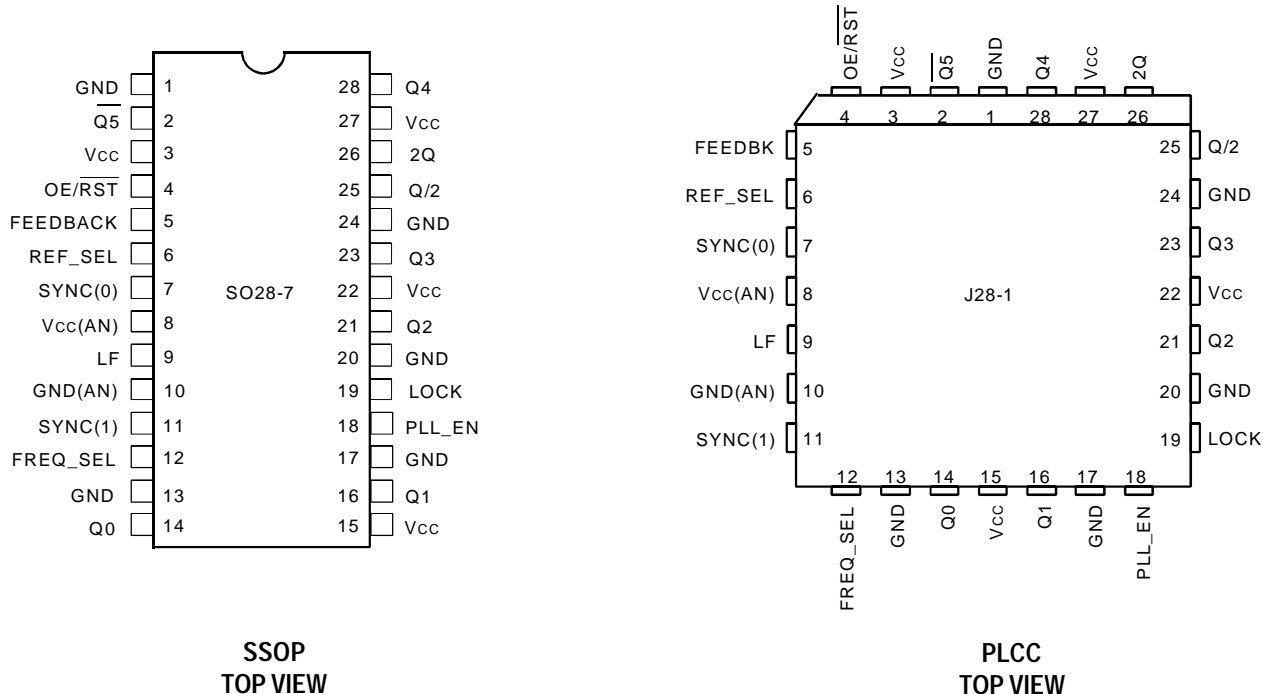
The FREQ_SEL control provides an additional $\div 2$ option in the output path. PLL_EN allows bypassing of the PLL, which is useful in static test modes. When PLL_EN is low, SYNC input may be used as a test clock. In this test mode, the input frequency is not limited to the specified range and the polarity of outputs is complementary to that in normal operation (PLL_EN = 1). The LOCK output attains logic HIGH when the PLL is in steady-state phase and frequency lock. When OE/ \overline{RST} is low, all the outputs are put in high impedance state and registers at Q, \overline{Q} and Q/2 outputs are reset.

The FCT388915T requires one external loop filter component as recommended in Figure 3.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	I/O	Description
SYNC(0)	I	Reference clock input.
SYNC(1)	I	Reference clock input.
REF_SEL	I	Chooses reference between SYNC (0) & SYNC (1). (Refer to functional block diagram)
FREQ_SEL	I	Selects between ÷ 1 and ÷ 2 frequency options. (Refer to functional block diagram)
FEEDBACK	I	Feedback input to phase detector.
LF	I	Input for external loop filter connection.
Q0-Q4	O	Clock output.
Q5	O	Inverted clock output.
2Q	O	Clock output (2 x Q frequency).
Q/2	O	Clock output (Q frequency ÷ 2).
LOCK	O	Indicates phase lock has been achieved (HIGH when locked).
OE/RST	I	Asynchronous reset (active LOW) and output enable (active HIGH). When HIGH, outputs are enabled. When LOW, outputs are in HIGH impedance.
PLL_EN	I	Disables phase-lock for low frequency testing. (Refer to functional block diagram)

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max.	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	−0.5 to +4.6	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	−0.5 to +7	V
V _{TERM} ⁽⁴⁾	Terminal Voltage with Respect to GND	−0.5 to V _{CC} +0.5	V
T _{STG}	Storage Temperature	−65 to +150	°C
I _{OUT}	DC Output Current	−60 to +60	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. Input terminals.
4. Outputs and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8	pF

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: T_A = 0°C to +70°C, V_{CC} = 3.3V ± 0.3V; Industrial: T_A = −40°C to +85°C, V_{CC} = 3V ± 0.3%

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	5.5	V
V _{IL}	Input LOW Level	Guaranteed Logic LOW Level		−0.5	—	0.8	V
I _{IH}	Input HIGH Current	V _{CC} = Max.	V _I = 5.5V	—	—	±1	μA
I _{IL}	Input LOW Current		V _I = GND	—	—	±1	μA
I _{OZH}	High Impedance Output Current (3-State Output Pins)	V _{CC} = Max.	V _O = V _{CC}	—	—	±1	μA
I _{OZL}			V _O = GND	—	—	±1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = −18mA		—	−0.7	−1.2	V
I _{ODH}	Output Drive Current	V _{CC} = Max., V _{IN} = V _{IH} or V _{IL} , V _O = 1.5V ⁽³⁾		−36	—	—	mA
I _{ODL}	Output Drive Current	V _{CC} = Max., V _{IN} = V _{IH} or V _{IL} , V _O = 1.5V ⁽³⁾		50	—	—	mA
V _{OH}	Output HIGH Voltage	V _{CC} = Min.	I _{OH} = −16mA	2.4 ⁽⁴⁾	3	—	V
V _{OL}	Output LOW Voltage	V _{CC} = Min.	I _{OL} = 32mA	—	0.3	0.5	V
V _H	Input Hysteresis	—		—	100	—	mV
I _{CC1} I _{CC2} I _{CCZ}	Quiescent Power Supply Current	V _{CC} = Max., V _{IN} = GND or V _{CC} (Test mode)		—	2	6	mA

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. V_{OH} = V_{CC} - 0.6V at rated current.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = V_{CC} - 2.1V^{(3)}$	$V_{IN} = V_{CC} - 0.6V^{(3)}$	—	2	30	μA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ All Outputs Open	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	0.2	0.3	mA/ MHz
CPD	Power Dissipation Capacitance	50% Duty Cycle		—	15	25	pF
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ PLL_EN = 1, LOCK = 1, FEEDBACK = Q4 SYNC frequency = 50MHz. All bits loaded with 15pF		—	30	60	mA
		$V_{CC} = \text{Max.}$ PLL_EN = 1, LOCK = 1, FEEDBACK = Q4 SYNC frequency = 50MHz. All bits loaded with 50 Ω Thevenin termination and 20pF		—	90	120	mA

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 3.3V$, +25°C ambient.
- Per TTL driven input. All other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations. It is derived with Q frequency as the reference.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} \cdot DH_{NT} + I_{CCD}(f) + I_{LOAD}$
 $I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ} \text{)}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input (} V_{IN} = 3.4V \text{)}$
 $DH = \text{Duty Cycle for TTL Inputs High}$
 $NT = \text{Number of TTL Inputs at } DH$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f = 2Q \text{ Frequency}$
 $I_{LOAD} = \text{Dynamic Current due to load.}$

SYNCH INPUT TIMING REQUIRMENTS

Symbol	Parameter	Min.	Max.	Unit
TRISE/FALL	Rise/Fall Times, SYNC inputs (0.8V to 2V)	—	3	ns
Frequency	Input Frequency, SYNC Inputs	10 ⁽¹⁾	2Q fmax	MHz
Duty Cycle	Input Duty Cycle, SYNC Inputs	25%	75%	—

OUTPUT FREQUENCY SPECIFICATIONS

Symbol	Parameter	Min.	Max. ⁽²⁾				Unit
			70	100	133 ⁽³⁾	150 ⁽³⁾	
f2Q	Operating frequency 2Q Output	40	70	100	133	150	MHz
fQ	Operating frequency Q0-Q4, $\overline{Q}5$ Outputs	20	35	50	66.7	75	MHz
fQ/2	Operating frequency Q/2 Output	10	17.5	25	33.3	37.5	MHz

NOTES:

- Note 7 in "General AC Specification Notes" and Figure 3 describes this specification and its actual limits depending on the feedback connection.
- Maximum operating frequency is guaranteed with the part in a phase locked condition and all outputs loaded.
- At this frequency, 2Q cannot be used as feedback.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (COMMERCIAL)

Symbol	Parameter	Condition ⁽¹⁾	Min.	Max.	Unit
t _{RISE/FALL} All Outputs	Rise/Fall Time (between 0.8V and 2V)	Load = 50Ω to V _{CC} /2, C _L = 20pF	0.2 ⁽²⁾	2	ns
t _{PULSE WIDTH} ⁽³⁾ Q, \bar{Q} , Q/2 outputs ⁽³⁾	Output Pulse Width Q0-Q4, $\bar{Q}5$, Q/2, @ 1.5V	Load = 50Ω to V _{CC} /2, C _L = 20pF	0.5t _{CYCLE} - 0.8 ⁽⁵⁾	0.5t _{CYCLE} + 0.8 ⁽⁵⁾	ns
t _{PULSE WIDTH} 2Q Output ⁽³⁾	Output Pulse Width 2Q @ 1.5V		0.5t _{CYCLE} - 1 ⁽⁵⁾	0.5t _{CYCLE} + 1 ⁽⁵⁾	ns
t _{PD} SYNC-FEEDBACK ⁽³⁾	SYNC input to FEEDBACK delay (measured at SYNC0 or 1 and FEEDBACK input pins)	Load = 50Ω to V _{CC} /2, C _L = 20pF 0.1μF from LF to Analog GND ⁽⁵⁾	+0.3	+1.3	ns
t _{SKEW} (rising) ^(3,4)	Output to Output Skew between outputs 2Q, Q0-Q4, Q/2 (rising edges only)	Load = 50Ω to V _{CC} /2, C _L = 20pF	—	600	ps
t _{SKEW} (falling) ^(3,4)	Output to Output Skew between outputs Q0-Q4 (falling edges only)		—	250	ps
t _{SKEW} ^(3,4)	Output to Output Skew 2Q, Q/2, Q0-Q4 rising, $\bar{Q}5$ falling		—	800	ps
t _{LOCK} ⁽⁶⁾	Time required to acquire Phase-Lock from time SYNC input signal is received		1 ⁽²⁾	10	ms
t _{PZH} t _{PZL}	Output Enable Time OE/ \overline{RST} (LOW-to-HIGH) to Q, 2Q, Q/2, \bar{Q}		3 ⁽²⁾	14	ns
t _{PHZ} t _{PLZ}	Output Disable Time OE/ \overline{RST} (HIGH-to-LOW) to Q, 2Q, Q/2, \bar{Q}		3 ⁽²⁾	14	ns

GENERAL AC SPECIFICATION NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested.
3. These specifications are guaranteed but not production tested.
4. Under equally loaded conditions, as specified under test conditions and at a fixed temperature and voltage.
5. t_{CYCLE} = 1/frequency at which each output (Q, \bar{Q} , Q/2 or 2Q) is expected to run.
6. With V_{CC} fully powered-on and an output properly connected to the FEEDBACK pin, t_{LOCK} Max. is with C₁ = 0.1μF, t_{LOCK} Min. is with C₁ = 0.01μF (where C₁ is loop filter capacitor shown in Figure 2).

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (INDUSTRIAL)

Symbol	Parameter	Condition ⁽¹⁾	Min.	Max.	Unit
t _{RISE/FALL} All Outputs	Rise/Fall Time (between 0.8V and 2V)	Load = 50Ω to V _{CC} /2, C _L = 20pF	0.2 ⁽²⁾	2	ns
t _{PULSE WIDTH} ⁽³⁾ Q, \bar{Q} , Q/2 outputs ⁽³⁾	Output Pulse Width Q0-Q4, \bar{Q} 5, @ 1.5V	Load = 50Ω to V _{CC} /2, C _L = 20pF	0.5t _{CYCLE} – 0.8 ⁽⁵⁾	0.5t _{CYCLE} + 0.8 ⁽⁵⁾	ns
t _{PULSE WIDTH} 2Q Output ⁽³⁾	Output Pulse Width 2Q, Q/2 @ 1.5V		0.5t _{CYCLE} – 1	0.5t _{CYCLE} + 1	ns
t _{PD} SYNC-FEEDBACK ⁽³⁾	SYNC input to FEEDBACK delay (measured at SYNC0 or 1 and FEEDBACK input pins)	Load = 50Ω to V _{CC} /2, C _L = 20pF 0.1μF from LF to Analog GND ⁽⁵⁾	0	1.3	ns
t _{SKEWR} (rising) ^(3,4)	Output to Output Skew between outputs 2Q, Q0-Q4, Q/2 (rising edges only)	Load = 50Ω to V _{CC} /2, C _L = 20pF	—	600	ps
t _{SKEWF} (falling) ^(3,4)	Output to Output Skew between outputs Q0-Q4 (falling edges only)		—	250	ps
t _{SKEWALL} ^(3,4)	Output to Output Skew 2Q, Q/2, Q0-Q4 rising, \bar{Q} 5 falling		—	800	ps
t _{LOCK} ⁽⁶⁾	Time required to acquire Phase-Lock from time SYNC input signal is received		1 ⁽²⁾	10	ms
t _{PZH} t _{PZL}	Output Enable Time OE/ \bar{RST} (LOW-to-HIGH) to Q, 2Q, Q/2, \bar{Q}	Load = 50Ω to V _{CC} /2, C _L = 20pF	3 ⁽²⁾	14	ns
t _{PHZ} t _{PLZ}	Output Disable Time OE/ \bar{RST} (HIGH-to-LOW) to Q, 2Q, Q/2, \bar{Q}		3 ⁽²⁾	14	ns

GENERAL AC SPECIFICATION NOTES:

- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested.
- These specifications are guaranteed but not production tested.
- Under equally loaded conditions, as specified under test conditions and at a fixed temperature and voltage.
- t_{CYCLE} = 1/frequency at which each output (Q, \bar{Q} , Q/2 or 2Q) is expected to run.
- With V_{CC} fully powered-on and an output properly connected to the FEEDBACK pin, t_{LOCK} Max. is with C₁ = 0.1μF, t_{LOCK} Min. is with C₁ = 0.01μF. (Where C₁ is loop filter capacitor shown in Figure 2).
- The wiring diagrams and written explanations of Figure 3 demonstrate the input and output frequency relationships for various possible feedback configurations. The allowable SYNC input range to stay in the phase-locked condition is also indicated. There are two allowable SYNC frequency ranges, depending on whether FREQ_SEL is HIGH or LOW. Also it is possible to feed back the \bar{Q} 5 output, thus creating a 180° phase shift between the SYNC input and the Q outputs. The table below summarizes the allowable SYNC frequency range for each possible configuration.

FREQ_SEL Level	Feedback Output	Allowable SYNC Input Frequency Range (MHZ)	Corresponding 2Q Output Frequency Range	Phase Relationship of the Q Outputs to Rising SYNC Edge
HIGH	Q/2	10 to (2x_Q f _{MAX} Spec)/4	40 to (2Q f _{MAX} Spec)	0°
HIGH	Any Q (Q0-Q4)	20 to (2x_Q f _{MAX} Spec)/2	40 to (2Q f _{MAX} Spec)	0°
HIGH	\bar{Q} 5	20 to (2x_Q f _{MAX} Spec)/2	40 to (2Q f _{MAX} Spec)	180°
HIGH	2X_Q	40 to (2x_Q f _{MAX} Spec)	40 to (2Q f _{MAX} Spec)	0°
LOW	Q/2	5 to (2x_Q f _{MAX} Spec)/8	20 to (2Q f _{MAX} Spec)/2	0°
LOW	Any Q (Q0-Q4)	10 to (2x_Q f _{MAX} Spec)/4	20 to (2Q f _{MAX} Spec)/2	0°
LOW	\bar{Q} 5	10 to (2x_Q f _{MAX} Spec)/4	20 to (2Q f _{MAX} Spec)/2	180°
LOW	2X_Q	20 to (2x_Q f _{MAX} Spec)/2	20 to (2Q f _{MAX} Spec)/2	0°

GENERAL AC SPECIFICATION NOTES (continued):

8. The tPD spec describes how the phase offset between the SYNC input and the output connected to the FEEDBACK input, varies with process, temperature and voltage. The phase measurements were made at 1.5V. The Q/2 output was terminated at the FEEDBACK input with 100Ω to V_{CC} and 100Ω to ground. tPD measurements were made with the loop filter connection shown in Figure 1 below:

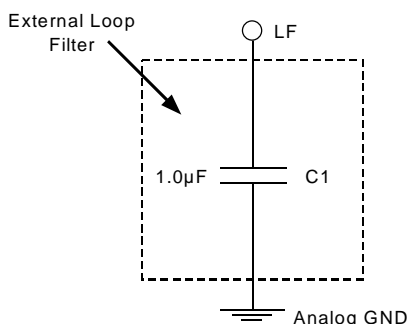


Figure 1

NOTES:

1. Figure 2 shows a loop filter and analog isolation scheme which will be effective in most applications. The following guidelines should be followed to ensure stable and jitter-free operation:

- All loop filter and analog isolation components should be tied as close to the package as possible. Stray current passing through the parasitics of long traces can cause undesirable voltage transients at the LF pin.
- The 10µF low frequency bypass capacitor and the 0.1µF high frequency bypass capacitor form a wide bandwidth filter that will minimize the 388915T's sensitivity to voltage transients from the system digital V_{CC} supply and ground planes.
 If good bypass techniques are used on a board design near components which may cause digital V_{CC} and ground noise, V_{CC} step deviations should not occur at the 388915T's digital V_{CC} supply. The purpose of the bypass filtering scheme shown in figure 2 is to give the 388915T additional protection from the power supply and ground plane transients that can occur in a high frequency, high speed digital system.
- The loop filter capacitor (0.1µF) can be a ceramic chip capacitor, the same as a standard bypass capacitor.

2. In addition to the bypass capacitors used in the analog filter of Figure 2 there should be a 0.1µF bypass capacitor between each of the other (digital) four V_{CC} pins and the board ground plane. This will reduce output switching noise caused by the 388915T outputs, in addition to reducing potential for noise in the "analog" section of the chip. These bypass capacitors should also be tied as close to the 388915T package as possible.

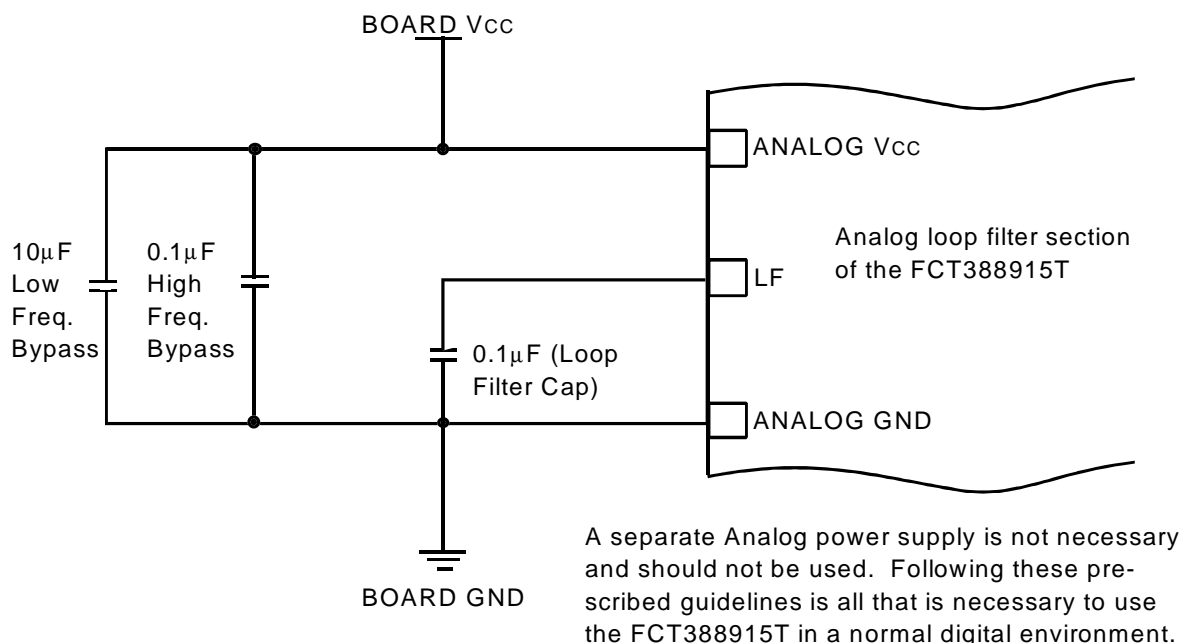
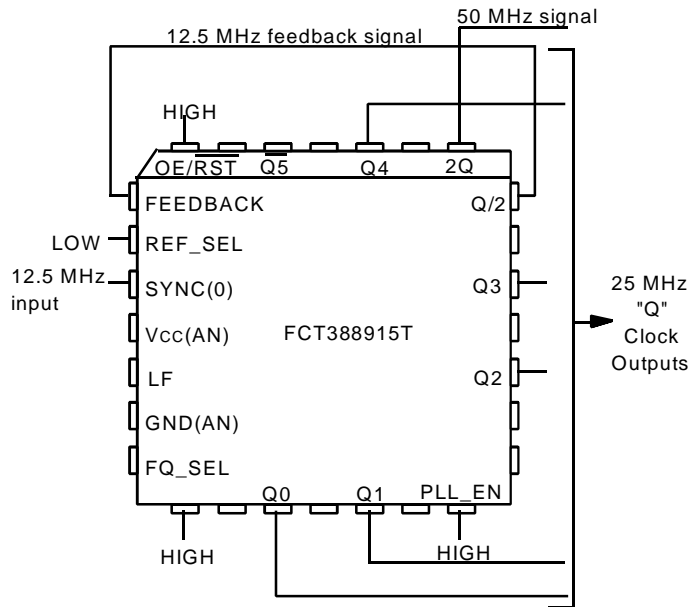


Figure 2. Recommended Loop Filter and Analog Isolation Scheme for the FCT388915T

The frequency relationship shown here is applicable to all Q outputs (Q0, Q1, Q2, Q3 and Q4).

1:2 INPUT TO "Q" OUTPUT FREQUENCY RELATIONSHIP

In this application, the Q/2 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q/2 and SYNC, thus the Q/2 frequency will equal the SYNC frequency. The Q outputs (Q0-Q4, Q5) will always run at 2X the Q/2 frequency, and the 2Q output will run at 4X the Q/2 frequency.

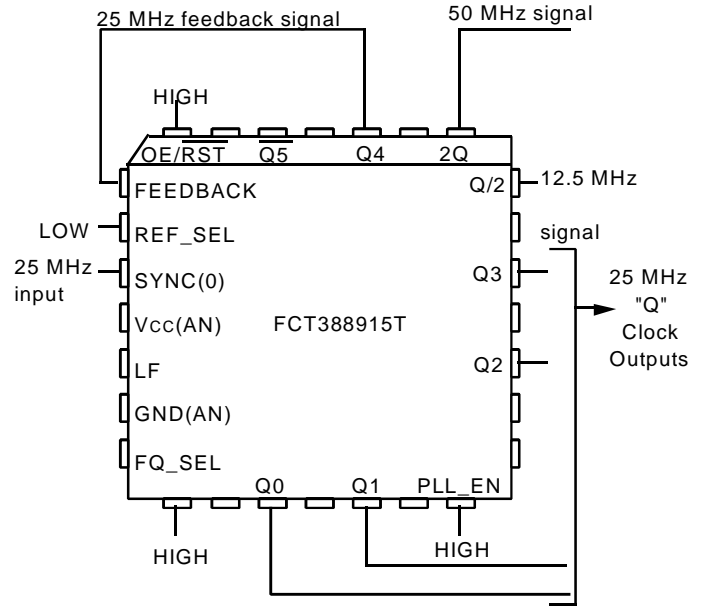


Allowable Input Frequency Range:
 10MHz to (f2Q MAX Spec)/4 (for FREQ_SEL HIGH)
 5MHz to (f2Q MAX Spec)/8 (for FREQ_SEL LOW)

Figure 3a. Wiring Diagram and Frequency Relationships With Q/2 Output Feedback

1:1 INPUT TO "Q" OUTPUT FREQUENCY RELATIONSHIP

In this application, the Q4 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q4 and SYNC, thus the Q4 frequency (and the rest of the "Q" outputs) will equal the SYNC frequency. The Q/2 output will always run at 1/2 the Q frequency, and the 2Q output will run at 2X the Q frequency.

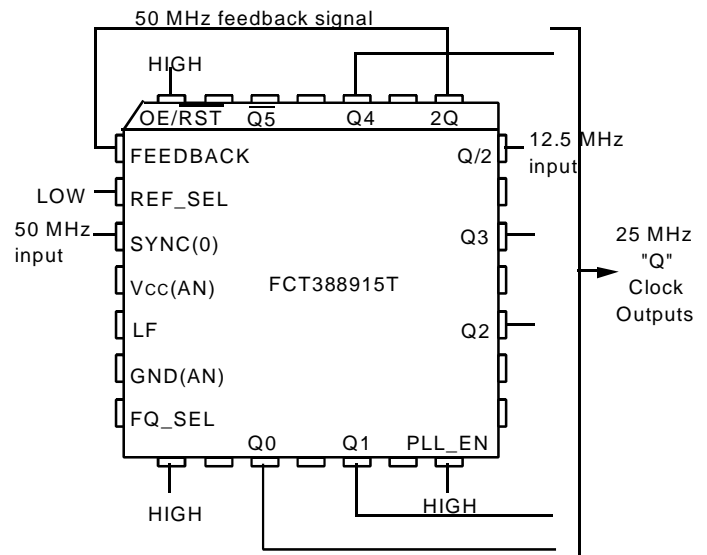


Allowable Input Frequency Range:
 20MHz to (f2Q MAX Spec)/2 (for FREQ_SEL HIGH)
 10MHz to (f2Q MAX Spec)/4 (for FREQ_SEL LOW)

Figure 3b. Wiring Diagram and Frequency Relationships With Q4 Output Feedback

2:1 INPUT TO "Q" OUTPUT FREQUENCY RELATIONSHIP

In this application, the 2Q output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of 2Q and SYNC, thus the 2Q frequency will equal the SYNC frequency. The Q/2 output will always run at 1/4 the 2Q frequency, and the Q output will run at 1/2 the 2Q frequency.



Allowable Input Frequency Range:
 40MHz to (f2Q MAX Spec) (for FREQ_SEL HIGH)
 20MHz to (f2Q MAX Spec)/2 (for FREQ_SEL LOW)

Figure 3c. Wiring Diagram and Frequency Relationships With 2Q Output Feedback

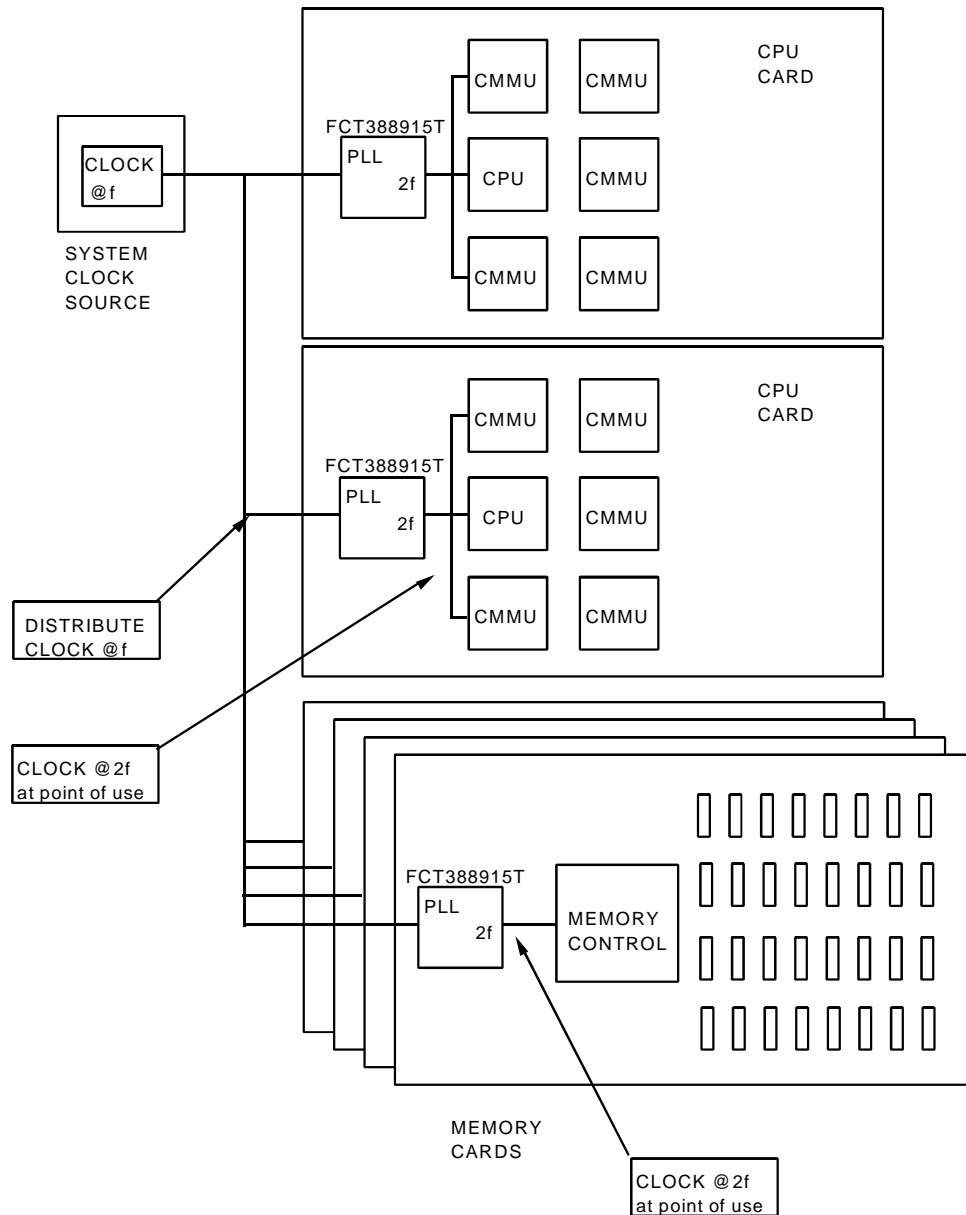


Figure 4. Multiprocessing Application Using the FCT388915T for Frequency Multiplication and Low Board-to-Board skew

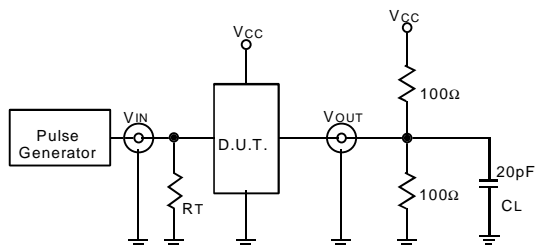
FCT388915T System Level Testing Functionality

When the PLL_EN pin is LOW, the PLL is bypassed and the FCT388915T is in low frequency "test mode". In test mode (with FREQ_SEL HIGH), the 2Q output is inverted from the selected SYNC input, and the Q outputs are divide-by-2 (negative edge triggered) of the SYNC input, and the Q/2 output is divide-by-4 (negative edge triggered). With FREQ_SEL LOW the 2Q output is divide-by-2 of the SYNC, the Q outputs divide-by-4, and the Q/2 output divide-by-8.

These relationships can be seen in the block diagram. A recommended test configuration would be to use SYNC0 or SYNC1 as the test clock input, and tie PLL_EN and REF_SEL together and connect them to the test select logic.

This functionality is needed since most board-level testers run at 1 MHz or below, and the FCT 388915T cannot lock onto that low of an input frequency. In the test mode described above, any test frequency test can be used.

50Ω TO $V_{CC}/2$, $C_L = 20PF$



The diagram shows a central block labeled 'D.U.T.' (Device Under Test). Its input is labeled V_{IN} and its output is labeled V_{OUT} . The input side has a 'Pulse Generator' connected to V_{IN} . A resistor R_T is connected between V_{IN} and ground. The output side has a resistor connected between V_{OUT} and ground, and another resistor connected between V_{OUT} and a 6.0V source. A ground symbol is also shown near the 6.0V source.

Timing diagram for the 74VHC04 inverter. The diagram shows the relationship between the SYNC input, feedback input, and various outputs (Q/2, Q0-Q4, Q5, 2Q) over one cycle. Key timing parameters are labeled: t_{PD} (propagation delay), $t_{CYCLE\ SYNC\ INPUT}$ (sync input cycle), t_{SKEWf} (fall skew), t_{SKEWr} (rise skew), and $t_{CYCLE\ "Q"\ OUTPUTS}$ (output cycle). Voltage levels are indicated as 1.5V, $V_{CC}/2$, and V_{CC} .

NOTES:

1. The FCT388915T aligns rising edges of the FEEDBACK input and SYNC input, therefore the SYNC input does not require a 50% duty cycle.
2. All skew specs are measured between the $V_{CC}/2$ crossing point of the appropriate output edges. All skews are specified as "windows", not as \pm deviation around a center point.
3. If a Q output is connected to the FEEDBACK input (this situation is not shown), the Q output frequency would match the SYNC input frequency, the 2Q output would run at twice the SYNC frequency and the Q/2 output would run at half the SYNC frequency.

Test	Switch
Disable Low Enable Low	6V
Disable High Enable High	GND

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: $t_F \leq 2.5\text{ns}$; $t_R \leq 2.5\text{ns}$.

ORDERING INFORMATION

IDT74FCT	XXXX	XX	XX	X		
	Device Type	Speed	Package	Process		
				Blank		Commercial (0° to +70°C)
				I		Industrial (–40° to +85°C)
				J		PLCC (J28-1)
				PY		SSOP (SO28-7)
				70		70MHz Max. Frequency
				100		100MHz Max. Frequency
				133		133MHz Max. Frequency
				150		150MHz Max. Frequency
				388915T		3.3V Low skew PLL-based CMOS clock driver