MOTOROLA

MC14504B

CMOS SSI

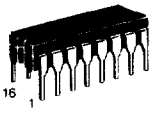
(LOW-POWER COMPLEMENTARY MOS)

TTL or CMOS to CMOS HEX LEVEL SHIFTER

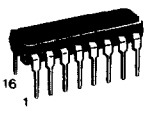
HEX LEVEL SHIFTER FOR TTL to CMOS or CMOS to CMOS

The MC14504B is a hex non-inverting level shifter using CMOS technology. The level shifter will shift a TTL signal to CMOS logic levels for any CMOS supply voltage between 5 and 15 volts. A control input also allows interface from CMOS to CMOS at one logic level to another logic level. Either up or down level translating is accomplished by selection of power supply levels V_{DD} and V_{CC}. The V_{CC} level sets the input signal levels while V_{DD} selects the output voltage levels.

- UP Translates from a Low to a High Voltage or DOWN Translates from a High to a Low Voltage
- Input Threshold Can Be Shifted for TTL Compatibility
- No Sequencing Required on Power Supplies or Inputs for Power Up or Power Down
- 3 to 18 Vdc Operation for V_{DD} and V_{CC}
- Diode Protected Inputs to V_{SS}
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620



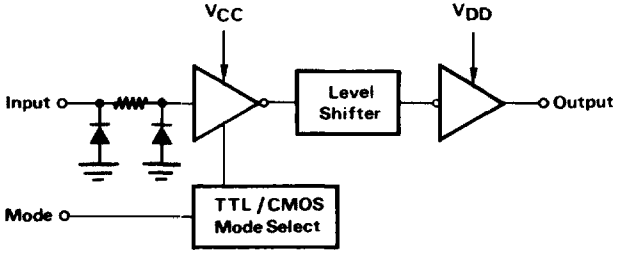
P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

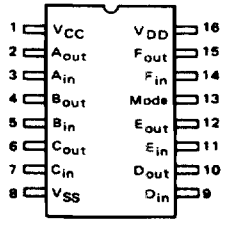
LOGIC DIAGRAM



Mode Select	Input Logic Levels	Output Logic Levels
1 (V_{CC})	TTL	CMOS
0 (V_{SS})	CMOS	CMOS

1/6 of package shown.

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields **referenced to the V_{SS} pin, only.** Extra precautions must be taken to avoid applications of any voltage higher than the maximum rated voltages to this high-impedance circuit. For proper operation, the ranges $V_{SS} \leq V_{in} \leq 18$ V and $V_{SS} \leq V_{out} \leq V_{DD}$ are recommended.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	−0.5 to +18.0	V
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}	Input Voltage (DC or Transient)	−0.5 to +18.0	V
V_{out}	Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package**	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum ratings are those values beyond which damage to the device may occur.
**Power dissipation temperature derating: Plastic "P" package: −12 mW/°C from 65°C to 85°C. Ceramic "L" package: −12 mW/C° from 100°C to 125°C.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{CC} Vdc	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	–	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = 0 V		–	10	–	0.05	–	0	0.05	–	0.05	
		–	15	–	0.05	–	0	0.05	–	0.05	
V_{in} = V_{CC} "1" Level	V_{OH}	–	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		–	10	9.95	–	9.95	10	–	9.95	–	
		–	15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}										Vdc
(V_{OL} = 1.0 Vdc) TTL–CMOS		5	10	–	0.8	–	1.3	0.8	–	0.8	
(V_{OL} = 1.5 Vdc) TTL–CMOS		5	15	–	0.8	–	1.3	0.8	–	0.8	
(V_{OL} = 1.0 Vdc) CMOS–CMOS		5	10	–	1.5	–	2.25	1.5	–	1.4	
(V_{OL} = 1.5 Vdc) CMOS–CMOS		5	15	–	1.5	–	2.25	1.5	–	1.5	
(V_{OL} = 1.5 Vdc) CMOS–CMOS		10	15	–	3.0	–	4.5	3.0	–	2.9	
Input Voltage "1" Level	V_{IH}										Vdc
(V_{OH} = 9.0 Vdc) TTL–CMOS		5	10	2.0	–	2.0	1.5	–	2.0	–	
(V_{OH} = 13.5 Vdc) TTL–CMOS		5	15	2.0	–	2.0	1.5	–	2.0	–	
(V_{OH} = 9.0 Vdc) CMOS–CMOS		5	10	3.6	–	3.5	2.75	–	3.5	–	
(V_{OH} = 13.5 Vdc) CMOS–CMOS		5	15	3.6	–	3.5	2.75	–	3.5	–	
(V_{OH} = 13.5 Vdc) CMOS–CMOS		10	15	7.1	–	7.0	5.5	–	7.0	–	
Output Drive Current (AL Device)	I_{OH}										mAdc
(V_{OH} = 2.5 Vdc) Source		–	5.0	-3.0	–	−2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		–	5.0	-0.64	–	−0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		–	10	-1.6	–	−1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		–	15	-4.2	–	−3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	–	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		–	10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		–	15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}										mAdc
(V_{OH} = 2.5 Vdc) Source		–	5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		–	5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		–	10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		–	15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	–	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		–	10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		–	15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL)	I_{in}	–	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP)	I_{in}	–	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD} or	–	5.0	–	0.05	–	0.0005	0.05	–	1.5	μAdc
(Per Package)	I_{CC}	–	10	–	0.10	–	0.0010	0.10	–	3.0	
CMOS–CMOS Mode		–	15	–	0.20	–	0.0015	0.20	–	6.0	
Quiescent Current (CL/CP Device)	I_{DD} or	–	5.0	–	0.5	–	0.0005	0.5	–	3.8	μAdc
(Per Package)	I_{CC}	–	10	–	1.0	–	0.0010	1.0	–	7.5	
CMOS–CMOS Mode		–	15	–	2.0	–	0.0015	2.0	–	15.0	
Quiescent Current (AL/CL/CP Device)	I_{DD}	5.0	5.0	–	0.5	–	0.0005	0.5	–	3.8	μAdc
(Per Package)		5.0	10	–	1.0	–	0.0010	1.0	–	7.5	
TTL–CMOS Mode		5.0	15	–	2.0	–	0.0015	2.0	–	15.0	
Quiescent Current (AL/CL/CP Device)	I_{CC}	5.0	5.0	–	5.0	–	2.5	5.0	–	6.0	mAdc
(Per Package)		5.0	10	–	5.0	–	2.5	5.0	–	6.0	
TTL–CMOS Mode		5.0	15	–	5.0	–	2.5	5.0	–	6.0	

*T_{LOW} = −55°C for AL Device, −40°C for CL/CP Device
T_{HIGH} = +125°C for AL Device, +85°C for CL/CP Device

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

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SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	Shifting Mode	V_{CC} Vdc	V_{DD} Vdc	Limits Min	Limits Typ #	Limits Max	Units
Propagation Delay, High to Low	t_{PHL}	TTL–CMOS	5.0	10	–	140	280	ns
		$V_{DD} > V_{CC}$	5.0	15	–	140	280	
		CMOS–CMOS	5.0	10	–	120	240	
		$V_{DD} > V_{CC}$	5.0	15	–	120	240	
			10	15	–	70	140	
		CMOS–CMOS	10	5.0	–	185	370	
		$V_{CC} > V_{DD}$	15	5.0	–	185	370	
			15	10	–	175	350	
Propagation Delay, Low to High	t_{PLH}	TTL–CMOS	5.0	10	–	170	340	ns
		$V_{DD} > V_{CC}$	5.0	15	–	160	320	
		CMOS–CMOS	5.0	10	–	170	340	
		$V_{DD} > V_{CC}$	5.0	15	–	170	340	
			10	15	–	100	200	
		CMOS–CMOS	10	5.0	–	275	550	
		$V_{CC} > V_{DD}$	15	5.0	–	275	550	
			15	10	–	145	290	
Output Rise and Fall Time	t_{TLH}, t_{THL}	ALL	–	5.0	–	100	200	ns
			–	10	–	50	100	
			–	15	–	40	80	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance

FIGURE 1 – INPUT SWITCHPOINT CMOS to CMOS MODE

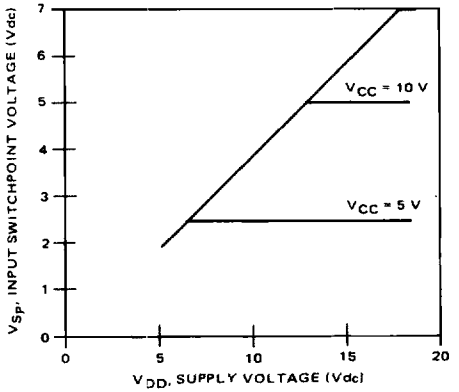


FIGURE 2 – INPUT SWITCHPOINT TTL to CMOS MODE

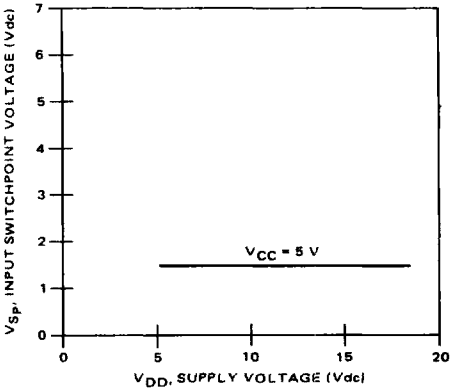


FIGURE 3 – OPERATING BOUNDARY CMOS to CMOS MODE

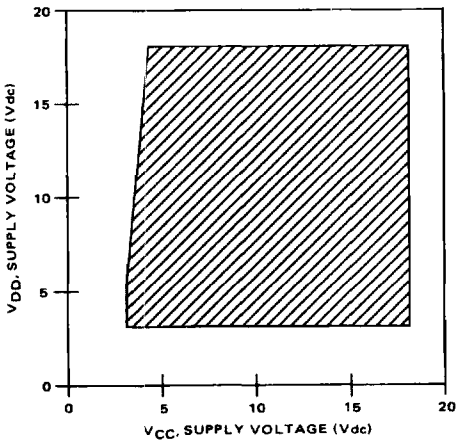
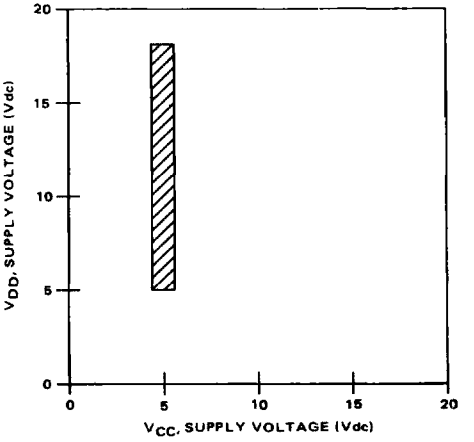


FIGURE 4 – OPERATING BOUNDARY TTL to CMOS MODE



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