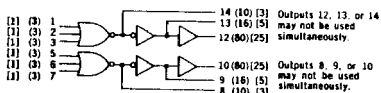


# MC788P • MC888P

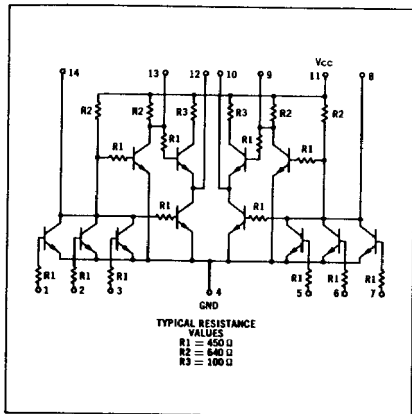
Two 3-input positive logic NOR gates, each followed by an inverting and non-inverting high fan-out amplifier, are provided in a single package. For each section, the output from each stage is available. If more than one output is used, the full loading factors cannot be employed since each output provides the drive for the succeeding stage.



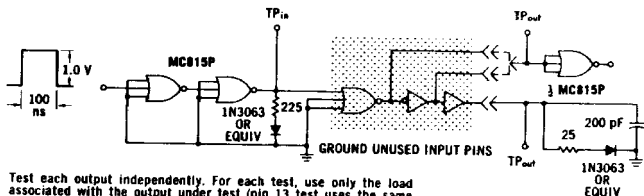
14 = 1 + 2 + 3    13 = 1 + 2 + 3    12 = 1 + 2 + 3

NUMBER IN PARENTHESES INDICATES LOADING FACTOR FOR mW MRTL  
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MRTL

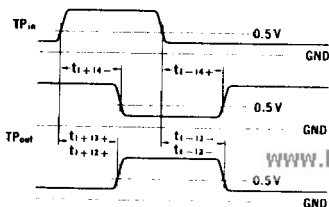
$t_{pd} = 24 \text{ ns}$   
 $P_o = 145 \text{ mW (Input Low)}$   
 $56 \text{ mW (Inputs Low)}$



## SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



Test each output independently. For each test, use only the load associated with the output under test (pin 13 test uses the same load as pin 14 test). Outputs not under test should be left open.



## ELECTRICAL CHARACTERISTICS

Test procedures are shown for one buffer only.  
The other buffer is tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC888P Test Limits						MC788P Test Limits						TEST VOLTAGE						Gnd				
			0°C		+25°C		+75°C		+15°C		+25°C		+55°C		APPLIED TO PINS LISTED BELOW:										
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	V <sub>in</sub>	V <sub>out</sub>	V <sub>err</sub>	V <sub>cc</sub>	V <sub>in</sub> *	V <sub>out</sub> *					
Input Current	I <sub>in</sub>	1	-	600	-	600	-	570	μAdc	↑	-	500	-	500	-	470	μAdc	↑	1	2,3	11	-	4		
		2	-	↓	-	↓	-	↓	↑	↑	-	↓	-	↓	-	↓	↑	↑	2	1,3	-	-	-		
		3	-	↓	-	↓	-	↓	↑	↑	-	↓	-	↓	-	↓	↑	↑	3	1,2	-	-	-		
Output Current	I <sub>AB</sub>	12	15.0	-	15.0	-	14.25	-	mAdc	13.50	-	13.75	-	12.50	-	-	mAdc	-	12	-	14	11	-	4	
	I <sub>A5</sub>	13	3.0	-	3.0	-	2.85	-	↑	2.65	-	2.65	-	2.50	-	-	mAdc	-	13	-	14	↑	-	-	
	I <sub>A3</sub>	14	1.8	-	1.8	-	1.71	-	-	-	-	-	-	-	-	-	-	-	14	-	1,2,3	↑	-	-	
	V <sub>out</sub>	12	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	↑	↑	14	-	-	11	12	1,2,3,4	
Output Voltage	V <sub>out</sub>	13	-	↑	-	↑	-	↑	↑	↑	-	↑	-	↑	-	↑	↑	↑	14	-	-	-	-	1,2,3,4	
		14	-	↑	-	↑	-	↑	↑	↑	-	↑	-	↑	-	↑	↑	↑	1	-	-	-	-	1,2,3,4	
		14	-	↑	-	↑	-	↑	↑	↑	-	↑	-	↑	-	↑	↑	↑	2	-	-	-	-	1,3,4	
		14	-	↑	-	↑	-	↑	↑	↑	-	↑	-	↑	-	↑	↑	↑	3	-	-	-	-	1,2,4	
Saturation Voltage	V <sub>CE(sat)</sub>	12	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	↑	↑	-	14	-	11	12	1,2,3,4	
		13	-	↑	-	↑	-	↑	↑	↑	-	↑	-	↑	-	↑	↑	↑	14	-	-	-	-	1,2,3,4	
		14	-	↑	-	↑	-	↑	↑	↑	-	↑	-	↑	-	↑	↑	↑	1	-	-	-	-	2,3,4	
		14	-	↑	-	↑	-	↑	↑	↑	-	↑	-	↑	-	↑	↑	↑	2	-	-	-	-	1,3,4	
Switching Time	t	1+12+	-	-	-	-	65	-	-	-	-	65	-	-	-	-	-	-	-	-	-	-	-	-	1,2,3,4
		1-12+	-	-	-	-	58	-	-	-	-	58	-	-	-	-	-	-	-	-	-	-	-	-	1,2,3,4
		1+13+	-	-	-	-	42.5	-	-	-	-	42.5	-	-	-	-	-	-	-	-	-	-	-	-	1,2,3,4
		1-13+	-	-	-	-	42.5	-	-	-	-	42.5	-	-	-	-	-	-	-	-	-	-	-	-	-
Pulse	In	1	-	-	-	20	-	-	-	-	20	-	-	-	-	-	-	-	-	-	-	-	-	-	1,2,3,4
		14	-	-	-	28	-	-	-	-	28	-	-	-	-	-	-	-	-	-	-	-	-	-	1,2,3,4
Pulse	Out	1	-	-	-	12	-	-	-	-	12	-	-	-	-	-	-	-	-	-	-	-	-	-	1,2,3,4
		14	-	-	-	13	-	-	-	-	13	-	-	-	-	-	-	-	-	-	-	-	-	-	1,2,3,4

Ground input pins of buffer not under test. Other pins not listed are left open. \*Resistor value to V<sub>CC</sub>