512K x 8 SRAM MODULE

SYS8512FKX-70/85/10/12

Issue 5.0: November 1999

Description

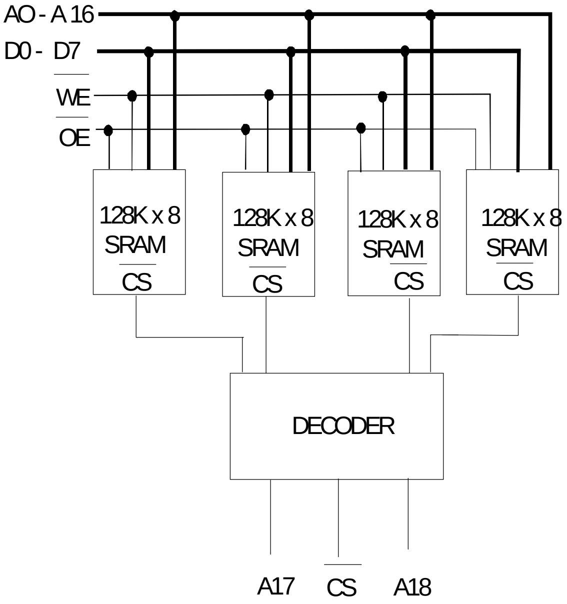
The SYS8512FKX is plastic 4M Static RAM Module housed in a standard 32 pin Dual-In-Line package organised as 512K x 8. The module utilises fast SRAMs housed in TSOP packages, and uses double sided surface mount techniques, buried decoder and dual board construction to achieve a very high density module.

The module has Chip Select, Write Enable and Output Enable control inputs; the Output Enable pin allows faster access times than address access during a Read Cycle.

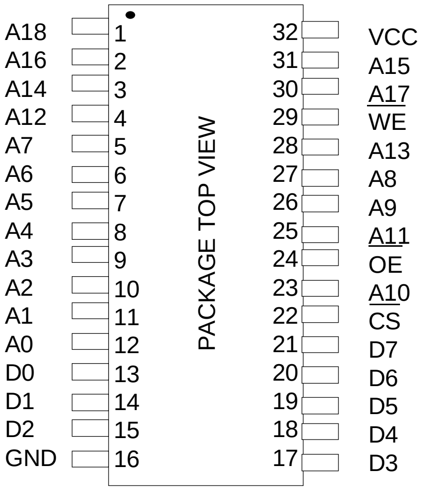
Features

- Access Times of 70/85/100/120 ns.
- Low seated height
- 32 Pin 0.6" Dual-In-Line package with JEDEC compatible pinout.
- 5 Volt Supply ± 10%.
- Low Power Dissipation:
  - Average (min cycle) 605mW (maximum).
  - Standby (CMOS) 44mW (maximum).
- Completely Static Operation.
- Equal Access and Cycle Times.
- All Inputs and Outputs Directly TTL Compatible.
- On-board Supply Decoupling Capacitors.

Block Diagram



Pin Definition



Pin Functions

Address Inputs	**A0 - A18**
Data Input/Output	**D0 - D7**
Chip Select Input	**CS**
Read/Write Input	**WE**
Output Enable Input	**OE**
Power (+5V)	**V_{CC}**
Ground	**GND**

DC OPERATING CONDITIONS

Absolute Maximum Ratings (1)

Parameter	*Symbol*	*min*	*typ*	*max*	*unit*
Voltage on any pin relative to V_{SS}	V_T	-0.3V	-	+7	V
Power Dissipation	P_T	-	1	-	W
Storage Temperature	T_{STG}	-55	-	+150	°C

Notes :

(1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) V_t can be -3.5V pulse of less than 20ns.

Recommended Operating Conditions

Parameter	*Symbol*	*min*	*typ*	*max*	*unit*
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	-	Vcc + 0.3	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (I)

DC Electrical Characteristics (V_{CC}=5V±10%) TA 0 to 70°C

*Pa*rameter		Symbol	Test Condition	min	typ[2]	max	Unit
I/P Leakage Current	A0~A16, $\overline{OE}$	I_{LI1}	0V - V_{IN} - V_{CC}	-	-	±8	µA
Output Leakage Current	D0~D7	I_{LO}	$\overline{CS}$ = $V_{IH,}$ $V_{I/O}$ = GND to V_{CC}	-	-	±8	µA
Operating Supply Current		I_{CC}	$\overline{CS}$ = V_{IL} ,$I_{I/O}$ = 0mA, V_{IL} - V_{IN} - V_{CC}-2.1V	-	16	45	mA
Average Supply Current	TTL levels	I_{CC1}	Min. Cycle, $\overline{CS}$ = V_{IL}, V_{IN} = V_{IL}/V_{CC}-2.1V	-	70	110	mA
	CMOS levels	I_{CC2}	Min. Cycle, $\overline{CS}$ - 0.2V, V_{IN} = 0.2V/V_{CC}-0.2V	-	24	40	mA
Standby Supply Current	TTL levels	I_{SB}	$\overline{CS}$,A17-A18 = V_{CC}-2.1V, V_{IL} - V_{IN} - V_{CC}-2.1V	-	5	12	mA
	CMOS levels	I_{SB1}	$\overline{CS}$,A17-A18 = V_{CC}-0.2V, 0.2 - V_{IN} - V_{CC}-0.2V	-	0.2	8	mA
	-L Part	I_{SB2}	As above	-	10	500	µA
Output Voltage		V_{OL}	I_{OL} = 2.1mA	-	-	0.4	V
		V_{OH}	I_{OH} = -1.0mA	2.4	-	-	V

Typical values are at V_{CC}=5.0V,T_A=25°C and specified loading.

Capacitance (V_{CC}=5V±10%,T_A=25°C) Note: Capacitance calculated, not measured.

Parameter	*Symbol*	*Test Condition*	*max*	*Unit*
Input Capacitance ($\overline{CS}$, A17, A18)	C_{IN1}	V_{IN} = 0V	10	pF
I/P Capacitance (other)	C_{IN2}	V_{IN} = 0V	40	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	40	pF

Operation Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	*DATA PINS*	*SUPPLY CURRENT*	*MODE*
H	X	X	High Impedance	I_{SB1} , I_{SB2}	Standby
L	L	H	Data Out	I_{CC1} , I_{CC2}	Read
L	L	L	Data In	I_{CC1} , I_{CC2}	Write
L	H	L	Data In	I_{CC1} , I_{CC2}	Write

Notes : H = V_{IH} : L =V_{IL} : X = V_{IH} or V_{IL}

Low V_{cc} Data Retention Characteristics - L Version Only

			-L Part						
Parameter	*Symbol*	*Test Condition*	*min*	*typ*[(1)]	*max*				
V_{CC} for Data Retention	V_{DR}	$\overline{CS}$ - V_{CC}-0.2V	2.0	-	-				
Data Retention Current		V_{CC} = 3.0V, $\overline{CS}$ = V_{CC}-0.2V							
	I_{CCDR2}	T_{OP} = 0C to 70C	-	9	230		µA		
	I_{CCDR3}	T_{OP} = T_{AI}	-	-	310		µA		
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	5	-	-	0	-	-	ms

Notes (1) Typical figures are measured at 25°C.

(2) This parameter is guaranteed not tested.

AC Test Conditions Output Load

- * Input pulse levels: 0V to 3.0V
- * Input rise and fall times: 5ns
- * Input and Output timing reference levels: 1.5V
- * Output load: see diagram
- * V_{CC}=5V±10%

AC OPERATING CONDITIONS

Read Cycle

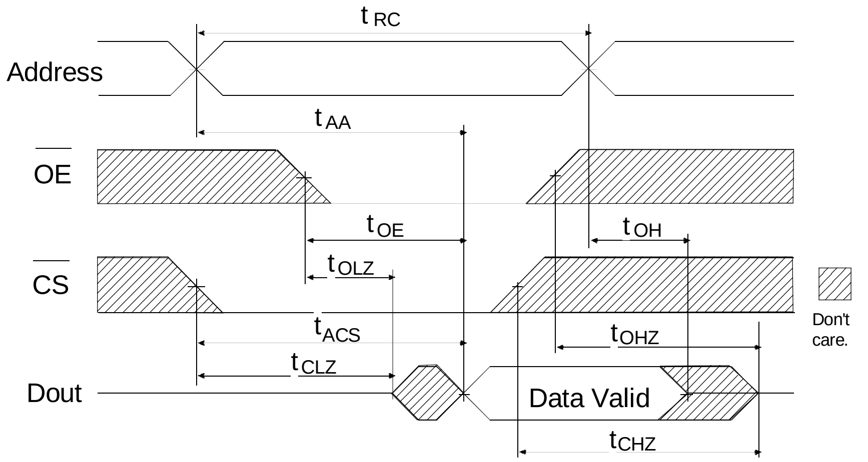
Parameter	*Symbol*	*-70* *min*	*-70* *max*	*-85* *min*	*-85* *max*	*-10* *min*	*-10* *max*	*-12* *min*	*-12* *max*	*Unit*
Read Cycle Time	t_{RC}	70	-	85	-	100	-	120	-	ns
Address Access Time	t_{AA}	-	70	-	85	-	100	-	120	ns
Chip Select Access Time	t_{ACS}	-	70	-	85	-	100	-	120	ns
Output Enable to Output Valid	t_{OE}	-	50	-	55	-	60	-	70	ns
Output Hold from Address Change	t_{OH}	10	-	10	-	10	-	10	-	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	-	10	-	10	-	10	-	ns
Output Enable to Output in Low Z	t_{OLZ}	5	-	5	-	5	-	5	-	ns
Chip Deselection to O/P in High Z	t_{CHZ}	0	25	0	30	0	35	0	45	ns
Output Disable to Output in High Z	t_{OHZ}	0	25	0	30	0	35	0	45	ns

Notes. (1) t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels.These parameters are sampled and not 100% tested.

Write Cycle

Parameter	*Sym*	*-70* *min*	*-70* *max*	*-85* *min*	*-85* *max*	*-10* *min*	*-10* *max*	*-12* *min*	*-12* *max*	*Unit*
Write Cycle Time	t_{WC}	70	-	85	-	100	-	120	-	ns
Chip Selection to End of Write	t_{CW}	60	-	80	-	90	-	100	-	ns
Address Valid to End of Write	t_{AW}	60	-	80	-	90	-	100	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	55	-	65	-	75	-	85	-	ns
Write Recovery Time	t_{WR}	5	-	5	-	10	-	10	-	ns
Write to Output in High Z	t_{WHZ} (11)	0	25	0	30	0	35	0	40	ns
Data to Write Time Overlap	t_{DW}	30	-	35	-	40	-	45	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	0	-	ns
Output active from end of write	t_{OW} (10)	5	-	5	-	5	-	5	-	ns

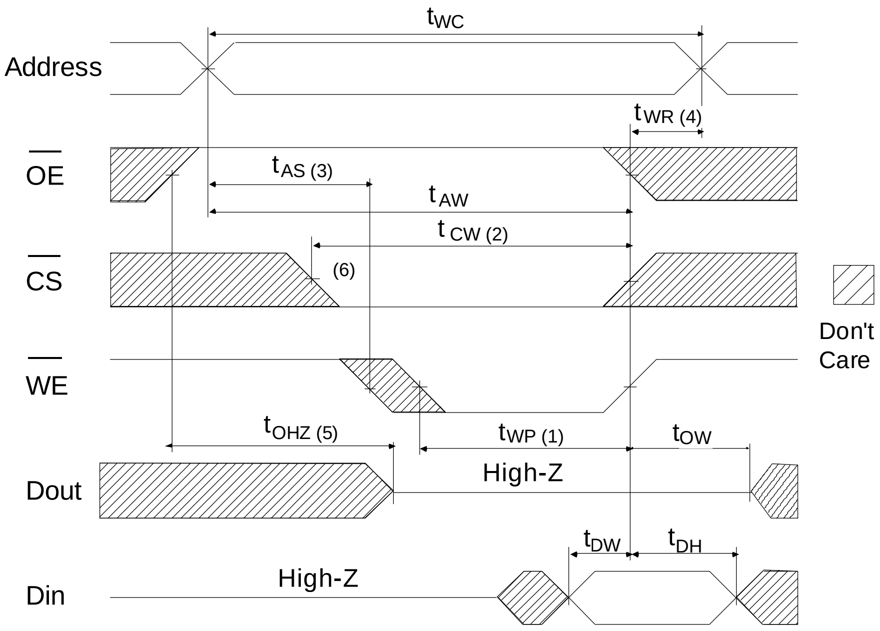
Read Cycle Timing Waveform (1,2)



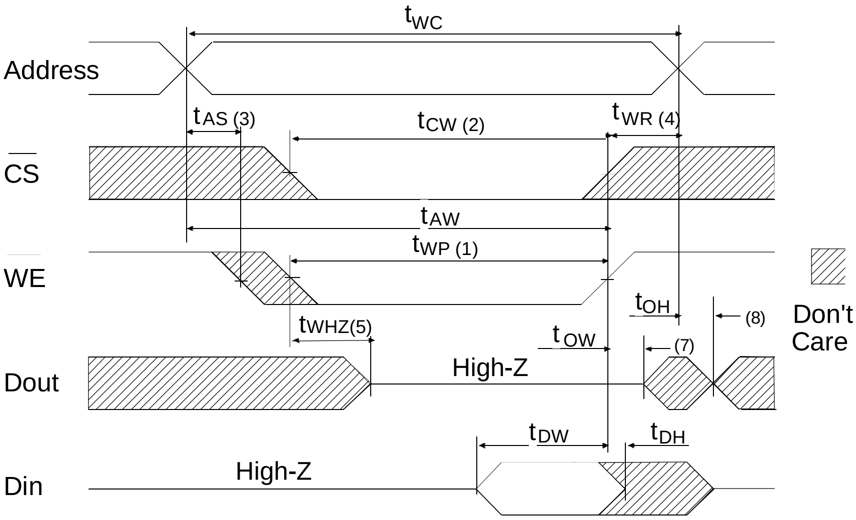
Notes (1) WE is High for Read Cycle.

(2) t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels.These parameters are sampled and not 100% tested.

Write Cycle No.1 Timing Waveform



Write Cycle No.2 Timing Waveform



AC Characteristics Notes

(1) A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.

(2) t_{CW} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

(3) t_{AS} is measured from the address valid to the beginning of write.

(4) t_{WR} is measured from the earliest of $\overline{CS}$ or $\overline{WE}$ going high to the end of write.

(5) During this period, I/O pins are in the output state. Input signals out of phase must not be applied.

(6) If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low , outputs remain in a high impedance state.

(7) D_{OUT} is in the same phase as written data of this write cycle.

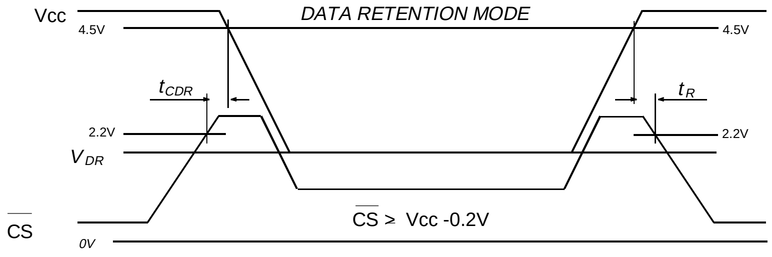
(8) D_{OUT} is the read data of next address.

(9) If $\overline{CS}$ is low during this period, I/O pins are in the output state, and inputs out of phase must not be applied to I/O pins.

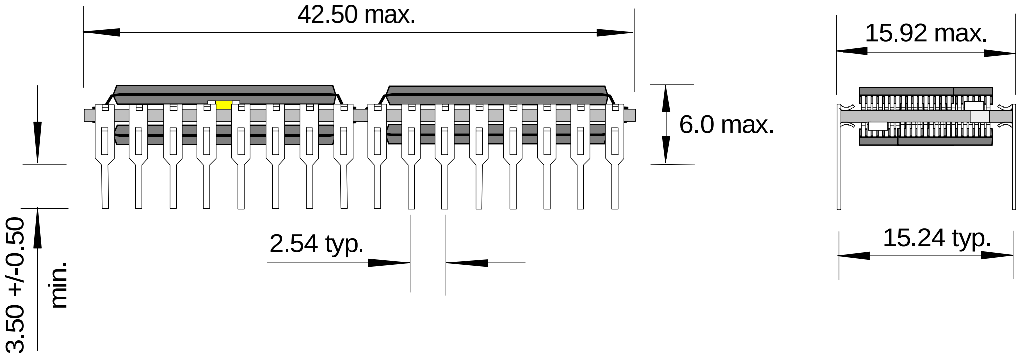
(10) This parameter is sampled and not 100% tested.

(11) t_{WHZ} is defined as the time at which the outputs achieve open circuit conditions and is not referenced to output voltage levels. This parameter is sampled and not 100% tested.

Data Retention Waveform



Package Information



Dimensions in mm

Ordering Information

SYS8512FKXLI-10

Speed	70	= 70 ns
	85	= 85 ns
	10	= 100 ns
	12	= 120 ns
Temperature Range	Blank	= Commercial Temperature
	I	= Industrial Temperature
Power Consumption	Blank	= Standard Part
	L	= Low Power Part
Package	FKX	= Plastic 32 pin DIL
Organization	8512	= 512K x 8
Memory Type	SYS	= Static RAM