



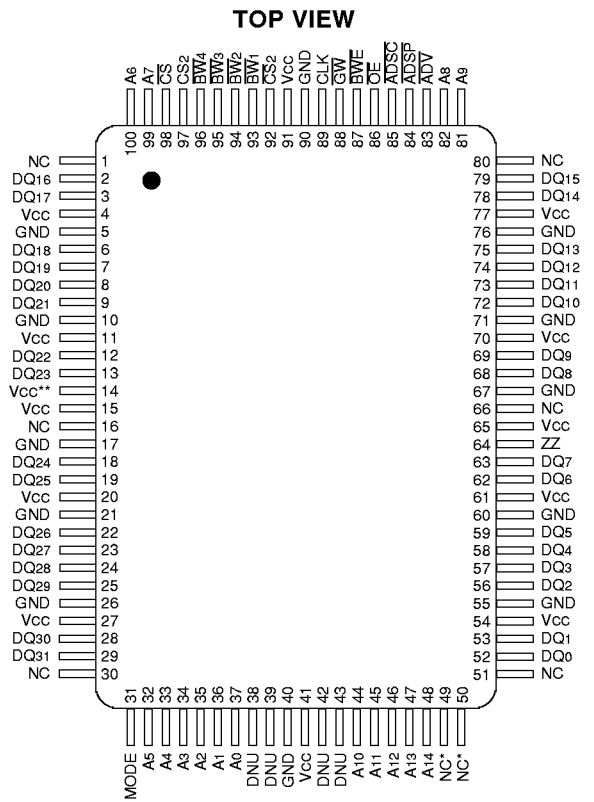
32Kx32 Monolithic Pipelined Synchronous SRAM *ADVANCED**

FEATURES

- Fast Access Times of 8 and 10ns
- Fast \overline{OE} Access Time of 7ns
- Packaging:
 - 100-pin Ceramic Quad Flatpack, CQFP. Footprint compatible with standard 100 lead TQFP package.
- Single +3.3V $\pm 5\%$ Power Supply
- 5V-Tolerant Common Data I/O
- Individual Byte Write Control and Global Write
- Single-Cycle Disable
- Industrial and Military Temperature Ranges
- Write Pass-through Capability
- Clock Controlled, Registered, Address, Data and Control for Fully Pipelined Applications
- Internally Self-timed Write Cycle
- Burst Control Pin (Interleaved or Linear Burst)
- Snooze Mode for Reduced Power Standby
- High 30pF Output Drive Capability at Rated Access Time

* This data sheet describes a product that may or may not be under development and is subject to change or cancellation without notice.

FIG. 1 PIN CONFIGURATION FOR WMYP32K32V-XTQX



PIN DESCRIPTION

DQ0-31	Data Inputs/Outputs
A0-14	Address Inputs
$\overline{BW}1-4$	Byte Writes
CLK, $\overline{CS}1$, $\overline{CS}2$	Synchronous Chip Selects
\overline{OE}	Output Enable
\overline{ADV}	Synchronous Address Advance
\overline{ADSP}	Synchronous Address Status Processor
\overline{ADSC}	Synchronous Address Status Controller
ZZ	Snooze Enable
\overline{BWE}	Byte Write Enable
\overline{GW}	Global Write
MODE	Burst Sequence Mode
Vcc	+3.3V Power Supply
GND	Ground
NC	Not Connected
DNU	Do Not Use

* Pin 49 is reserved for A15, pin 50 for A16.
 ** Pin 14 does not have to be directly connected to Vcc as long as the input voltage is $\geq V_{IH}$.



GENERAL DESCRIPTION

The device integrates a 32Kx32 SRAM Core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous input passes through registers controlled by a positive-edge-triggered Signal Clock Input (CLK). The synchronous inputs include all Addresses, all Data Inputs, active low Chip Select (\overline{CS}), two additional chip selects for easy depth expansion (\overline{CS}_2 , \overline{CS}_2), Burst Control Inputs (\overline{ADSC} , \overline{ADSP} , \overline{ADV}), Byte Write Enables (\overline{BW}_{1-4}), and Global Write (\overline{GW}).

Asynchronous inputs include the Output Enable (\overline{OE}), Clock (CLK) and Snooze Enable (ZZ). There is a Burst Mode pin (MODE) that selects between interleaved and linear burst modes. The Data Out (Q), enabled by \overline{OE} is also asynchronous. WRITE cycles can be from 1 to 4 bytes wide as controlled by the write control inputs.

Burst operation can be initiated with either \overline{ADSP} or \overline{ADSC} input pins. Subsequent burst addresses can be internally generated as controlled by the Burst Advance pin (\overline{ADV}).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written.

\overline{GW} Low causes all Bytes to be written. WRITE pass-through makes written data immediately available at the output register during the READ cycle following a WRITE, as controlled solely by \overline{OE} , to improve cache system response.

This device incorporates a single-cycle deselect feature during READ cycles. If the device is immediately deselected after a READ cycle, the output bus goes to a High-Z state after the rising edge of the clock. This feature can be useful in eliminating bus contention when depth expansion is used in cache applications

The device operates from a 3.3V power supply and all inputs and outputs are TTL-compatible.

TRUTH TABLE

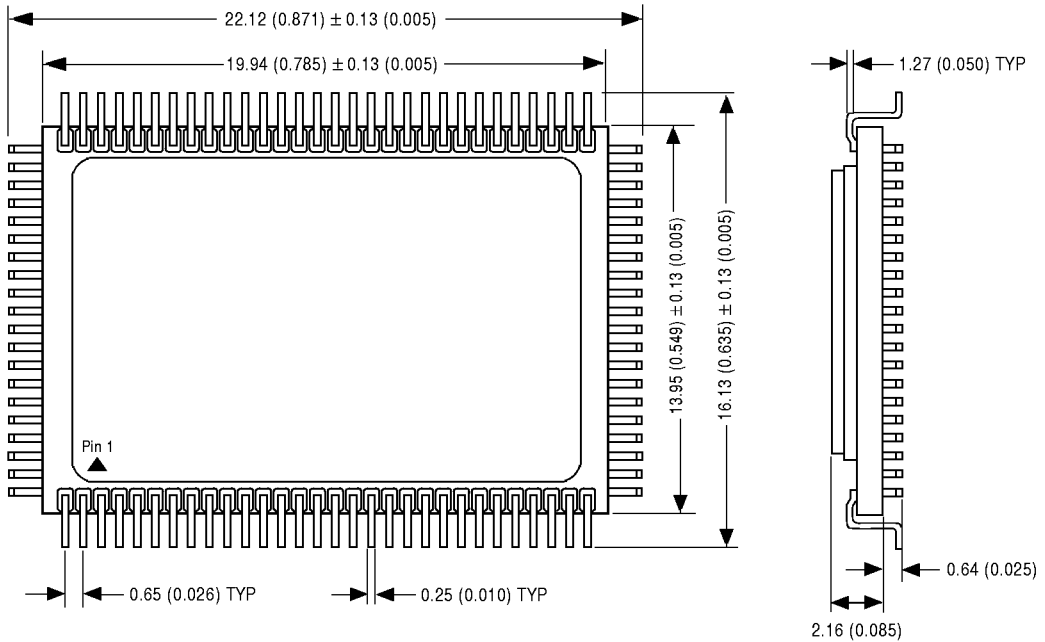
\overline{CS}	\overline{CS}_2	CS_2	ZZ	\overline{ADSP}	\overline{ADSC}	\overline{ADV}	WRITE	\overline{OE}	CLK	DQ	Address Used	Operation
H	X	X	L	X	L	X	X	X	L→H	High-Z	N/A	Deselected Cycle, Power-down
L	X	L	L	L	X	X	X	X	L→H	High-Z	N/A	Deselected Cycle, Power-down
L	H	X	L	L	X	X	X	X	L→H	High-Z	N/A	Deselected Cycle, Power-down
L	X	L	L	H	L	X	X	X	L→H	High-Z	N/A	Deselected Cycle, Power-down
L	H	X	L	H	L	X	X	X	L→H	High-Z	N/A	Deselected Cycle, Power-down
X	X	X	H	X	X	X	X	X	X	High-Z	N/A	SNOOZE MODE, Power-down
L	L	H	L	L	X	X	X	L	L→H	Q	External Address	READ Cycle, Begin Burst
L	L	H	L	L	X	X	X	H	L→H	High-Z	External Address	READ Cycle, Begin Burst
L	L	H	L	H	L	X	L	X	L→H	D	External Address	WRITE Cycle, Begin Burst
L	L	H	L	H	L	X	H	L	L→H	Q	External Address	READ Cycle, Begin Burst
L	L	H	L	H	L	X	H	H	L→H	High-Z	External Address	READ Cycle, Begin Burst
X	X	X	L	H	H	L	H	L	L→H	Q	Next Address	READ Cycle, Continue Burst
X	X	X	L	H	H	L	H	H	L→H	High-Z	Next Address	READ Cycle, Continue Burst
H	X	X	L	X	H	L	H	L	L→H	Q	Next Address	READ Cycle, Continue Burst
H	X	X	L	X	H	L	H	H	L→H	High-Z	Next Address	READ Cycle, Continue Burst
X	X	X	L	H	H	L	L	X	L→H	D	Next Address	WRITE Cycle, Continue Burst
H	X	X	L	X	H	L	L	X	L→H	D	Next Address	WRITE Cycle, Continue Burst
X	X	X	L	H	H	H	H	L	L→H	Q	Current Address	READ Cycle, Suspend Burst
X	X	X	L	H	H	H	H	H	L→H	High-Z	Current Address	READ Cycle, Suspend Burst
H	X	X	L	X	H	H	H	L	L→H	Q	Current Address	READ Cycle, Suspend Burst
H	X	X	L	X	H	H	H	H	L→H	High-Z	Current Address	READ Cycle, Suspend Burst
X	X	X	L	H	H	H	L	X	L→H	D	Current Address	WRITE Cycle, Suspend Burst
H	X	X	L	X	H	H	L	X	L→H	D	Current Address	WRITE Cycle, Suspend Burst

NOTES:

- X means "don't care." H means logic HIGH. L means logic LOW. WRITE = L means any one or more byte write enable signals (\overline{BW}_1 , \overline{BW}_2 , \overline{BW}_3 or \overline{BW}_4) and \overline{BWE} are LOW or \overline{GW} is LOW. WRITE = H means all byte write enable signals and \overline{GW} are HIGH.
- \overline{BW}_1 enables WRITES to Byte 1 (DQ0-7). \overline{BW}_2 enables WRITES to Byte 2 (DQ8-15). \overline{BW}_3 enables WRITES to Byte 3 (DQ16-23). \overline{BW}_4 enables WRITES to Byte 4 (DQ24-31).
- All inputs except \overline{OE} and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
- Wait states are inserted by suspending burst.
- For a WRITE operation following a READ operation, \overline{OE} must be HIGH before the input data setup time and held HIGH throughout the input data hold time.
- This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
- \overline{ADSP} LOW always initiates an internal READ at the L→H edge CLK. A WRITE is performed by setting one or more byte write enable signals and \overline{BWE} LOW or \overline{GW} LOW for subsequent L→H edge of CLK.



PACKAGE DIMENSION: 100 PIN CERAMIC QUAD FLAT PACK



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

WM YP 32K 32 V - XX TQ X X

LEAD FINISH:

- Blank = Gold plated leads
- A = Solder dip leads

DEVICE GRADE:

- M = Military Screened -55°C to +125°C
- I = Industrial -40°C to +85°C

PACKAGE TYPE:

- TQ = 100 pin Ceramic Quad Flatpack, CQFP

ACCESS TIME (ns)

Voltage Supply 3.3V ± 5%

ORGANIZATION, 32Kx32

Synchronous Pipelined SRAM

MONOLITHIC

WHITE MICROELECTRONICS