DS3 / SONET STS-1 Integrated Line Receiver

GENERAL DESCRIPTION

The XR-T7295 DS3/SONET STS-1 Integrated Line Receiver is a fully integrated receive interface that terminates a bipolar DS3 (44.736 MBPS) or SONET (51.84 MBPS) signal transmitted over coaxial cable.

The device also provides the functions of receive equalization (optional), automatic-gain control (AGC), clock-recovery and data retiming, loss-of-signal and loss-of-frequency-lock detection. The digital system interface is dual-rail, with received positive and negative 1s appearing as unipolar digital signals on separate output leads. The on-chip equalizer is designed for cable distances of 0 to 450ft. from the cross-connect frame to the device. The receive input has a variable input sensitivity control, providing three different sensitivity settings. High input sensitivity allows for significant amounts of flat loss within the system. Figure 1 shows the block diagram of the device.

The XR-T7295 device is manufactured by using linear CMOS technology and is packaged in a 20-pin, plastic DIP or 20-pin, plastic SOJ package for surface mounting.

Two versions of the XR-T7295 are available, one for DS3 and one for STS-1 operation (see ordering informatrion section) an input reference clock at 44.736MHz or 51.84MHz provides the frequency reference for the device.

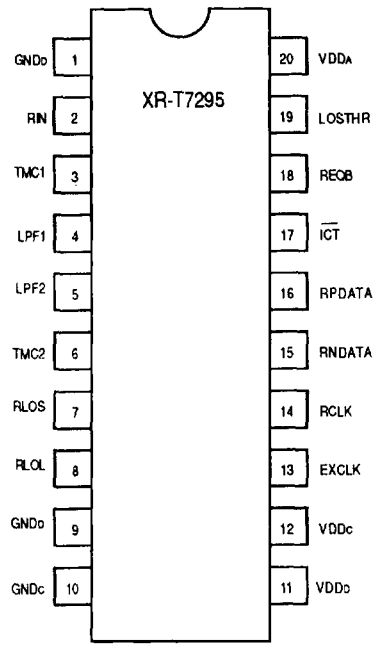
FEATURES

Fully Integrated Receive Interface for DS3 and STS-1 Rate Signals
Integrated Equalization (optional) and Timing Recovery
Loss-of-Signal and Loss-of-Lock Alarms
Variable Input Sensitivity Control
5V Power Supply

ABSOLUTE MAXIMUM RATINGS

Power Supply	-0.5V to +6.5V
Storage Temperature	-65°C to +150°

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Packages	Operating Temperature
XR-T7295TIP	Plastic DIP	-40°C to+85°C
XR-T7295TIW	SOJ	-40°C to+85°C
XR-T7295SIP	Plastic DIP	-40°C to+85°C
XR-T7295SOJ	SOJ	-40°C to+85°C

APPLICATIONS

Interface to DS-3 or E3 Networks
Digital Cross-Connect Systems
CSU/DSU Equipment
PCM Test Equipment
Fiber Optic Terminals

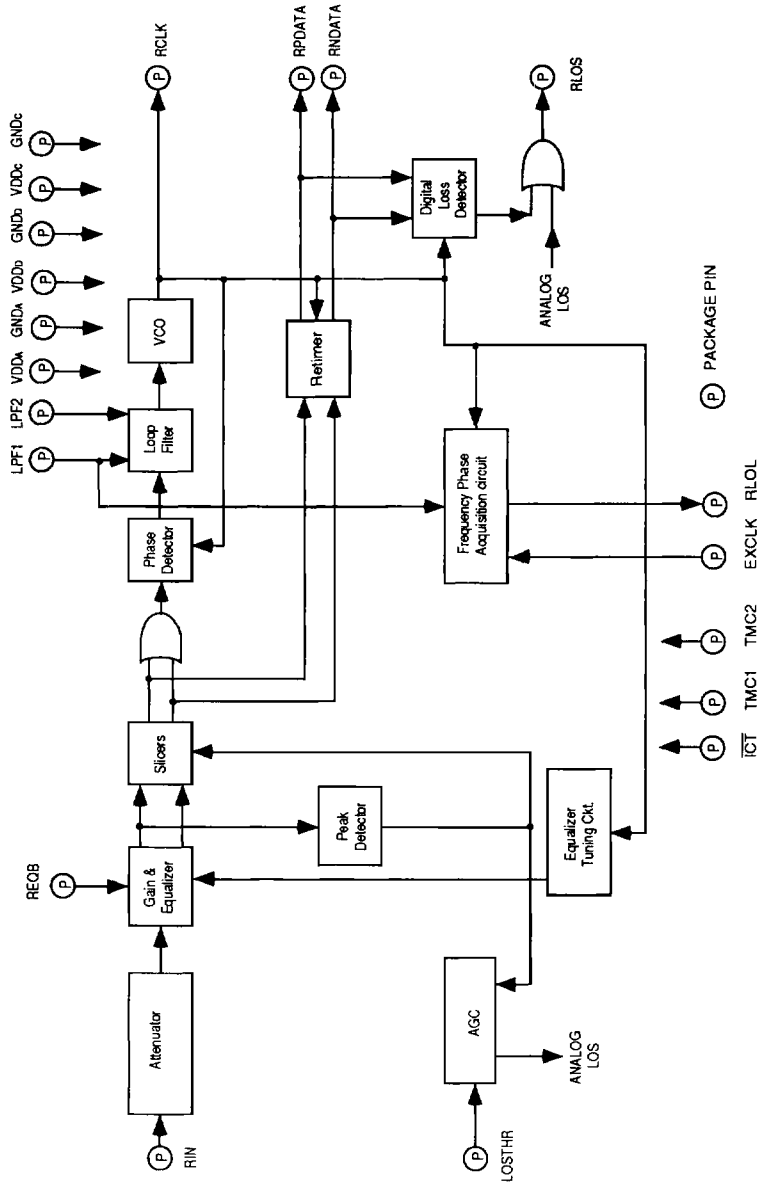


Figure 1. Block Diagram

PIN #	SYMBOL	TYPE	PIN DESCRIPTION
1	GNDA	—	**Analog Ground.**
2	RIN	I	**Receive Input.** Analog receive input. This pin is internally biased.
3,6	TMC1-TMC2	I	**Test Mode Control 1 and 2.** Internal test modes are enabled within the device by using TMC1 and TMC2. Users must tie these pins to the ground plane.
4,5	LPF1-LPF2	I	**PLL Filter 1 and 2.** An external capacitor (0.1µF ± 20%) is connected between these pins.
7	RLOS	O	**Receive Loss-of-Signal.** This pin is set high on loss of the data signal at the receive input.
8	RLOL	O	**Receive PLL Loss-of-Lock.** This pin is set high on loss of PLL frequency lock.
9	GNDD	—	**Digital Ground for PLL Clock.** Ground lead for all circuitry running synchronously with PLL clock.
10	GNDC	—	**Digital Ground for EXCLK.** Ground lead for all circuitry running synchronously with EXCLK.
11	VDDD	—	**5V Digital Supply (±10%) for PLL Clock.** Power for all circuitry running synchronously with PLL clock.
12	VDDC	—	**5V Digital Supply (±10%) for EXCLK.** Power for all circuitry running synchronously with EXCLK.
13	EXCLK	I	**External Reference Clock.** A valid DS3 (44.736MHz±100ppm) or STS-1 (51.84MHz ± 100ppm) clock must be provided at this input. The duty cycle of EXCLK, referenced to VDD /2 levels, must be 40%-60%. The EXCLK frequency determines the operation frequency of the device.
14	RCLK	O	**Receive Clock.** Recovered clock signal to the terminal equipment.
15	RNDATA	O	**Receive Negative Data.** Negative pulse data output to the terminal equipment.
16	RPDATA	O	**Receive Positive Data.** Positive pulse data output to the terminal equipment.
17	$\overline{\text{ICT}}$	I	**Output In-Circuit Test Control** (Active-Low). If $\overline{\text{ICT}}$ is forced low, all digital output pins (RCLK, RPDATA, RNDATA, RLOS, RLOL) are placed in a high-Impedance state to allow for in-circuit testing. There is an internal pull-up on this pin.
18	REQB	I	**Receive Equalization Bypass.** A high on this pin bypasses the internal equalizer. A low places the equalizer in the data path.
19	LOSTHR	I	**Loss-of-Signal Threshold Control.** The voltage forced on this pin controls the input loss-of-signal threshold. Three settings are provided by forcing GND, VDD/2, or VDD at LOSTHR.
20	VDDA	—	**5 V Analog Supply (±10%).**

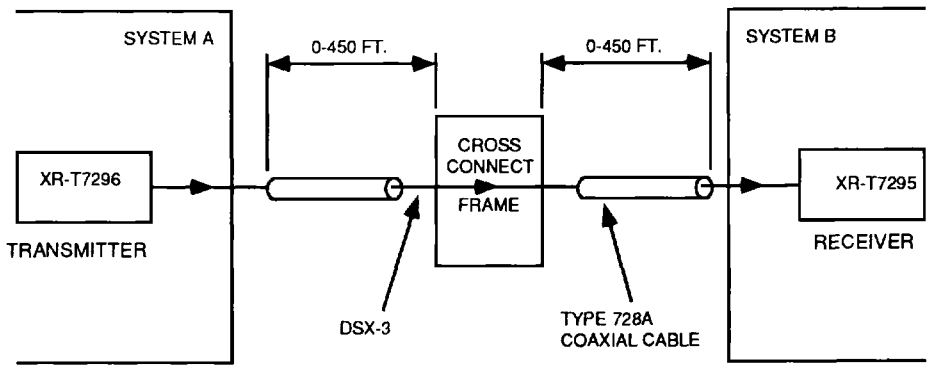


Figure 2. Application Diagram

SYSTEM DESCRIPTION

Receive Path Configurations

In the receive signal path (see Figure 1), the internal equalizer can be included by setting REQB = 0 or bypassed by setting REQB = 1. The equalizer bypass option allows easy interfacing of the XR-T7295 device into systems already containing external equalizers. Figure 3 illustrates the receive path options.

In Case 1, the signal from the DSX-3 cross-connect feeds directly into RIN. In this mode, the user should set REQB = 0, engaging the equalizer in the data path. Table 2 and the following sections describe the receive signal requirements.

In Case 2, external line build-out (LBO) and equalizer networks precede the XR-T7295 device. In this mode, the signal at RIN is already equalized, and the on-chip filters should be bypassed by setting REQB=1. The signal at RIN must meet the amplitude limits described in Table 2.

In applications where the XR-T7295 device is used to monitor DS3 transmitter outputs directly, the receive equalizer should be bypassed. Again, the signal at RIN must meet the amplitude limits described in Table 2.

Minimum signals are for SOJ devices. Due to increased package parasitics, add 5 dB to all table values for DIP devices.

Maximum input amplitude under all conditions is 850 mV pk.

Although system designers typically use power in dBm to describe input levels, the XR-T7295 responds to peak input signal amplitude, Therefore, the XR-T7295 input signal limits are given in mV pk. Conversion factors are as follows:

At DSX3: 390mV pk $\simeq$ 0dBm
At DSX3 + 450 ft. of cable 310 mV pk $\simeq$ 0 dBm.

DATA RATE	REQB	LOSTHR	MINIMUM SIGNAL	UNIT
DS3	0	0	80	mV pk
		$V_{DD}/2$	60	mV pk
		V_{DD}	40	mV pk
	1	0	80	mV pk
		$V_{DD}/2$	80	mV pk
		V_{DD}	80	mV pk
STS-1	0	0	110	mV pk
		$V_{DD}/2$	80	mV pk
		V_{DD}	60	mV pk
	1	0	110	mV pk
		$V_{DD}/2$	110	mV pK
		V_{DD}	110	mV pk

Table 2. Receive Input Signal Amplitude Requirements

DS3 SIGNAL REQUIREMENTS AT THE DSX

Pulse characteristics are specified at the DSX-3, which is an interconnection and test point referred to as the cross-connect (see Figure 2). The cross-connect exists at the point where the transmitted signal reaches the distribution frame jack. Table 3 lists the signal requirements. Currently, two isolated pulse template requirements exist: the ACCUNET T45 pulse template (see Table 4 and Figure 4) and the G.703 pulse template (see Table 5 and Figure 5) Tables 4 and 5 give the associated boundary equations for the templates. The XR-T7295 correctly transmitted signal that meets one of these templates at the cross-connect.

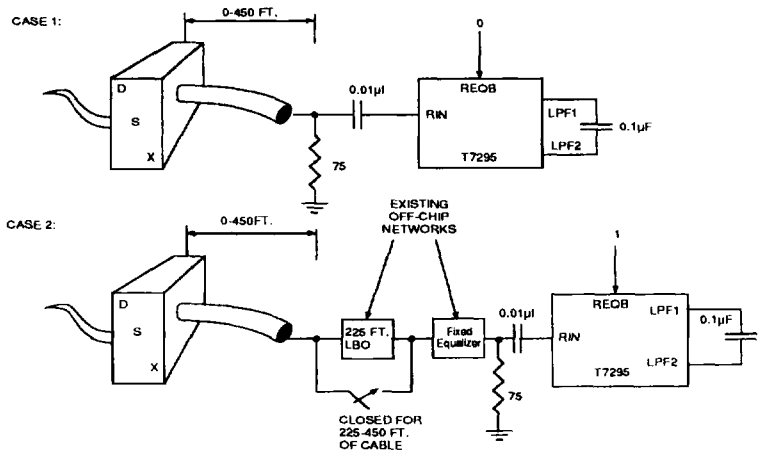


Figure 3. Receiver Configurations

PARAMETER	SPECIFICATION
Line Rate	44.736 MBPS ± 20 ppm
Line Code	Bipolar with three-0 substitution (B3ZS)
Test Load	75 Ω ± 5%
Pulse Shape	An isolated pulse must fit the template in Figure 4 or 5.* The pulse amplitude may be scaled by a constant factor to fit the template. The pulse amplitude must be between 0.36 Vpk and 0.85 Vpk , measured at the center of the pulse.
Power Levels	For and all 1s transmitted pattern, the power at 22.368 ± 0.002 MHz must be -1.8 to +5.7 dBm, and the power at 44.736 ± .002 MHz must be -21.8 dBm to -14.3 dBm.√ †

* *The pulse template proposed by G.703 standards is shown in Figure 5 and specified in Table 5. The proposed G.703 standards further state that the voltage in a time slot containing a 0 must not exceed ± 5% of the peak pulse amplitude, except for the residue of preceding pulses.*

√ *The power levels specified by the proposed G.703 standards are identical except that the power is to be measured in 3 kHz bands.*

† *The all-1s pattern must be a pure all-1s signal, without framing or other control bits.*

Table 3. DSX-3 Interconnection Specification

LOWER CURVE		UPPER CURVE	
Time	Equation	Time	Equation
$T \leq -0.36$	0	$T \leq -0.68$	0
$-0.36 \leq T \leq +0.28$	$0.5\left[1 + \sin\frac{\pi}{2}\left[1 + \frac{T}{0.18}\right]\right]$	$-0.68 \leq T \leq +0.36$	$0.5\left[1 + \sin\frac{\pi}{2}\left[1 + \frac{T}{0.34}\right]\right]$
$0.28 \leq T$	$0.11e^{-3.42(T-0.3)}$	$0.36 \leq T$	$0.05 + 0.407e^{-1.84(T-0.36)}$

Table 4. DSX-3 Pulse Template Boundaries for ACCUNET T45 Standards (See Figure 4.)

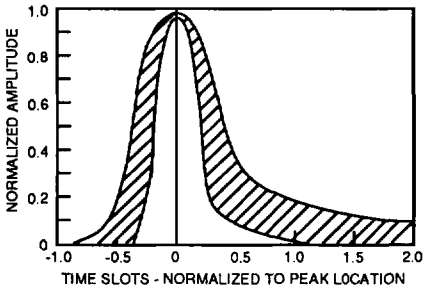


Figure 4. DSX-3 Isolated Pulse Template for ACCUNET T45 Standards

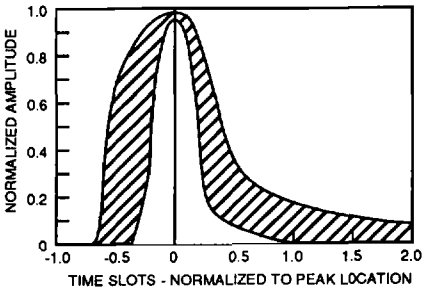


Figure 5. DSX-3 Isolated Pulse Template for G.703 Standards

LOWER CURVE		UPPER CURVE	
Time	Function	Time	Function
$T \leq -0.36$	0	$T \leq -0.65$	0
$-0.36 \leq T \leq +0.28$	$0.5\left[1 + \sin\frac{\pi}{2}\left[1 + \frac{T}{0.18}\right]\right]$	$-0.65 \leq T \leq +0$	$1.05\left[1 - e^{-4.6(T + 0.65)}\right]$
$0.28 \leq T$	$0.11e^{-3.42(T-0.3)}$	$0 \leq T \leq 0.36$	$0.5\left[1 + \sin\frac{\pi}{2}\left[1 + \frac{T}{0.34}\right]\right]$
—	—	$0.36 \leq T$	$0.05 + 0.407e^{-1.84(T-0.36)}$

Table 5. DSX-3 Pulse Template Boundaries for G.703 Standards (See Figure 5.)

STS-1 SIGNAL REQUIREMENTS AT THE STSX

For STS-1 operation, the cross-connect is referred at the STSX-1. Table 6 lists the signal requirements at the STSX-1. Instead of the DS3 isolated pulse template, an eye diagram mask is specified for STS-1 operation (TA-TSY-000253). The XR-T7295 correctly decodes any transmitted signal that meets the mask shown in Figure 6 at the STSX-1.

PARAMETER	SPECIFICATION
Line Rate	51.84 MBPS
Line Code	Bipolar with three-0 substitution (B3ZS)
Test Load	75 Ω ± 5%
Power Levels	A wide-band power level measurement at the STSX-1 interface using a low-pass filter with a 3 dB cutoff frequency of at least 200 MHz is within -2.7 dBm and 4.7 dBm.

Table 6. STSX-1 Interconnection Specification

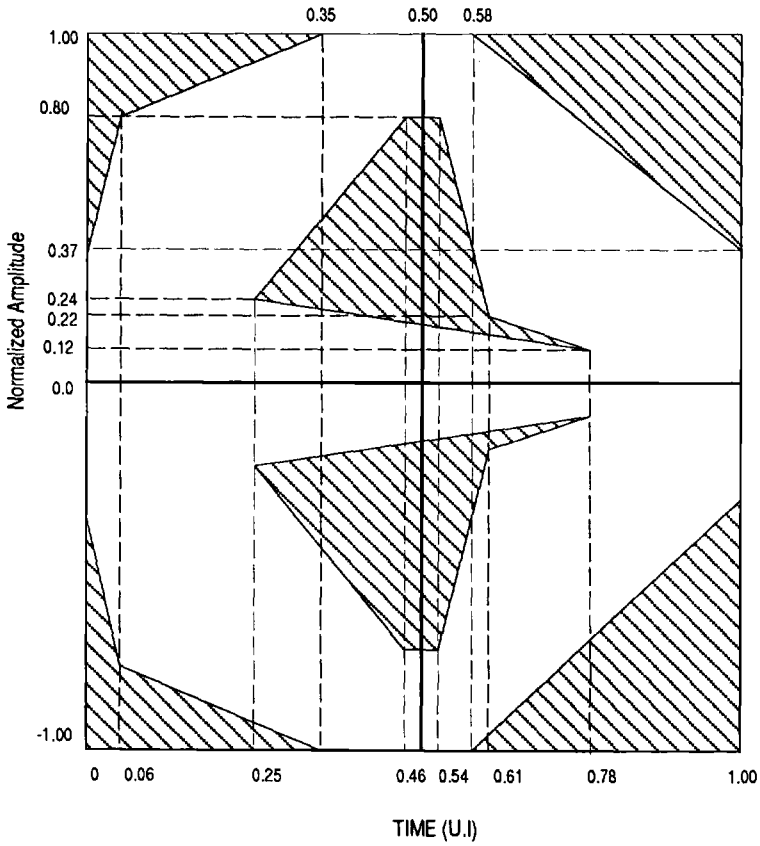


Figure 6. STSX-1 Eye Diagram Mask

LINE TERMINATION AND INPUT CAPACITANCE

The recommended receive termination is shown in Figure 3. The 75 Ω resistor terminates the coaxial cable with its characteristic Impedance. The 0.01 µF capacitor to RIN couples the signal into the receive input without disturbing the internally generated dc bias level present on RIN. The input capacitance at the RIN pin is 2.8 pF (SOJ package) and 3.6 pF (DIP package).

LOSS LIMITS FROM THE DSX-3 TO THE RECEIVE INPUT.

The signal at the cross-connect may travel through a distribution frame, coaxial cable, connectors, splitters, and backplanes before reaching the XR-T7295 device. This section defines the maximum distribution frame and cable loss from the cross-connect to the XR-T7295 input.

The distribution frame jack may introduce 0.6 ± 0.55 dB of loss. This loss may be any combination of flat or shaped (cable) loss.

The maximum cable distance between the point where the transmitted signal exits the distribution frame jack and the XR-T7295 device is 450 ft. (see Figure 2). The coaxial cable (Type 728A) used for specifying its distance limitation has the loss and phase characteristics shown in Figures 7 and 8. Other cable types also may be acceptable if distances are scaled to maintain cable loss equivalent to Type 728A cable loss.

TIMING RECOVERY

Figure 3 shows the connection to an external 0.1 µF capacitor at the LPF1/LPF2 pins. This capacitor is part of the PLL filter. A non-polarized, low-leakage capacitor should be used. A ceramic capacitor with the value 0.1 µF ± 20% is acceptable.

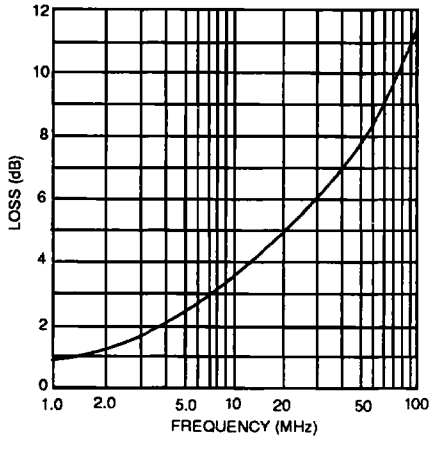


Figure 7. Loss Characteristic of 728A Coaxial Cable (450 ft.)

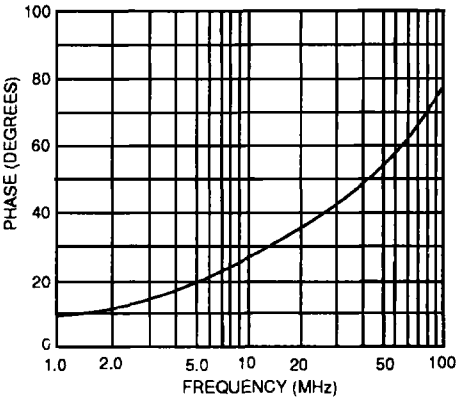


Figure 8. Phase Characteristic of 728A Coaxial Cable (450 ft.)

OUTPUT JITTER

The total jitter appearing on the RCLK output during normal operation consists of two components. First, some jitter appears on RCLK because of jitter on the incoming signal. (The next section discusses the jitter transfer characteristic, which describes the relationship between input and output jitter.) Second, noise sources within the XR-T7295 device or noise sources that are coupled into the device through the power supplies and data pattern dependent jitter due to misequalization of the input signal, all create jitter on RCLK. The magnitude of this internally generated jitter is a function of the PLL bandwidth, which in turn is a function of the input 1s density. For higher 1s densities, the amount of generated jitter decreases. Generated jitter also depends on the quality of the power supply bypassing networks used. Figure 9 shows the suggested bypassing network, and Table 7 lists the typical generated jitter performance achievable with this network.

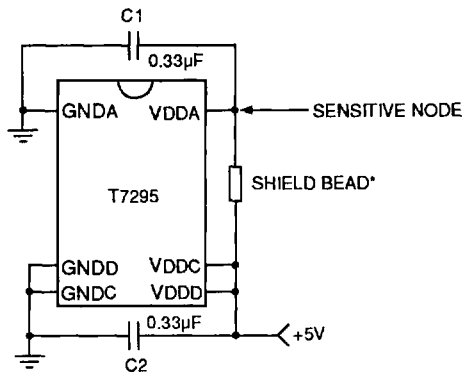
PARAMETER	TYP	MAX	UNIT
Generated Jitter*			
All-1s pattern	1.0	-	ns peak-to-peak
Repetitive 100 pattern	1.5	-	ns peak-to-peak
Jitter Transfer Characteristic**			
Peaking	0.05	0.1	dB
f 3dB	205	-	kHz

** Repetitive input data pattern at nominal DSX-3 level with VDD = 5V TA = 25°C.*
*** Repetitive 100 input at nominal DSX-3 level with VDD = 5V, TA = 25°C.*

Table 7. Generated Jitter and Jitter Transfer Characteristics

JITTER TRANSFER CHARACTERISTIC

The jitter transfer characteristic indicates the fraction of input jitter that reaches the RCLK output as a function of input jitter frequency. Table 7 shows Important jitter transfer characteristic parameters. Figure 10 also shows a typical characteristic, with the operating conditions as described in Table 7. Although standard documents do not specify jitter transfer characteristic requirements, the XR-T7295 information is provided here to assist in evaluation of the device.



**Recommended shield beads are the Fair-Rite 2643000101 or the Fair-Rite 2743019446 (surface mount).*

Figure 9. Recommended Power Supply Bypassing Network

JITTER ACCOMMODATION

Under all allowable operating conditions, the jitter accommodation of the XR-T7295 device exceeds all system requirements for error-free operation (BER<1e^{-9}). The typical (VDD = 5V, T = 25°C, DSX-3 nominal signal level) jitter accommodation for the XR-T7295 is shown in Figure 11.

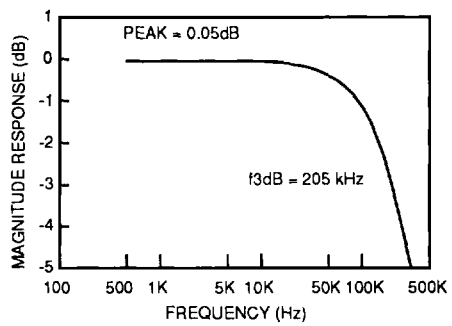
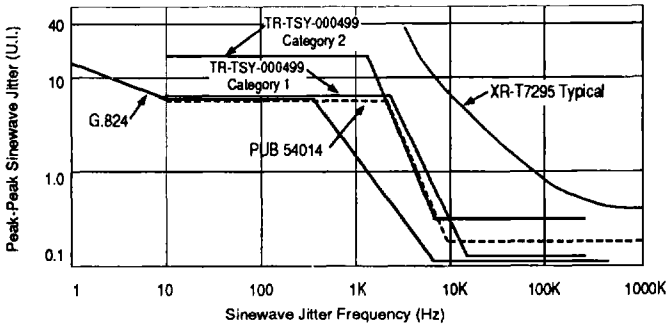


Figure 10. Typical PLL Jitter Transfer Characteristic



XR-T7295 Typical	
Jitter Frequency (Hz)	Jitter Amplitude (U.I.)
5k	10
10k	5
60k	1
300k	0.5
1M	0.4

Figure 11. Input Jitter Tolerance at DSX-3 Level

FALSE-LOCK IMMUNITY

False-lock is defined as the condition where a PLL recovered clock obtains stable phase-lock at a frequency not equal to the incoming data rate. The XR-T7295 device uses a combination frequency/phase-lock architecture to prevent false-lock. An on-chip frequency comparator continuously compares the EXCLK reference to the PLL clock. If the frequency difference between the EXCLK and PLL clock exceeds approximately ± 0.5%, correction circuitry forces re-acquisition of the proper frequency and phase.

ACQUISITION TIME

If a valid input signals is assumed to be already present at RIN, the maximum time between the application of device power and error-free operation is 20 ms. If power has already been applied, the interval between the application of valid data and error-free operation is 4 ms.

LOSS-OF-LOCK DETECTION

As stated above, the PLL acquisition aid circuitry monitors the PLL clock frequency relative to the EXCLK frequency. The acquisition circuit also monitors the retimed data to detect possible phase-lock which is 180° out of a normal phase alignment. The RLOL alarm is activated if either or both of the following conditions exist:

- The difference between the PLL clock and the EXCLK frequency exceeds approximately ± 0.5%.
- Seven consecutive 0s are detected in the retimed data (indicates possible lock which is 180° out of normal alignment).

A high RLOL output indicates that the acquisition circuit is working to bring the PLL into proper frequency lock. RLOL remains high until frequency lock has occurred; however, the minimum RLOL pulse width is 32 clock cycles.

LOSS-OF-SIGNAL DETECTION

Figure 1 shows that analog and digital methods of loss-of-signal (LOS) detection are combined to create the RLOS alarm output. RLOS is set if either the analog or digital detection circuitry indicates LOS has occurred.

ANALOG DETECTION

The analog LOS detector monitors the peak input signal amplitude.RLOS makes a high-to-low transition (input signal regained) when the input signal amplitude exceeds the loss-of signal threshold defined in Table 8. The RLOS low-to-high transition (input signal loss) occurs at a level typically 1.0 dB below the high-to-low transition level. The hysteresis prevents RLOS chattering. Once set, the RLOS alarm remains high for at least 32 clock cycles, allowing for system detection of a LOS condition without the use of an external alarm latch.

DATA RATE	REQB	LOSTHR	MIN. THRESHOLD	MAX. THRESHOLD	UNIT
DS3	0	0	60	220	mV pk
		$V_{DD/2}$	40	145	mV pk
		V_{DD}	25	90	mV pk
	1	0	45	175	mV pk
		$V_{DD/2}$	30	115	mV pk
		V_{DD}	20	70	mV pk
STS-1	0	0	75	275	mV pk
		$V_{DD/2}$	50	185	mV pk
		V_{DD}	30	115	mV pk
	1	0	55	220	mV pk
		$V_{DD/2}$	35	145	mV pk
		V_{DD}	25	90	mV pk

Lower threshold is 1.5 dB below upper threshold.

Table 8. Analog Loss-of-Signal Thresholds

Note: *The RLOS alarm is an indication of the presence of an input signal, not a bit error rate indication. Table 2 gives the minimum input amplitude needed for error free operation (BER < $1e^{-9}$) Independent of the RLOS state, the device will attempt to recover correct timing data. The RLOS low-to-high transition typically occurs 1dB below the high-tolow transition.*

To allow for varying levels of noise and crosstalk in different applications, three loss-of-signal threshold settings are available using the LOSTHR pin. Setting LOSTHR = VDD provides the lowest loss-of-signal threshold; LOSTHR = VDD /2 (can be produced using between VDDD and GNDD) provides an intermediate threshold; and LOSTHR = GND provides the highest threshold. The LOSTHR pin must be set to its desired value at powerup and must not be changed during operation.

DIGITAL DETECTION

In addition to the signal amplitude monitoring of the analog LOS detector, the digital LOS detector monitors the recovered data 1s density. The RLOS alarm goes high if 160 $\pm$ 32 or more consecutive 0s occur in the receive data stream. The alarm goes low when at least ten 1s occur in a string of 32 consecutive bits. This hysteresis prevents RLOS chattering and guarantees a minimum RLOS pulse width of 32 clock cycles.

RECOVERED CLOCK AND DATA TIMING

Table 10 and Figure 12 summarize the timing relationships between the high-speed logic signals RCLK, RPDATA, and RNDATA. All duty cycle and timing relationships are referenced to VDD/2 threshold level. RPDATA and RNDATA change on the rising edge of RCLK and are valid during the falling edge of RCLK. A positive pulse at RIN creates a high level on RPDATA and a low level on RNDATA. A negative pulse at the input creates a high level on RNDATA and a low level on RPDATA, and a received zero produces low levels on both RPDATA and RNDATA.

IN-CIRCUIT TEST CAPABILITY

When pulled low, the $\overline{ICT}$ pin forces all digital output buffers (RCLK, RPDATA, RNDATA, RLOS, RLOL pins) to be placed in a high output impedance state. This feature allows in-circuit testing to be done on neighboring devices without concern for XR-T7295 device buffer damage. When forced high, the $\overline{ICT}$ pin does not affect device operation. An internal pull-up device (nominally 50 kΩ) is provided on this pin; therefore, users can leave this pin floating for normal operation. In-circuit test equipment can pull ICT low during in-circuit testing without damaging the device. This is the only pin for which Internal pull-up/pull-down is provided.

LOGIC INTERFACE CHARACTERISTICS $-40°C \leq T_A \leq +85°C$, $V_{DD} = 5V \pm 10\%$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
Input Voltage					
Low	VIL	—	GNDD	0.5	V
High	VIH	—	VDDD-0.5	VDDD	V
Output Voltage					
Low	VOL	-5.0mA	GNDD	0.4	V
High	VOH	5.0mA	VDDD- 0.5	VDDD	V
Input Capacitance	CI	—	10	pF	
Load Capacitance	CL	—	10	pF	
Input Leakage	IL	-0.5 to VDD + 0.5V (all input pins except 2 and 17)	-10	+10	µA
		0 V (pin 17)	0.02	0.5	mA
		VDD (pin 2)	5	8	mA

Table 9. Logic Interface Characteristic

TIMING CHARACTERISTICS All timing characteristics are measured with 10pF loading

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
tRCH1RCH2	Clock Rise Time (10% - 90%)	-	-	3.5	ns
tRCL2RCL1	Clock Fall Time (10% - 90%)	-	-	2.5	ns
tRDVRCL	Receive Data Set-up Time	5.5	-	-	ns
tRCLRDX	Receive Data Hold Time	8.5	-	-	ns
tRCHRDV	Receive Propagation Delay	0.6	-	3.0	ns
-	Clock Duty Cycle	45	50	55	%

Table 10. System Interface Timing Characteristics (See Figure 14.)

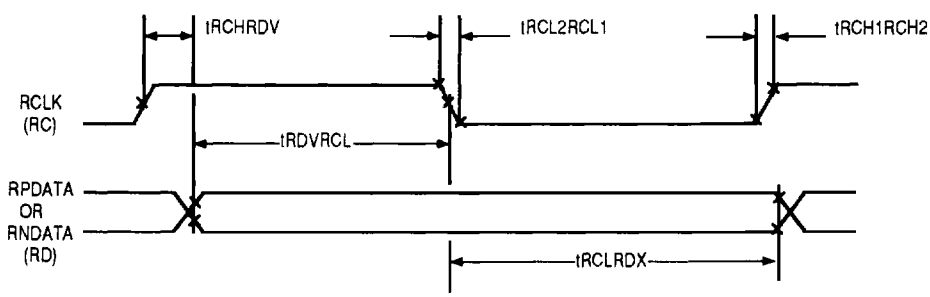


Figure 12. Timing Diagram for System Interface

ELECTRICAL CHARACTERISTICS

T_A = -40°C to +85°C, V_{DD} = 5V ± 10%
Typical values are for V_{DD} = 5.0 V, 25°C, and random data. Maximum values are for V_{DD} = 5.5V all 1s data.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Power Supply Current DS3	IDD				
REQB = 0		-	82	106	mA
REQB = 1		-	79	103	mA
STS-1					
REQB = 0		-	87	111	mA
REQB = 1		-	83	108	mA

BOARD LAYOUT CONSIDERATIONS

Power Supply Bypassing

Figure 9 Illustrates the recommended power supply bypassing network. A 0.1 µF capacitor bypasses the digital supplies. The analog supply V_{DDA} is bypassed by using a 0.1 µF capacitor and a shield bead that removes significant amounts of that removes significant amounts of high-frequency noise generated by the system and by the device logic. Good quality, high-frequency (low lead Inductance) capacitors should be used. Finally, it is most important that all ground connections be made to a low-impedance ground plane.

Receive Input

The connections to the receive Input pin, RIN, must be carefully considered. Noise-coupling must be minimized along the path from the signal entering the board to the input pin. Any noise coupled into the XR-T7295 input directly degrades the signal-to-noise ratio of the Input signal.

PLL Filter Capacitor

The PLL filter capacitor between pins LPF1 and LPF2 must be placed as close to the chip as possible. The LPF1 and LPF2 pins are adjacent, allowing for short lead lengths with no crossover's to the external capacitor. Noise-coupling into the LPF1 and LPF2 pins may degrade PLL performance.

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting.

COMPLIANCE SPECIFICATIONS

• Compliance with *AT&T Publication54014, "ACCUNET* ® T45 Service Description and Interface Specifications," June 1987.

• Compliance with *ANSI Standard T1.102*-1989, " Digital Hierarchy - Electrical Interfaces, " 1989.

• Compliance with *Compatibility Bulletin 119,* "Interconnection Specification for Digital Cross-Connects," October 1979.

• Compliance with *CCITT Recommendations G.703 and G.824,* 1988.

• Compliance with *TR-TSY-000499,* "Transport Systems Generic Requirements (TSGR): Common Requirements, " December 1988.