

### FEATURES

- Monolithic Complete 10-Bit ADC
- 40 MSPS Conversion Rate
- On-Chip Track-and-Hold
- On-Chip Voltage Reference
- Low 5 pF Input Capacitance
- TTL/CMOS Outputs
- Tri-State Output Buffers
- Single +5V Power Supply Operation
- +5 or +3V Output Logic Compatibility
- Low Power Dissipation: 215 mW-typ
- -25°C to +85°C Operation Temperature Range

### APPLICATIONS

- Video Imaging
- Digital Cameras and Camcorders
- Medical Ultrasound Imaging
- IR Imaging
- Radar Receivers
- Digital Communications

### BENEFITS

- Reduction of Components
- Reduction of System Cost
- High Performance @ Low Power Dissipation
- Long Term Time and Temperature Stability

### GENERAL DESCRIPTION

The XRD6440 is a 10-bit, monolithic, complete 40 MSPS ADC. Manufactured using a standard CMOS process, XRD6440 offers low power, low cost and excellent performance. The on-chip track-and-hold amplifier(T/H) and voltage reference (VREF) eliminate the need for external active components, requiring only an external ADC conversion clock for the application. The XRD6440 analog input can be driven with ease due to the high input impedance of  $R_{in} = 34K\Omega$  and  $C_{in} = 5pF$ .

The patented design architecture uses 16 time-interleaved 10-bit SAR ADCs to achieve high conversion rate of 40 MSPS minimum. In order to insure and maintain accurate 10-bit operation with respect to time and temperature, XRD6440 incorporates an auto-calibration circuit which continuously adjusts and matches the offset and linearity of each ADC. This

auto-calibration circuit is transparent to the user after the initial 4ms calibration (168,000 initial clock cycles).

The power dissipation at 40 MSPS is only 215 mW with +5V power supply, decreasing to 170mW at 20 MSPS.

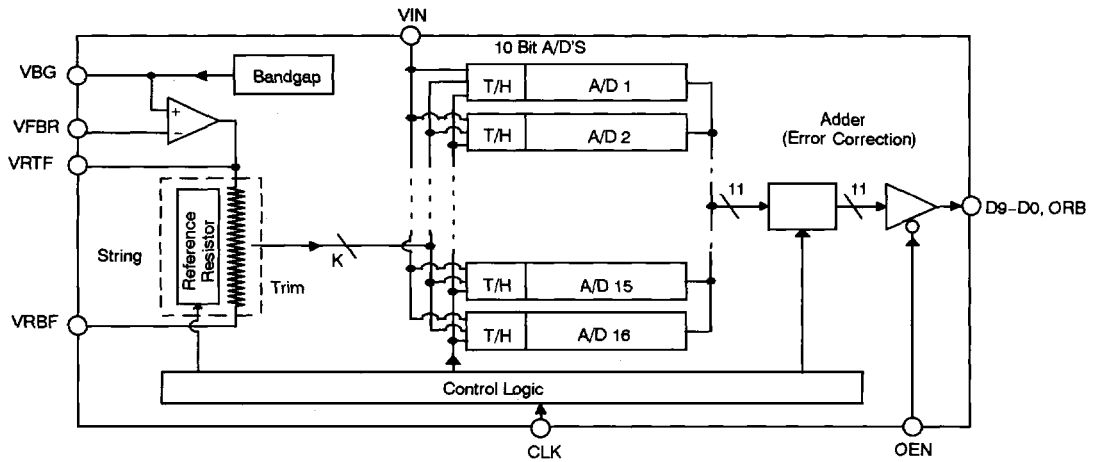
The outputs are compatible with +5 and +3V TTL/CMOS logic levels. The digital output data is straight binary format, and the tri-state disable function is provided for common bus interface.

The XRD6440 internal reference provides cost savings and simplifies the design/development. The output voltage of the internal reference is set by two external resistors. The internal reference can be disabled if an external reference is used.

The XRD6440 is available in 28-Lead plastic SSOP and 32-Lead plastic TQFP packages over the temperature range of -25°C to +85°C.

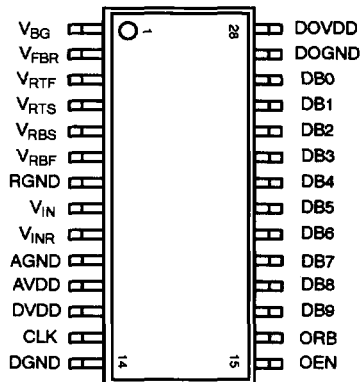
### ORDERING INFORMATION

| Part No.   | Package                    | Operating Temperature Range |
|------------|----------------------------|-----------------------------|
| XRD6440AIU | 28 -Lead SSOP(10x5x1.7 mm) | -25°C to +85°C              |
| XRD6440AIV | 32- Lead TQFP (7x7x1.0 mm) | -25°C to +85°C              |



**Figure 1. XRD6440 Simplified Block Diagram**

## PIN CONFIGURATION



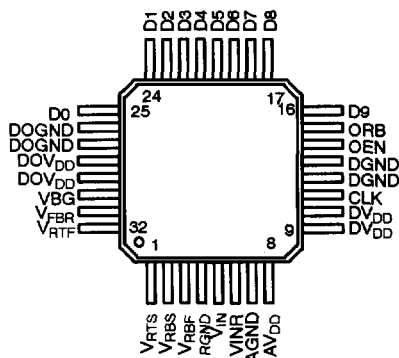
**28 Lead SSOP Package**

## PIN DESCRIPTION (28-Lead SSOP Package)

| Pin # | Symbol | Description   |
|-------|--------|---|
| 1     | VBG    | Bandgap Voltage Output  |
| 2     | VFBR   | Feedback for Internal Voltage Regulator   |
| 3     | VRTF   | Top(+) Reference Voltage Force  |
| 4     | VRTS   | Top(+) Reference Voltage Sense  |
| 5     | VRBS   | Bottom(-) Reference Voltage Sense   |
| 6     | VRBF   | Bottom(-) Reference Voltage Force   |
| 7     | RGND   | Analog Reference Ground   |
| 8     | VIN    | Analog Voltage Input  |
| 9     | VINR   | Analog Input Reference  |
| 10    | AGND   | Analog Ground   |
| 11    | AVDD   | Analog Power Supply   |
| 12    | DVDD   | Digital Power Supply  |
| 13    | CLK    | Clock Input   |
| 14    | DGND   | Digital Ground  |
| 15    | OEN    | Digital Output Enable (Tri-State Control), Low=Enable, High=Disable (Tri-State) |
| 16    | ORB    | Over Range Digital Output Bit   |

## PIN DESCRIPTION (CONT'D)

| Pin # | Symbol | Description                      |
|-------|--------|----------------------------------|
| 17    | DB9    | MSB-Digital Output Data Bit 9    |
| 18    | DB8    | Digital Output Data Bit 8        |
| 19    | DB7    | Digital Output Data Bit 7        |
| 20    | DB6    | Digital Output Data Bit 6        |
| 21    | DB5    | Digital Output Data Bit 5        |
| 22    | DB4    | Digital Output Data Bit 4        |
| 23    | DB3    | Digital Output Data Bit 3        |
| 24    | DB2    | Digital Output Data Bit 2        |
| 25    | DB1    | Digital Output Data Bit 1        |
| 26    | DB0    | LSB- Digital Output Data Bit 0   |
| 27    | DOGND  | Digital Data Output Ground       |
| 28    | DOVDD  | Digital Data Output Power Supply |



**32 Lead TQFP Package**

**PIN DESCRIPTION (32-Lead TQFP Package)**

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| Pin # | Symbol | Description                        |
|-------|--------|------------------------------------|
| 1     | VRTS   | Top (+) Reference Voltage Sense    |
| 2     | VRBS   | Bottom (-) Reference Voltage Sense |
| 3     | VRBF   | Bottom (-) Reference Voltage Force |
| 4     | RGND   | Analog Reference Ground            |
| 5     | VIN    | Analog Voltage Input               |
| 6     | VINR   | Analog Input Reference             |
| 7     | AGND   | Analog Ground                      |
| 8     | AVDD   | Analog Power Supply                |
| 9     | DVDD   | Digital Power Supply               |
| 10    | DVDD   | Digital Power Supply               |
| 11    | CLK    | Clock Input                        |
| 12    | DGND   | Digital Ground                     |
| 13    | DGND   | Digital Ground                     |
| 14    | OEN    | Output Enable Control              |
| 15    | ORB    | Out of Range Digital Output        |
| 16    | D9     | Data Output Bit 9 (MSB)            |
| 17    | D8     | Data Output Bit 8                  |
| 18    | D7     | Data Output Bit 7                  |
| 19    | D6     | Data Output Bit 6                  |
| 20    | D5     | Data Output Bit 5                  |
| 21    | D4     | Data Output Bit 4                  |
| 22    | D3     | Data Output Bit 3                  |
| 23    | D2     | Data Output Bit 2                  |
| 24    | D1     | Data Output Bit 1                  |
| 25    | D0     | Data Output Bit 0 (LSB)            |

## PIN DESCRIPTION(32-Lead TQFP Package)

| Pin # | Symbol            | Description                             |
|-------|-------------------|---|
| 26    | DOGND             | Digital Data Output Ground              |
| 27    | DOGND             | Digital Data Output Ground              |
| 28    | DOV <sub>DD</sub> | Digital Data Output Power Supply        |
| 29    | DOV <sub>DD</sub> | Digital Data Output Power Supply        |
| 30    | VBG               | Bandgap Voltage Output                  |
| 31    | V <sub>FBR</sub>  | Feedback for Internal Voltage Regulator |
| 32    | V <sub>RTF</sub>  | Top (+) Reference Voltage Force         |

## ELECTRICAL CHARACTERISTICS TABLE

Test Conditions (Unless Otherwise Specified):

Ta = 25°C AV<sub>DD</sub> = DV<sub>DD</sub> = +5V, V<sub>IN</sub> = GND to +4V, V<sub>RBF</sub> = GND, V<sub>RTF</sub> = +4V and Fs = 40 MSPS, 50% Duty Cycle

| Symbol  | Parameter                     | Min. | Typ.   | Max. | Unit   | Conditions/Comments                                 |
|---|-------------------------------|------|--------|------|--------|---|
| DC ACCURACY   |                               |      |        |      |        |   |
| DNL   | Differential Non-Linearity    | -1.0 | +/-0.7 | 1.0  | LSB    | Guaranteed by Test                                  |
| INL   | Integral Non-Linearity        |      | +/-1.1 |      | LSB    |   |
| MON   | Monotonicity                  |      |        |      |        |   |
| ZSE   | Zero Scale Error              |      | ±20    |      | mV     |   |
| ANALOG INPUT  |                               |      |        |      |        |   |
| INVR  | Input Voltage Range           | AGND |        | VRTR | V      | Guaranteed by Characterization<br>-1dB Small Signal |
| INRES   | Input Resistance              |      | 34     |      | KΩ     |   |
| INCAP   | Input Capacitance             |      | 5      | 8    | pF     |   |
| INBW  | Input Bandwidth               |      | 400    |      | MHz    |   |
| REFERENCE INPUT   |                               |      |        |      |        |   |
| RLAD  | Ladder Resistance             | 400  | 500    | 600  | Ω      | Guaranteed by Characterization                      |
| RLADTCO   | Ladder Resistance Tempco      |      | +0.8   |      | Ω/°C   |   |
| VRTR  | Top(+) Reference Range        | 3.0  |        | AVDD | V      |   |
| VRBR  | Bottom(-) Reference Range     | AGND |        | 2.0  | V      |   |
| ΔVRR  | (VRT-VRB) Reference Range     | 1.0  |        | AVDD | V      |   |
| INTERNAL BANDGAP REFERENCE AND REFERENCE BUFFER               |                               |      |        |      |        |   |
| VBGVR   | Bandgap Output Voltage Range  |      | 1.240  |      | V      |   |
| VBVR  | Buffer Output Voltage Range   |      |        | 4.5  | V      |   |
| VBGTC   | Bandgap Reference Tempco      | -120 | +36    | 120  | ppm/°C |   |
| BGPSRR  | Bandgap PSRR                  |      | +6     |      | mV/V   |   |
| CONVERSION and TIMING CHARACTERISTICS (C <sub>L</sub> = 15pF) |                               |      |        |      |        |   |
| MAXCON  | Maximum Conversion Rate       | 40   | 60     |      | MSPS   | Clock Cycles Digital Data Delay                     |
| MINCON  | Minimum Conversion Rate       |      | 100    |      | KSPS   |   |
| PDEL  | Pipeline Delay(Latency)       |      | 12     |      | CLK    |   |
| t <sub>ad</sub>   | Aperture Delay Time           |      | 4      |      | ns     |   |
| APJT  | Aperture Jitter Time          |      | 12     |      | ps     | Peak-to Peak  |
| t <sub>r</sub>  | Digital Output Rise Time      |      | 10     |      | ns     |   |
| t <sub>f</sub>  | Digital Output Fall Time      |      | 10     |      | ns     |   |
| t <sub>pd</sub>   | Output Data Propagation Delay |      | 10     | 14   | ns     |   |
| t <sub>den</sub>  | Output Data Enable Delay      |      | 10     | 14   | ns     | Guaranteed by Characterization                      |
| t <sub>dis</sub>  | Output Data Disable Delay     |      | 9      |      | ns     | Guaranteed by Characterization                      |
| CLKDC   | Clock Duty Cycle              | 30   | 50     | 70   | %      | Guaranteed by Characterization                      |

**ELECTRICAL CHARACTERISTICS TABLE (Continued)**

| Symbol                       | Parameter                      | Min. | Typ. | Max. | Unit | Conditions/Comments     |
|------------------------------|--------------------------------|------|------|------|------|-------------------------|
| DYNAMIC PERFORMANCE          |                                |      |      |      |      |                         |
| SNR                          | Signal-to-Noise Ratio          |      |      |      |      | Not Including Harmonics |
|                              | fin = 1.0 MHz                  | 55   | 58   |      | dB   |                         |
|                              | fin = 3.6 MHz                  | 55   | 58   |      | dB   |                         |
|                              | fin = 12.5 MHz                 |      | 57   |      | dB   |                         |
| THD                          | Harmonic Distortion            |      |      |      |      |                         |
|                              | fin = 1.0 MHz                  | -63  | -66  |      | dB   |                         |
|                              | fin = 3.6 MHz                  | -61  | -63  |      | dB   |                         |
|                              | fin = 12.5 MHz                 |      | -60  |      | dB   |                         |
| SINAD                        | Signal-to Noise and Distortion |      |      |      |      |                         |
|                              | fin = 1.0 MHz                  | 54   | 57   |      | dB   |                         |
|                              | fin = 3.6 MHz                  | 54   | 57   |      | dB   |                         |
|                              | fin = 12.5 MHz                 |      | 55   |      | dB   |                         |
| ENOB                         | Effective Number of Bits       |      |      |      |      |                         |
|                              | fin = 1.0 MHz                  |      | 9.2  |      | Bit  |                         |
|                              | fin = 3.6 MHz                  |      | 9.1  |      | Bit  |                         |
|                              | fin = 12.5 MHz                 |      | 8.9  |      | Bit  |                         |
| SFDR                         | Spurious Free Dynamic Range    |      | 73   |      | dBFS | fin=1MHz                |
| DIFFPH                       | Differential Phase             |      | 0.1  |      | °    | Degree                  |
| DIFFG                        | Differential Gain              |      | 0.5  |      | %    | Percent                 |
| DIGITAL INPUTS               |                                |      |      |      |      |                         |
| DVINH                        | Digital Input High Voltage     | 4.0  |      |      | V    |                         |
| DVINL                        | Digital Input Low Voltage      |      |      | 0.8  | V    |                         |
| DIINH                        | Digital Input High Current     | -5   | 0.05 | 5    | nA   |                         |
| DIINL                        | Digital Input Low Current      | -5   | 0.05 | 5    | nA   |                         |
| DINC                         | Digital Input Capacitance      |      | 5    | 8    | pF   |                         |
| DIGITAL OUTPUTS (CL = 15 pF) |                                |      |      |      |      |                         |
| DOHV                         | Digital Output High Voltage    | 4.5  | 4.7  |      | V    | IOH = 1.5 mA            |
| DOLV                         | Digital Output Low Voltage     |      | 0.3  | 0.5  | V    | IOL = 1.5 mA            |
| IOZ                          | High-Z Leakage                 | -10  | 0.1  | 10   | nA   |                         |



## ELECTRICAL CHARACTERISTICS TABLE (Continued)

| Symbol                | Parameter                    | Min. | Typ.             | Max. | Unit | Conditions                                    |
|-----------------------|------------------------------|------|------------------|------|------|---|
| <b>POWER SUPPLIES</b> |                              |      |                  |      |      |   |
| AV <sub>DD</sub>      | Analog Power Supply Voltage  | 4.5  | 5.0              | 5.5  | V    | DV <sub>DD</sub> = AV <sub>DD</sub>           |
| DV <sub>DD</sub>      | Digital Power Supply Range   |      | AV <sub>DD</sub> |      | V    |   |
| AI <sub>DD</sub>      | Analog Power Supply Current  |      | 27               | 35   | mA   |   |
| DI <sub>DD</sub>      | Digital Power Supply Current |      | 10               | 13   | mA   |   |
| DOI <sub>DD</sub>     | DOOUT Power Supply Current   |      | 6                | 8    | mA   |   |
| PD                    | Power Dissipation            |      | 215              | 280  | mW   | C <sub>L</sub> =10pF, AV <sub>DD</sub> = 5.0V |

Specifications are subject to change without notice

## ABSOLUTE MAXIMUM RATINGS (TA = +25°C unless otherwise noted)<sup>1, 2, 3</sup>

|                                   |                                   |  |         |
|-----------------------------------|-----------------------------------|--|---------|
| V <sub>DD</sub> to GND            | +7.0V                             | Package Power Dissipation Rating to 75°C |         |
| V <sub>RT</sub> & V <sub>RB</sub> | V <sub>DD</sub> +0.5 to GND -0.5V | TQFP                                     | 1000mW  |
| V <sub>IN</sub>                   | V <sub>DD</sub> +0.5 to GND -0.5V | Derates above 75°C                       | 18mW/°C |
| All Inputs                        | V <sub>DD</sub> +0.5 to GND -0.5V | SSOP                                     | 500mW   |
| All Outputs                       | V <sub>DD</sub> +0.5 to GND -0.5V | Derates above 75°C                       | 20mW/°C |
| Storage Temperature               | -65 to +150°C                     | Lead Temperature (Soldering 10 seconds)  | +300°C  |

### Notes:

- <sup>1</sup> Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
- <sup>2</sup> Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. All inputs have protection diodes which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
- <sup>3</sup> V<sub>DD</sub> refers to AV<sub>DD</sub> and DV<sub>DD</sub>. GND refers to AGND and DGND.

## TIMING DIAGRAMS

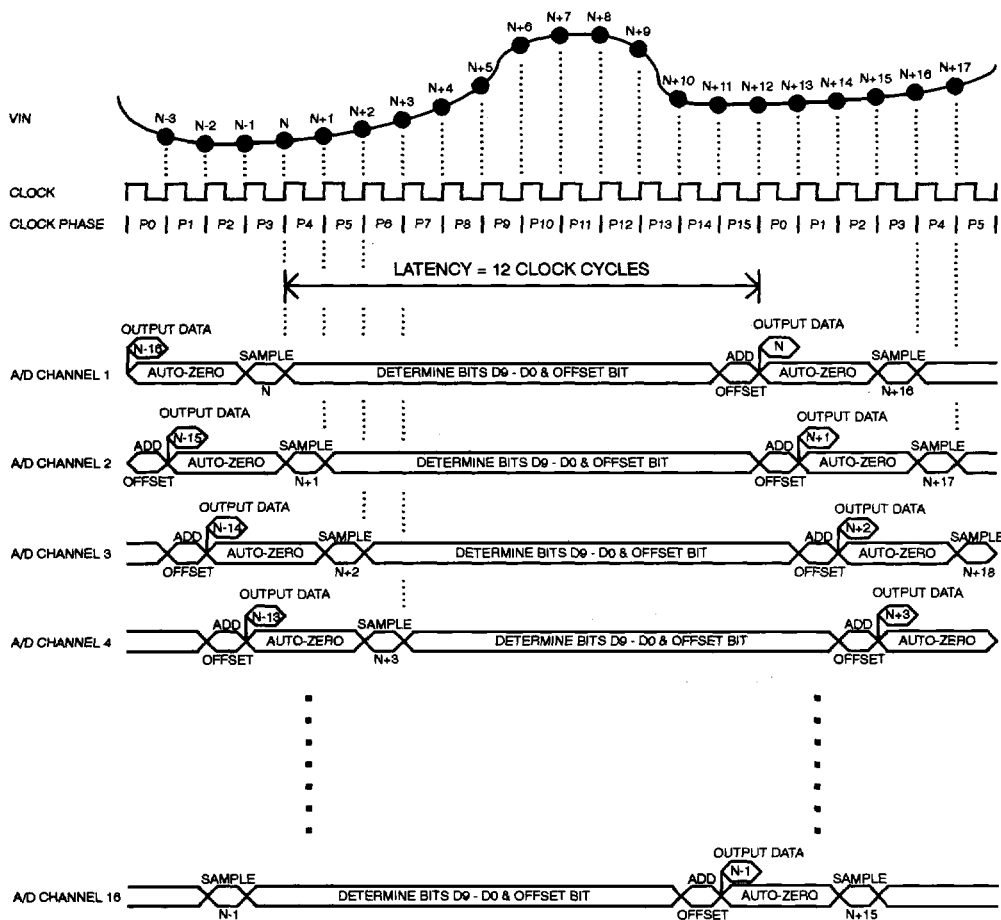


Figure 2. Timing Diagram

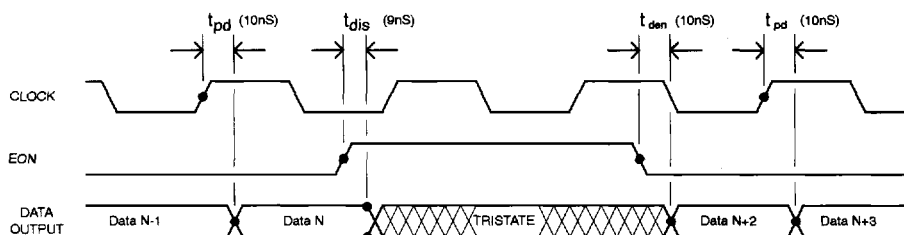


Figure 3. Clock-to-Output Data Relay

## THEORY OF OPERATION

The XRD6440 is composed of 16 individual 10 bit successive approximation A/D converters operated in a time-interleaved fashion (see Figure 1.) A single resistor string with multiple taps generates reference voltages. This string is shared by all 16 converter channels, so any non-linearity (differential and integral) is common to all 16 channels.

Multiplexing of the 16 channels gives a 10 bit output every clock cycle, while changes in the input will take 13 clock edges to appear at the output (i.e. latency), much like a pipeline converter.

Each A/D channel is calibrated for offset and linearity just before it samples the input. In addition, the reference resistor string is continuously calibrated for linearity (differential and integral).

### Successive Approximation A/D Conversion

N-bit successive approximation uses an N-bit digital-to-analog converter (DAC), a comparator, a sample-and-hold, and an N-bit successive approximation register (SAR) (see Figure 4.) After the input is sampled, the SAR sets all bits of the DAC to 0 except the MSB, which is set to 1 (output of the DAC is set to mid-scale). The comparator tells the SAR if the input is higher or lower than the DAC mid-scale. The MSB is set to 1 if the input is higher, 0 if it's lower. With the MSB set to its new value, the SAR then sets the next most significant bit to 1. The comparator again tells the SAR if the input is higher or

lower than the DAC output. The SAR sets the bit accordingly, and so on, until finally finishing with the LSB. Once the LSB has been determined, the conversion is finished and the next conversion may begin. A successive approximation converter needs one clock cycle for each bit, plus additional time to sample the input.

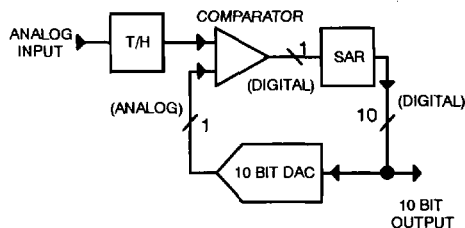
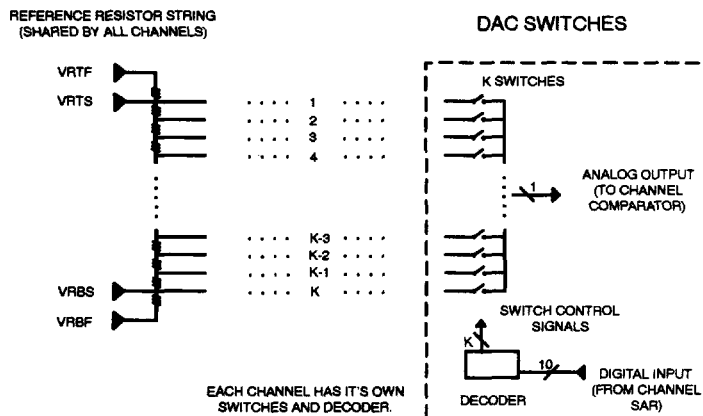


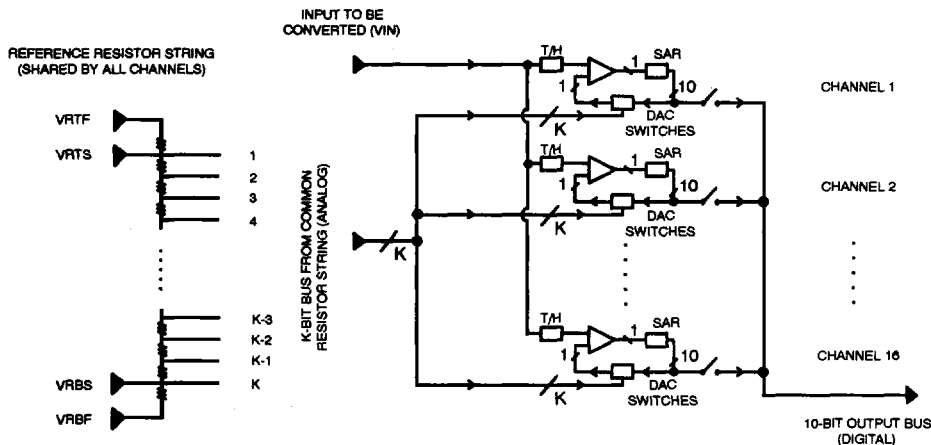
Figure 4. Successive Approximation (SAR) Architecture

### Common DAC Shared by the 16 A/D Channels

For the XRD6440, each of the 16 A/D channels has its own S/H, comparator and SAR. The resistor string portion of the DAC, however, is shared by all 16 channels. The DAC analog switches are included in each channel, with all switches from all 16 channels going to the common resistor string. This gives the ability for each channel to access a different point on the resistor string simultaneously (refer to Figure 5. and Figure 6.).



**Figure 5. Simplified DAC Architecture**



**Figure 6. ADC Channel Multiplexing**

## Time-Interleaved Multiplexing of the A/D Converters

A 16 phase clock governs the chip timing. Each A/D channel is offset one clock phase from the previous A/D channel. For any given clock phase, one of the channels is sampling, and one of the channels is producing an output (refer to Figure 2.).

## Digital Outputs

The circuits which supply the digital outputs (D0 - D9, and ORB) have their own supplies (DOVDD and DOGND). These supplies have no connection to the other supplies of the XRD6440, other than diode connections between DOGND and the other ground pins (AGND & DGND).

DOVDD can be at a lower voltage than  $AV_{DD}$  and  $DV_{DD}$ , allowing the A/D to send its data to a 3V system.

Output is normal binary. D9 is the MSB, and D0 is the LSB. Outputs change on the rising edge of the input clock (see Figure 2. and Figure 3.)

ORB is logic 1 if the input is out of range (i.e. too low or too high).

D0 - D9 and ORB outputs will become high impedance when OEN is high.

### Automatic Calibration

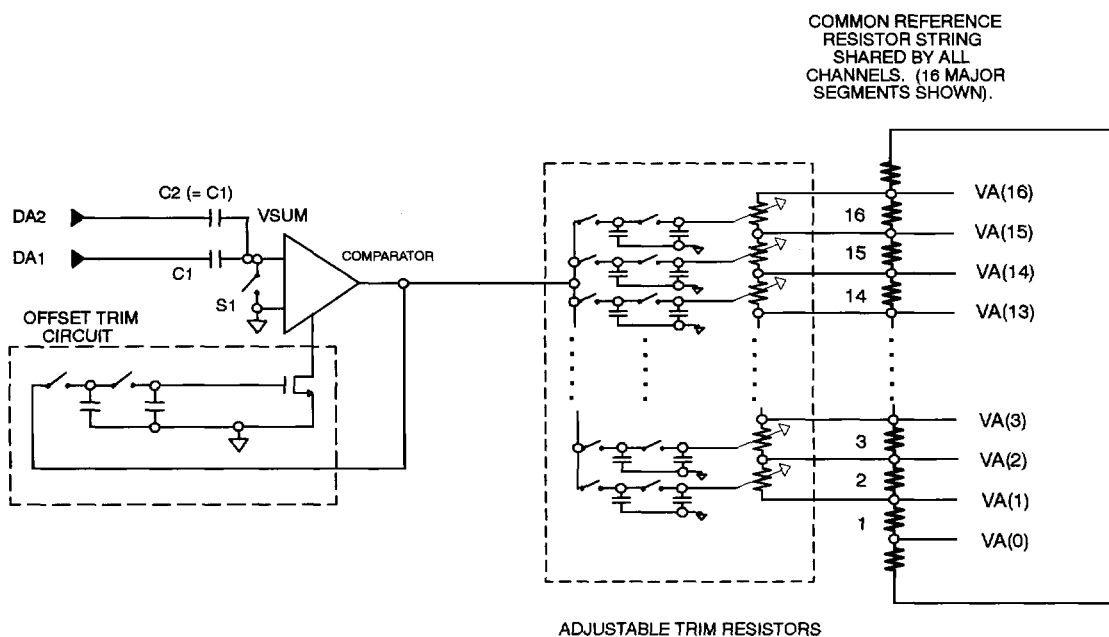
Two types of continuous automatic calibrations are done - the reference resistor string itself and each of the A/D channels. Calibration removes both non-linearity in the reference resistor string (correcting differential and integral non-linearity) and individual offsets in each of the 16 A/D channels (such offsets would cause a repeating pattern of code variation as the channels are multiplexed). Calibration is done by storing correction voltages on internal storage capacitors. Only a small voltage change on each capacitor is possible each correction cycle, which ensures stable maintenance of the correction voltages. Initial calibration can take as long as 168,000 clock cycles.

Calibration will be maintained as long as the clock is running. If the clock is interrupted, leakage will eventually affect the trim voltages stored on the internal capacitors, and some or all of the initial calibration wait time will be required to restore proper trim.

### Reference Resistor Ladder

The reference resistor ladder is continuously trimmed by looking at the 16 major segments of the common reference resistor ladder. The bottom segment is used as a standard, and the remaining 15 segments are tweaked to match the bottom segment. Calibration is done by means of voltage-controlled adjustable trim resistors in parallel with the 15 segments being trimmed (refer to Figure 7.)

Each round (phases 0 - 15) of clock phases adjusts one segment of the ladder. Since there are 15 segments to be trimmed, it takes 15 rounds to trim each of the 15 segments one time. There are 16 clocks in each round, so there are 240 clocks ( $=15 \times 16$ ) to trim the entire resistor ladder once. Since the permissible trim voltage changes are small, the user should allow for 168,000 clock cycles from the start-up to auto-calibrate the reference resistor ladder.



**Figure 7. Simplified DAC Resistor Ladder Auto-Calibration Circuit**

## A/D Channels :

Each A/D channel comparator is trimmed for offset and sampling capacitor mismatch just before it samples the input using the circuitry shown in *Figure 8*. since the permissible trim voltage changes are small, initial calibration takes a rather long time. The comparator calibration is impacted by the resistor string which is being simultaneously calibrated, so theoretical determination of the required comparator initial calibration time is difficult.

However, test results indicate that approximately 18,000 clock cycles are needed to begin producing recognizable outputs, and 42,000 clock cycles for more complete settling of the trim. After this time the reference resistor string is still undergoing initial trim, so integral non-linearities (INL) may still exist. This can create harmonics in the frequency domain and adversely impact SNR+distortion.

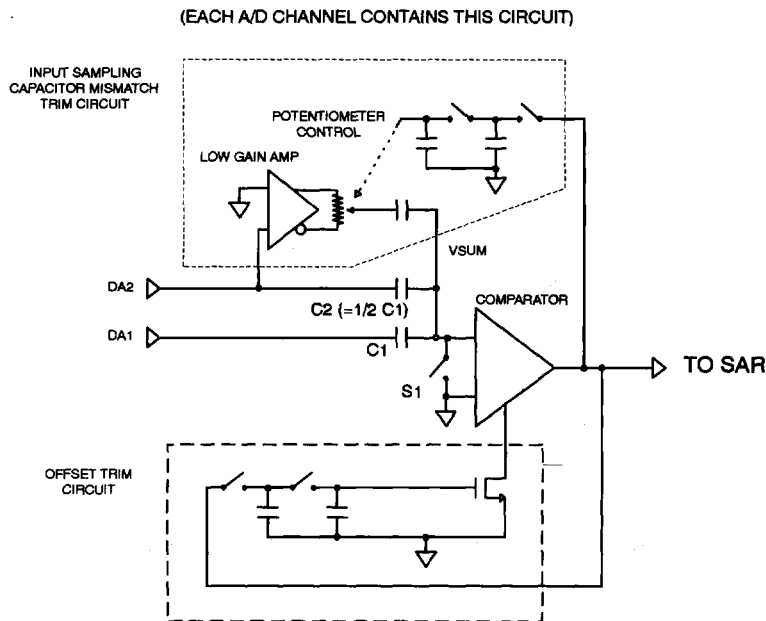


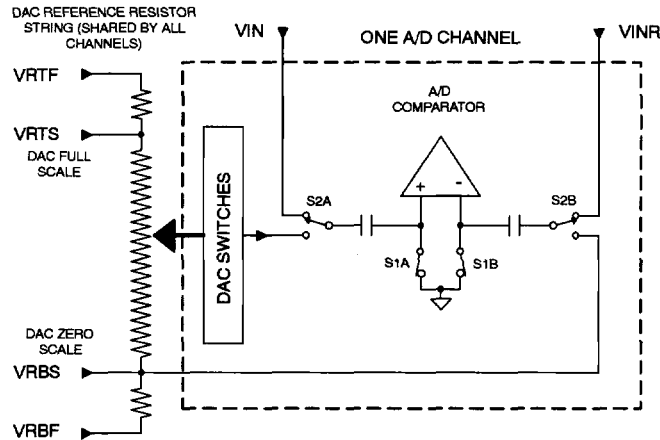
Figure 8. Simplified ADC Comparator Trimming Architecture

### Input Sampling Circuit for the A/D Channels

Figure 9. shows a simplified version of the input sampling circuit in each A/D channel. When sampling, S1A and S1B are closed. S2A and S2B are connected to VIN and VINR, respectively. Sampling is completed when S1A and S1B open. When converting, S2B is connected to VRBS, and S2A is connected to the DAC, which is controlled by the SAR.

Normally, VRBF is set to ground, and VRTF is driven by the on-chip buffer. While the actual conversion from sampled input to digital output is done in a single-ended

fashion, the input itself is sampled differentially - the difference between VIN and VINR is sampled. It is therefore theoretically possible to sample a differential signal, where both VIN and VINR are "active" (in that case VIN must be greater than VINR relative to ground, or an out of range condition will exist). However, best results are obtained if VINR is simply tied to VRBF (usually ground) or VRBS. This insures that the input common mode voltage of the A/D comparator will be proper (it's set during sampling through S1A and S1B).



**Figure 9. Simplified ADC Channel Input Sampling Circuit**

If VINR is tied to ground, the XRD6440 will give an output of :

zero scale : all 0's when VIN = 0v

full scale : all 1's when VIN = (VRTS - VRBS)

If VINR is tied to VRBS, the XRD6440 will give an output of:

zero scale : all 0's when VIN = VRBS

full scale : all 1's when VIN = VRTS

## Proper Setting of VRBF and VRTF Voltages

Proper setting of the voltages VRBF and VRTF is necessary to achieve full 10 bit dynamic range. VRTF can be set using either the internal voltage reference amplifier, or using an external buffer (see Figure 10. and Figure 11.) If using an external buffer, VRTS can be set more precisely by using VRTS as feedback to the external buffer. Likewise, VRBF can be forced with an external buffer, using VRBS as feedback. When not using the internal voltage reference amplifier, it must be disabled by connecting VFBR to VDD. This will not cause a conflict between the internal amplifier and the external buffer - the internal amplifier's output will become high impedance when the voltage on VFBR is higher than on VBG.

## VRTF

If VINR is tied to VRBS, VRTF should be set such that VRTS is equal to maximum VIN.

If VINR is tied to ground, VRTF should be set such that VRTS minus VRBS is equal to maximum VIN.

When using the internal amplifier, set VRTF to the desired value using the transfer function :

$$VRTF = VBG (1 + R2/R1) \quad \text{where VBG is nominally 1.24v}$$

The values in Figure 10., for example, would give VRTF = 3.968v = 1.24v x (1 + 11K/5K)

VRTS can be set more precisely by using an external buffer and known reference voltage VT (see Figure 11.)



## VRBF

For minimum use of external components, VRBF can be tied to ground (see Figure 10.) However, if a more precise VRBS voltage is needed, or if the minimum

expected voltage of VIN is not close to ground, then an external buffer and known reference voltage VB can be used (see Figure 11.) VINR can be tied to VRBS, and VRBS set with an external voltage source VB such that VRBS is at the expected minimum voltage of VIN.

CONNECTION DIAGRAM - USING INTERNAL AMPLIFIER

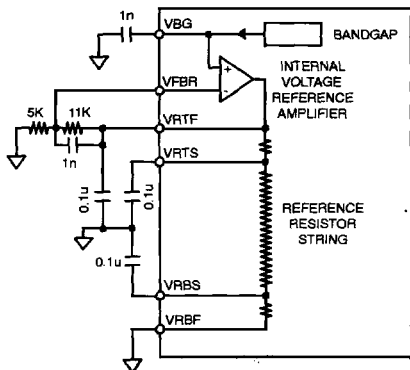


Figure 10. Circuit Diagram with Internal Amplifier

CONNECTION DIAGRAM - USING EXTERNAL BUFFERS

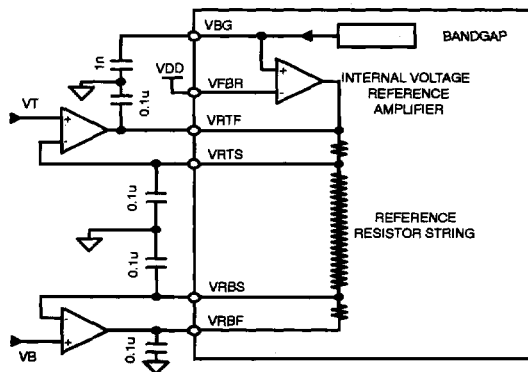


Figure 11. Circuit Diagram with External Amplifier

## Typical values for VRTS and VRBS

$$VRBS - VRBF = 0.024 \times (VRTF - VRBF)$$

$$VRTF - VRTS = 0.014 \times (VRTF - VRBF)$$

$$= 96\text{mV if } VRTF - VRBF = 4.0 \text{ volts}$$

$$= 56\text{mV if } VRTF - VRBF = 4.0 \text{ volts}$$

External buffers must be capable of driving the 500 ohm reference resistor string. With 4 volts between VRTS and VRBS, the buffers must be able to sink and source 8 mA.

## Board Layout Considerations

- 1) Sockets can degrade the A/D performance at these frequencies. Best results are obtained with the A/D soldered directly on the board.
- 2) Depending on the load seen by the output pins D0 - D9, it may be beneficial to latch the A/D output into digital latches placed fairly close to the A/D. D0 - D9 need only drive the inputs to the digital latches.
- 3) AGND and DGND pins for the A/D should be on the same ground plane. If digital output latches are used

to buffer the A/D from load, they should be on a separate ground plane. Ground planes should be generous.

- 4) Place 0.1μF power supply filtering caps as close to the power supply pins on the XRD6440 as possible. The connection from the caps to the ground plane should also be as short as possible. The same holds true for the caps shown in Figure 10. and Figure 11.

- 5) Both the clock and VIN lines should be shielded if possible. VIN must be free of noise for good results. The clock line must be prevented from propagating noise elsewhere, but it must also be prevented from *picking up* noise, which could be seen by the A/D as clock jitter.

## ANALOG INPUT

The operational range of the analog input, VIN, varies from VRT(+) to VRB(-) voltage references. Since these reference voltages set the full scale(all 1 code) and zero scale(all 0 code) of ADC, if VIN is driven above VRT(+) or below VRB(-), output produces full scale or zero scale codes respectively.

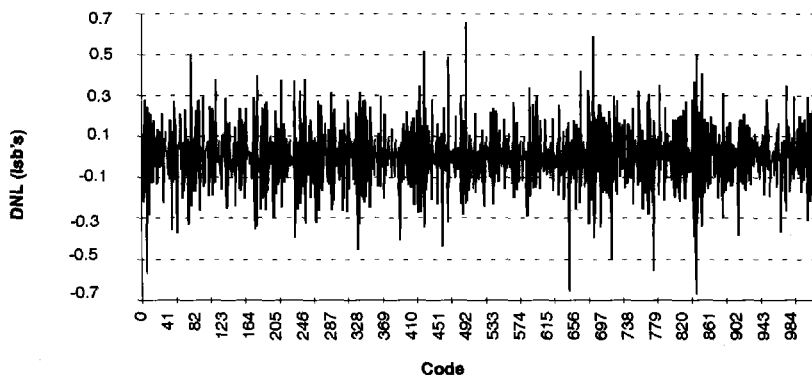
The input drive requirements are minimal due to the low input capacitance (5pF-typ) and high input resistance

(34 K $\Omega$ -typ) at this pin compared to the most other ADCs. This is made possible by the efficient design of sampling track-and-hold amplifiers(THAs) tied to this pin.

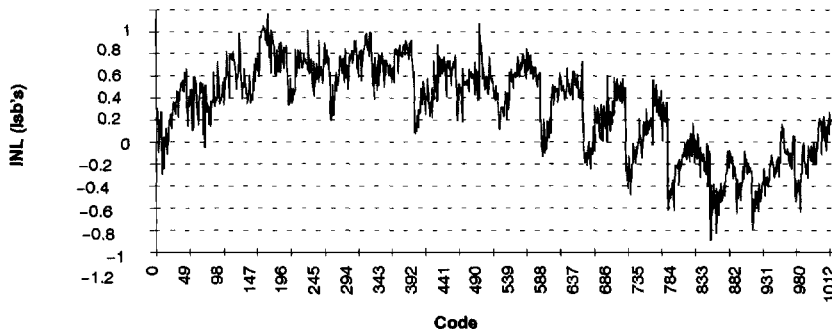
If this pin is to be driven above the analog power supply voltage( $AV_{DD}$ ), the input should be protected from a potential latch-up by using in series a 50 $\Omega$  resistor and a clamping diode.

## CALIBRATION CYCLE

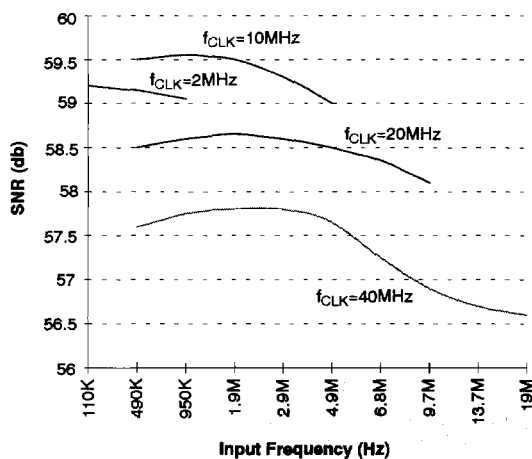
The XRD6440 incorporates a proprietary auto-calibration circuit which continuously adjusts the reference ladder, offset and gain of the sampling comparators. The auto-calibration algorithm is design to re-calibrate these errors by approximately 1/16 LSB per clock cycle to insure and maintain 10-bit accuracy over time and temperature changes.



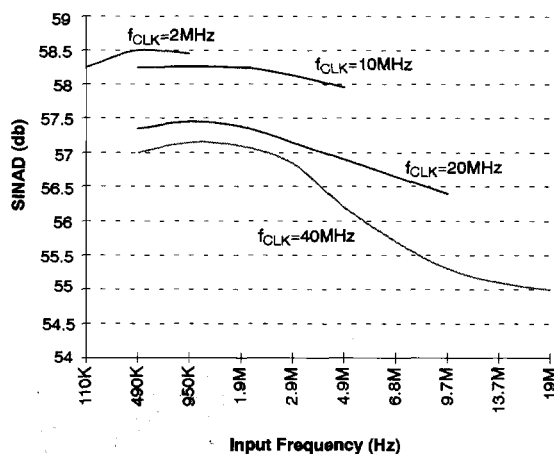
Graph 1. DNL  
 $f_{SAMPLE} = 40MHz$ ,  $f_{IN} = 490Khz$



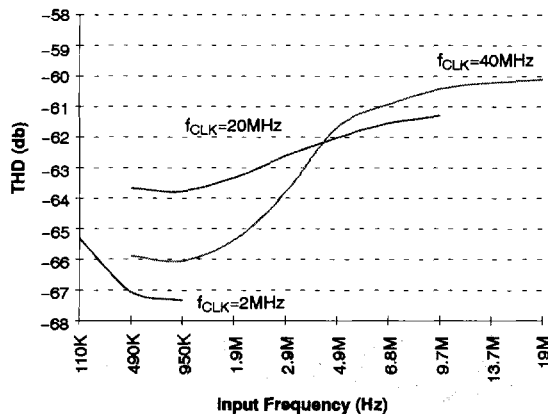
Graph 2. INL  
 $f_{SAMPLE} = 40MHz$ ,  $f_{IN} = 490Khz$



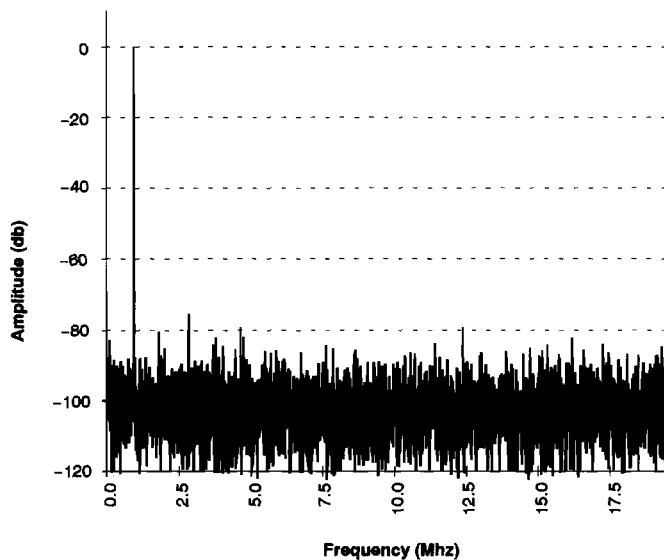
**Graph 3. SNR vs.  $f_{IN}$**   
 $f_{SAMPLE} = 2\text{MHz}, 10\text{MHz}, 20\text{MHz}, 40\text{MHz}$



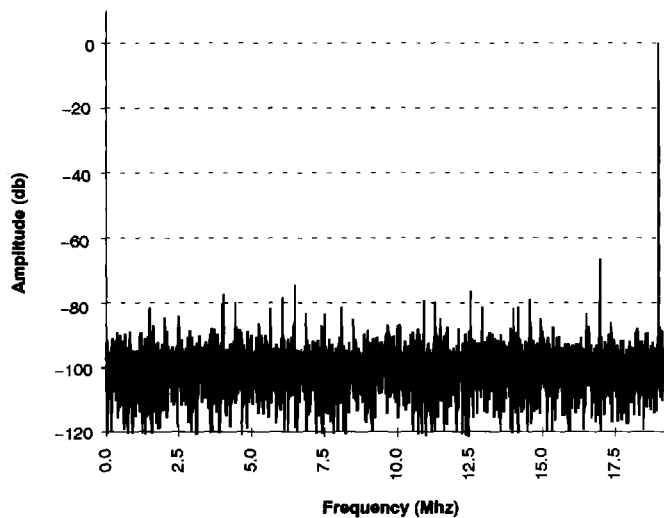
**Graph 4. SINAD vs.  $f_{IN}$**   
 $f_{SAMPLE} = 2\text{MHz}, 10\text{MHz}, 20\text{MHz}, 40\text{MHz}$



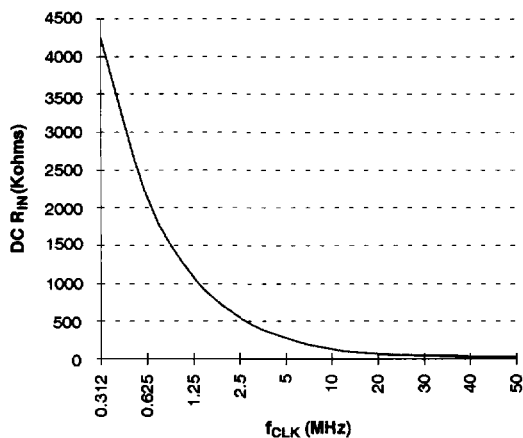
**Graph 5. THD vs.  $f_{IN}$**   
 $f_{SAMPLE} = 2\text{MHz}, 10\text{MHz}, 20\text{MHz}, 40\text{MHz}$



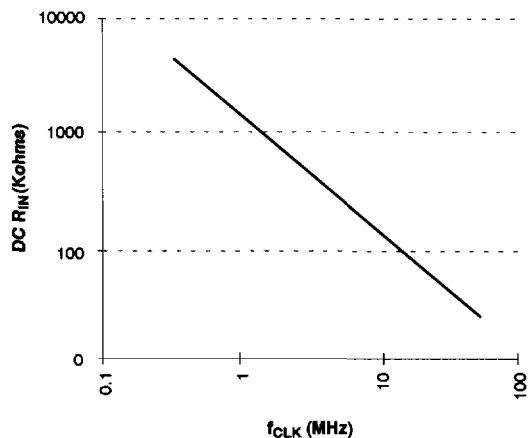
**Graph 6.FFT**  
 $f_{\text{SAMPLE}} = 40\text{MHz}$ ,  $f_{\text{IN}} = 950\text{KHz}$



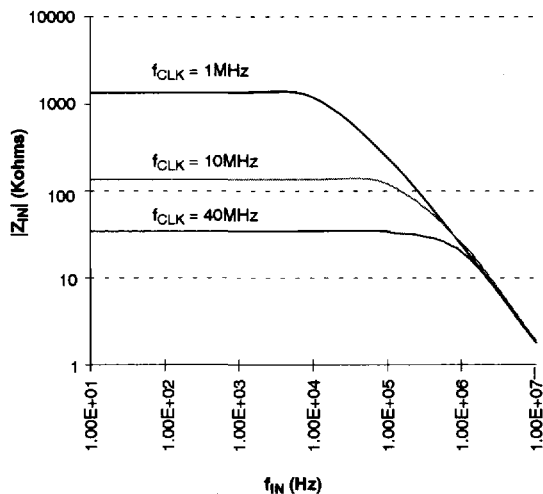
**Graph 7.FFT**  
 $f_{\text{SAMPLE}} = 40\text{MHz}$ ,  $f_{\text{IN}} = 19\text{MHz}$



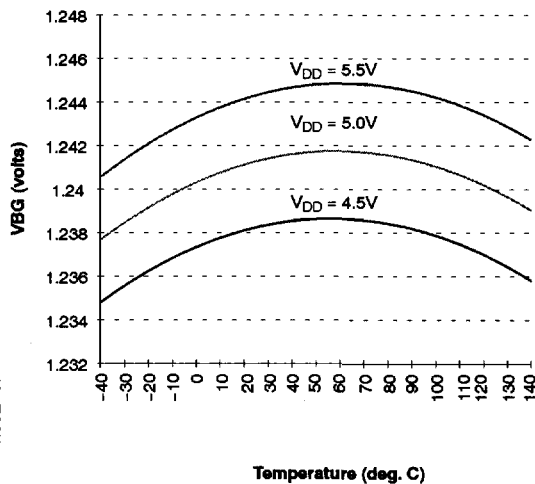
**Graph 8.DC  $R_{IN}$  vs.  $f_{CLK}$**



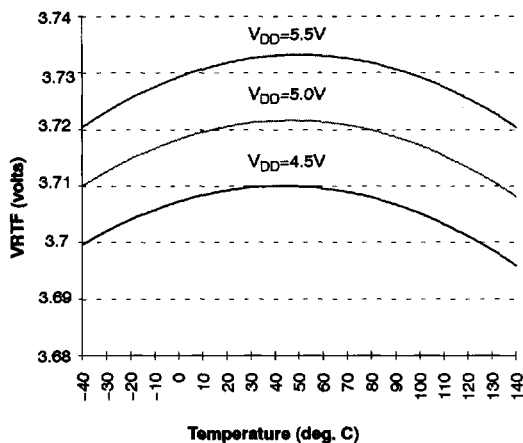
**Graph 9.DC  $R_{IN}$  vs.  $f_{CLK}$   
Log - Log Scale**



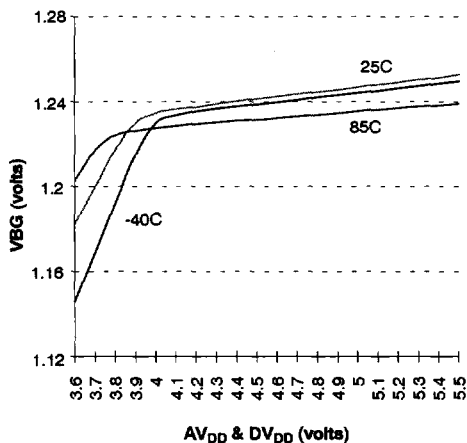
**Graph 10.  $|Z_{IN}|$  vs.  $f_{IN}$   
Log - Log Scale**



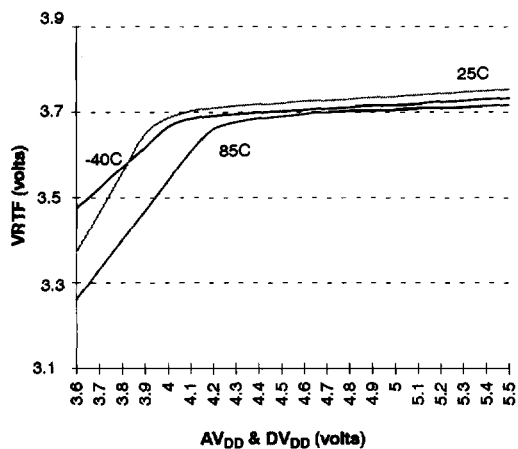
**Graph 11.VBG vs. TEMP  
 $V_{DD} = 4.5V, 5.5V$**



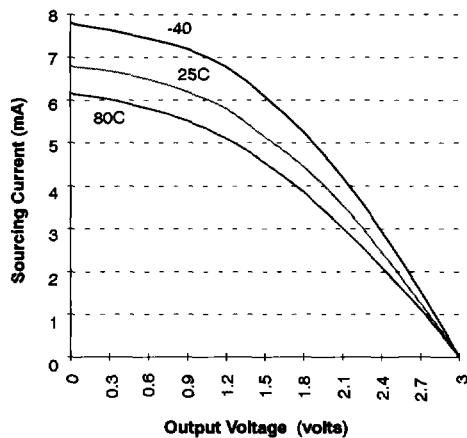
Graph 12.VTRF vs. TEMP  
 $V_{DD} = 4.5V, 5.5V$



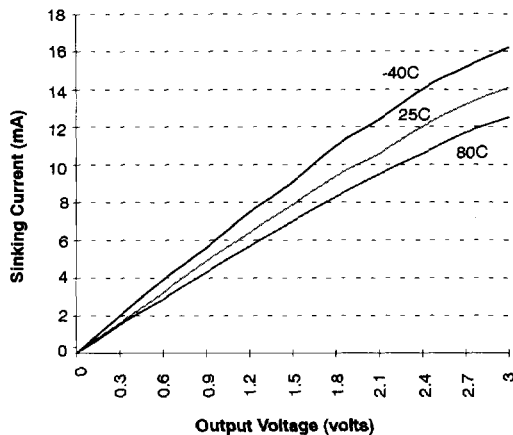
Graph 13.VBG vs.  $AV_{DD} (=DV_{DD})$



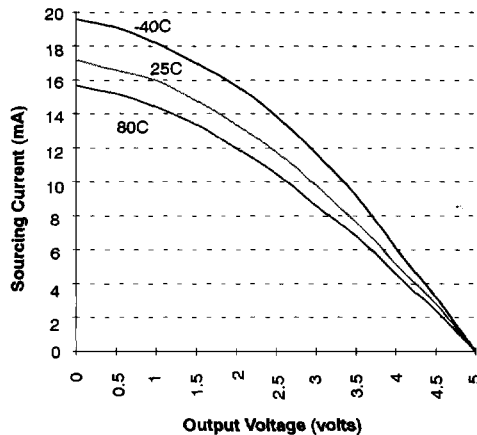
Graph 14.VTRF vs.  $AV_{DD} (=DV_{DD})$   
VTRF Set for 3.7V Using External 10K/5K



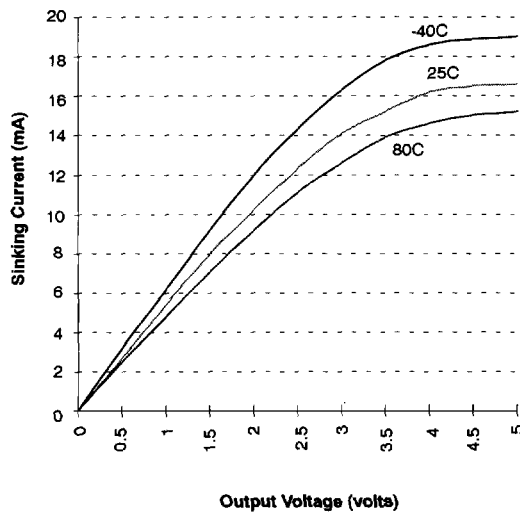
Graph 15.Digital Output Source Current  
 $DOV_{DD} = 3.0V$



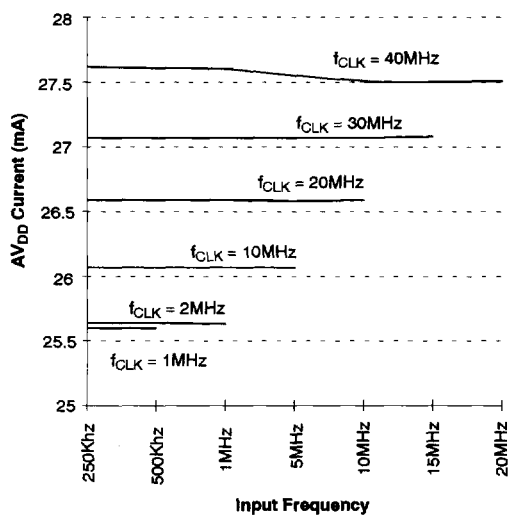
**Graph 16. Digital Output Sink Current**  
**DOV<sub>DD</sub> = 3.0V**



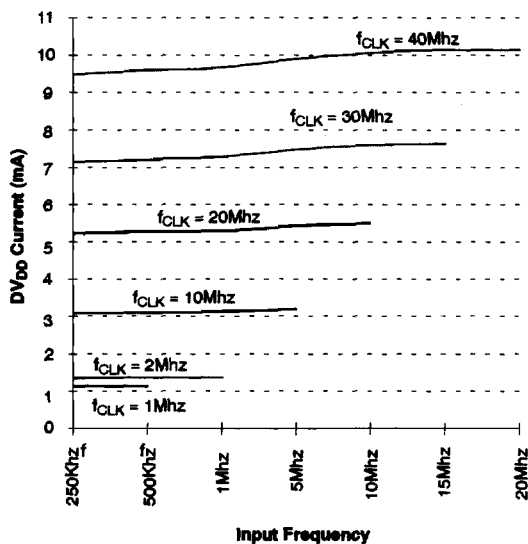
**Graph 17. Digital Output Source Current**  
**DOV<sub>DD</sub> = 5.0V**



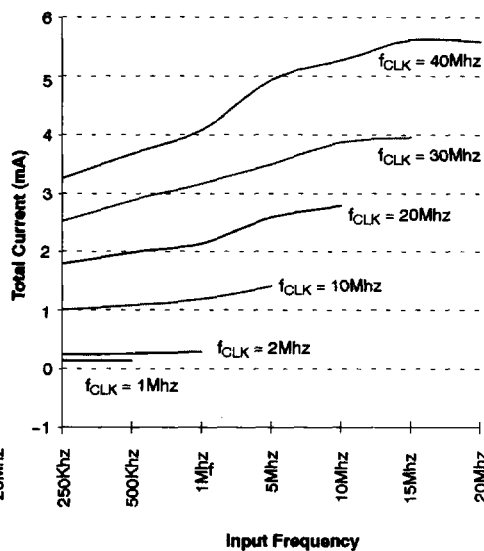
**Graph 18. Digital Output Sink Current**  
**DOV<sub>DD</sub> = 5.0V**



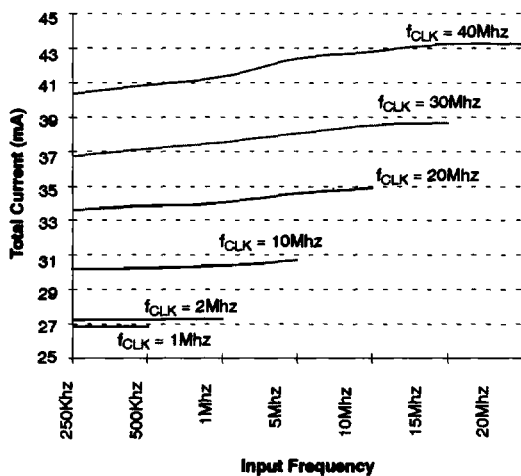
**Graph 19. I(AV<sub>DD</sub>) vs. f<sub>IN</sub>**  
**f<sub>IN</sub> = 1, 2, 10, 20, 30, 40MHz**



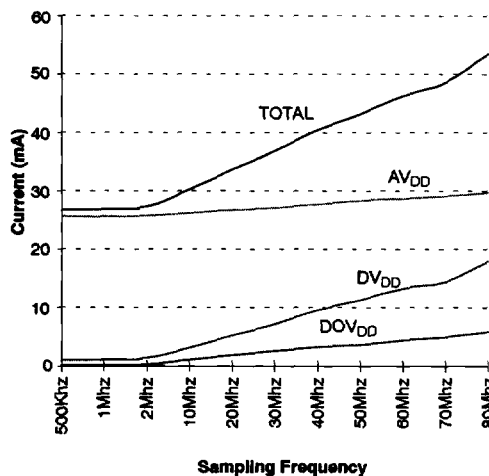
Graph 20. I(DV<sub>DD</sub>) vs.  $f_{IN}$   
 $f_{IN} = 1, 2, 10, 20, 30, 40\text{MHz}$



Graph 21. I(DOV<sub>DD</sub>) vs.  $f_{IN}$   
 $f_{SAMPLE} = 1, 2, 10, 20, 30, 40\text{MHz}$

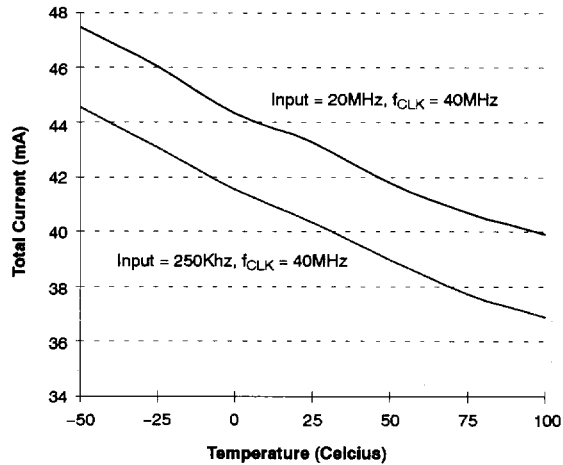


Graph 22. I(TOTAL) vs.  $f_{IN}$   
 $f_{SAMPLE} = 1, 2, 10, 20, 30, 40\text{MHz}$



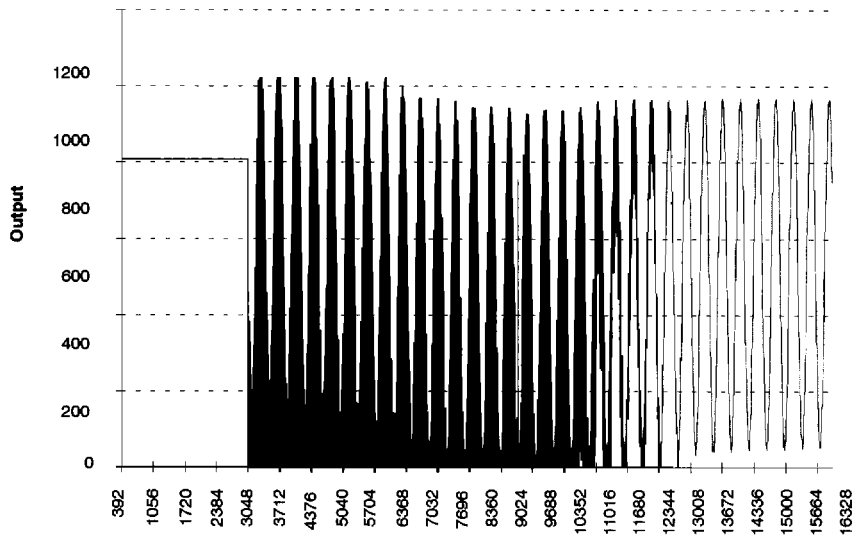
Graph 23. CURRENT vs.  $f_{SAMPLE}$   
 $f_{IN} = 250\text{KHz}$



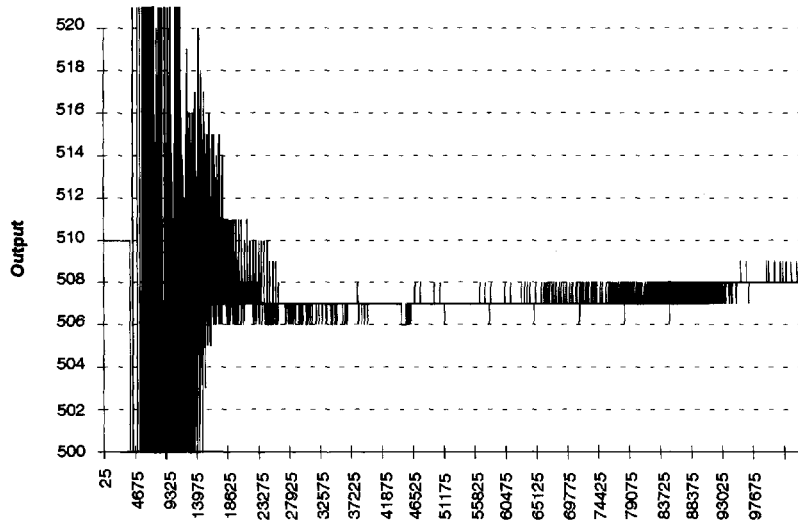


**Graph 24.I(TOTAL) vs. Temperature**  
 $f_{IN} = 250\text{Khz}$ ,  $20\text{MHz}$ ,  $f_{SAMPLE} = 40\text{MHz}$

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**Graph 25.A/D During Initial Start-up**  
 $f_{SAMPLE} = 40\text{MHz}$ ,  $f_{IN} = 100\text{Khz}$  Sine Wave



**Graph 26.A/D During Initial Start-up**  
 $f_{\text{SAMPLE}} = 40\text{MHz}$ ,  $f_{\text{IN}} = \text{DC}$