YAMAHA

YGV627

AVDP3E

Advanced Video Display processor 3 Enhanced

ν OUTLINE

YGV627 is a VDP (Video Display Processor) that realizes higher resolution, multi-color and high speed drawing by adopting a synchronous DRAM as the video memory, while maintaining the register compatibility with YGV617B that is used for controlling the high minuteness On Screen Display (OSD).

Since the device is capable of displaying bitmap images with various resolutions ranging from NTSC to SVGA on the monitors with any size of screen including wide screen, it can be used for controlling OSD for various display units. Also, it is capable of representation of varied images in accordance with the application because numerous number of colors can be selected such as the one in the range from 16 to 65536 RGB color display, or natural image display using YCrCb.

In addition, the existing system can be up-graded easily thanks to the basic features from YGV617B such as a high speed drawing function, character drawing function, synchronization with external video signal, digital video input / output function, and hardware cursor display function.

ν FEATURES

YGV627 is capable of selecting two modes by using the setting of $\overline{\text{ENH}}$ pin.

For convenience, the case of using $\overline{\text{ENH}}$ pin with LOW level (enabled) is referred to as “expansion mode” in this document. In the expansion mode, all the functions can be used.

The case of using $\overline{\text{ENH}}$ pin with HIGH level (disabled) is referred to as “compatibility mode”. In the compatibility mode, the software compatibility with YGV617B is maintained, but the functions enhanced for YGV617B cannot be used. These modes should be used in accordance with the purpose of the application of this device.

[Display functions]

- Three screen configuration including bitmap screen, sprite cursor screen and external input video screen (or single color border screen)
- Monitor synchronization frequency, dot clock frequency, and display screen resolution can be specified optionally.
- Display dot clock up to 40 MHz (Example of resolution: NTSC, PAL, VGA, SVGA, NTSC wide, and VGA wide)
- Support with progressive scanning and interlaced scanning
- Resolution of sprite cursor screen is 32 X 32 dots. (The sprite cursor can also be used as cross-hair line cursor.)
- Smooth hardware scroll function
- Upper / lower two division display on the bitmap screen (The two sections can be scrolled independently).
- 256 words X 16 bits CLUT is built-in (The number of display colors of 32768 colors or 65536 colors can be selected.)
- Display colors: 16 palette color, 256 palette color, 32768 RGB color, 65536 RGB color, YCrCb422 (ITU601)
- YCrCb(ITU601) -to-8 bit RGB decoder is built-in.
- α blending function that mixes with external input screen or single color border screen. (64 intensity levels)
- Dot clock generation with built-in PLL circuit
- Generates dot clock that synchronizes with HSYNC of external video signal.
- Generates dot clock that synchronizes with external input clock. (such as sub-carrier clock)

YAMAHA CORPORATION

YGV627 CATALOG
CATALOG No.: LSI-4GV627A60
2005.1

[Drawing functions]

● Commands	Block transfer by word (CPU to VRAM, VRAM to CPU, VRAM to VRAM) Font drawing, dot drawing and rectangular drawing.
● Drawing attribute	Sets drawing clip area, drawing offset or drawing page, and designates bit mask, color mask, logical operation (NOT, AND, OR, EOR etc.), or direction of transfer.

[Operational clock]

● System clock (clock for drawing system):	up to 33 MHz
● Dot clock (clock for display system):	up to 40 MHz

[CPU interface]

- 16 bit or 8 bit asynchronous interface
- Provided with a video memory space up to 8M bytes and internal register space of 128 bytes.
- The video memory space and internal register space can be mapped indirectly with 16 byte registers.
- Built-in data buffer for memory space access and built-in data FIFO for drawing commands
- CPU interruption based on various conditions of display and drawing
- DMA transfer of drawing command data can be made when connected with external DMA controller

[Video memory interface]

● Connected memory:	16M bits SDRAM (512k words X 16 bits X 2 banks) 1 piece or 64M bits SDRAM (1M words X 16 bits X 4 banks) 1 piece
● SDRAM clock:	up to 66 MHz (System clock multiplied by 2 or 4)

- Built-in FIFO for display data improves the drawing access efficiency and realizes high speed drawing.

[Monitor interface]

- Analog RGB output with built-in DAC (8 bits for RGB individually)
- Digital video input / output (6 bits for RGB individually)
- Equipped with sub-carrier clock output, dot clock output, sync signal output, YS and attribute output pins.

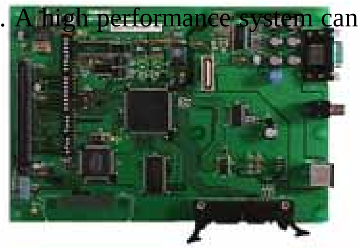
[Others]

- Package: 176LQFP (YGV627-V)
- CMOS, 3.3V single power supply
- Operating temperature range: −40 to +85 °C

Supplementary information:

For YGV627, Application Manual that details the specifications of the device and the evaluation board (MSY627DB01/02) are available in addition to this brochure.

The evaluation board is equipped with an SDRAM of 8 MB as a video memory. A high performance system can be realized when it is used with Hitachi's CPU board, Super H Solution Engine.

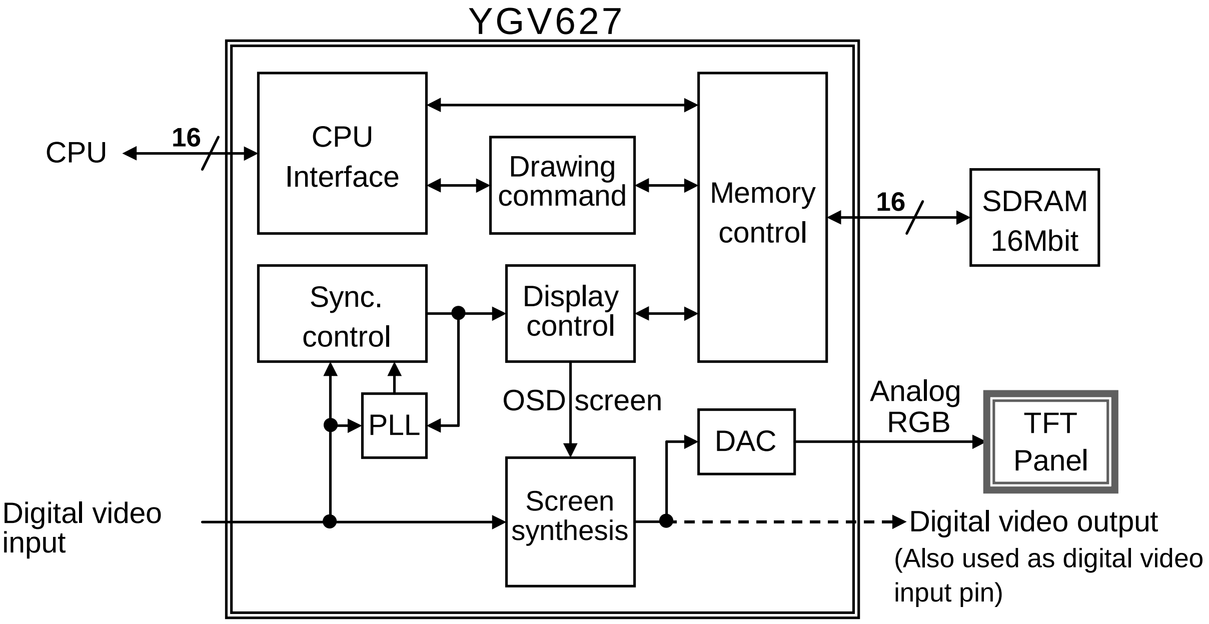


The device driver provided by Yamaha and attached to the evaluation board consists of the main body of the driver and API related layers, allowing the user to build it into the system easily according to the environment.

For the details of these products, inquire of the sales agents or our business offices.

For CPU board, inquire of: Hitachi ULSI Systems Co., Ltd.
Tel:+81-42-351-6600

ν BLOCK DIAGRAM


YGV627
CPU
16
CPU Interface
Drawing command
Memory control
16
SDRAM 16Mbit
Sync. control
Display control
PLL
OSD screen
DAC
Analog RGB
TFT Panel
Digital video input
Screen synthesis
Digital video output
(Also used as digital video input pin)

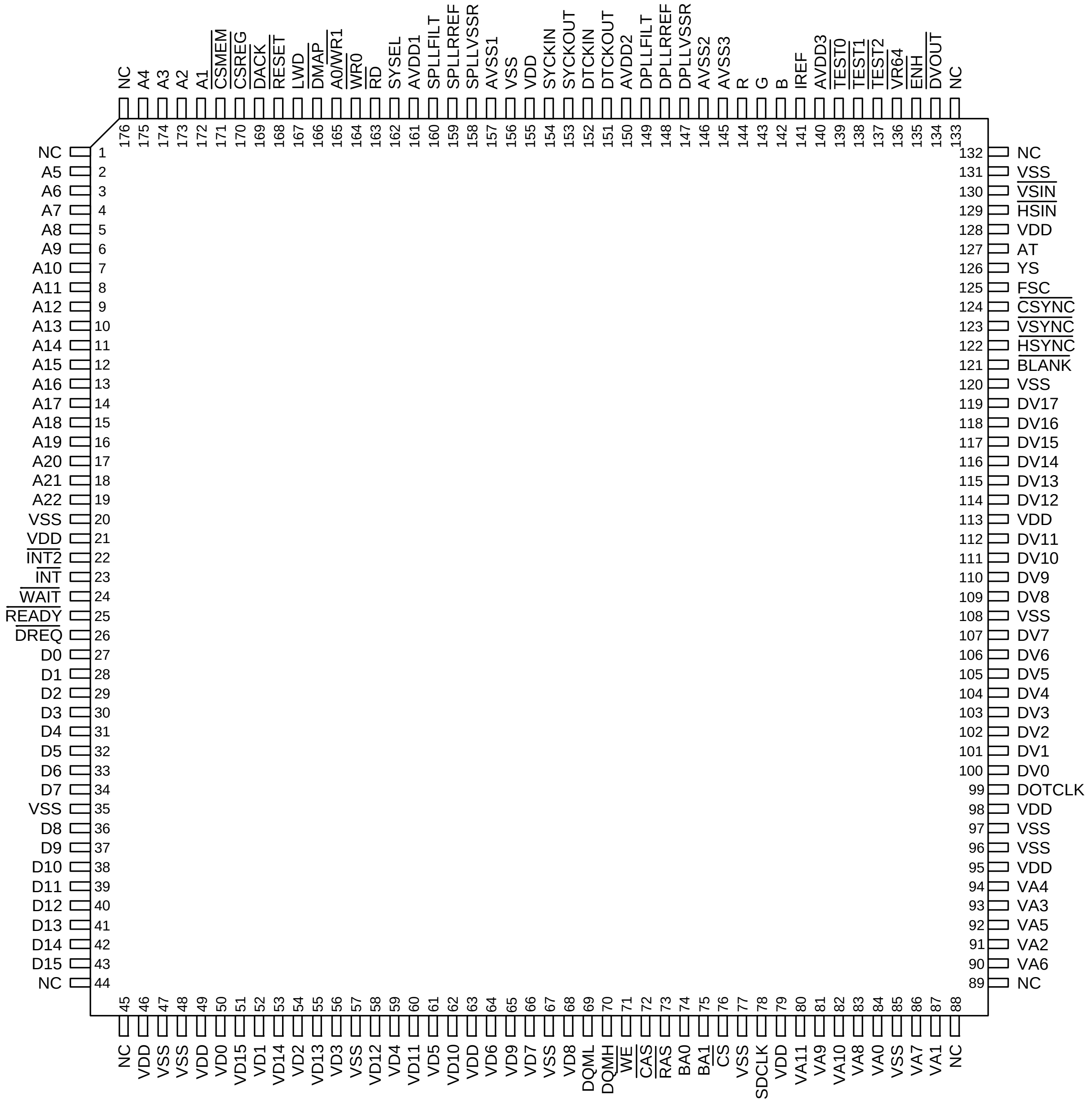
Internal block diagram

YGV627 is connected to the external memory bus of CPU as an external I/O device. As a video memory, SDRAM of up to 64M bits can be connected to local memory bus of YGV627 to send bitmap image data stored in the video memory into monitor as RGB signal in accordance with display scan timing.

YGV627 stores image data from CPU to the video memory by accessing video memory directly through CPU interface or by accessing the video memory using internal drawing command that transfers the data by block.

YGV627 has a function that synthesizes external images with bitmap image of YGV627 on the screen by synchronizing the scan timing of YGV627 with display timing of external video signals.

ν PIN ASSIGNMENT


1 NC
2 A5
3 A6
4 A7
5 A8
6 A9
7 A10
8 A11
9 A12
10 A13
11 A14
12 A15
13 A16
14 A17
15 A18
16 A19
17 A20
18 A21
19 A22
20 VSS
21 VDD
22 INT2
23 INT
24 WAIT
25 READY
26 DREQ
27 D0
28 D1
29 D2
30 D3
31 D4
32 D5
33 D6
34 D7
35 VSS
36 D8
37 D9
38 D10
39 D11
40 D12
41 D13
42 D14
43 D15
44 NC
45 NC
46 VDD
47 VSS
48 VSS
49 VDD
50 VD0
51 VD15
52 VD1
53 VD14
54 VD2
55 VD13
56 VD3
57 VSS
58 VD12
59 VD4
60 VD11
61 VD5
62 VD10
63 VDD
64 VD6
65 VD9
66 VD7
67 VSS
68 VD8
69 DQML
70 DQMH
71 WE
72 CAS
73 RAS
74 BA0
75 BA1
76 CS
77 VSS
78 SDCLK
79 VDD
80 VA11
81 VA9
82 VA10
83 VA8
84 VA0
85 VSS
86 VA7
87 VA1
88 NC
89 NC
90 VA6
91 VA2
92 VA5
93 VA3
94 VA4
95 VDD
96 VSS
97 VSS
98 VDD
99 DOTCLK
100 DV0
101 DV1
102 DV2
103 DV3
104 DV4
105 DV5
106 DV6
107 DV7
108 VSS
109 DV8
110 DV9
111 DV10
112 DV11
113 VDD
114 DV12
115 DV13
116 DV14
117 DV15
118 DV16
119 DV17
120 VSS
121 BLANK
122 HSYNC
123 VSYNC
124 CSYNC
125 FSC
126 YS
127 AT
128 VDD
129 HSIN
130 VSIN
131 VSS
132 NC
133 NC
134 DVOUT
135 ENH
136 VR64
137 TEST2
138 TEST1
139 TEST0
140 AVDD3
141 IREF
142 B
143 G
144 R
145 AVSS3
146 AVSS2
147 DPLLVSSR
148 DPLLRREF
149 DPLLFILT
150 AVDD2
151 DTCKOUT
152 DTCKIN
153 SYCKOUT
154 SYCKIN
155 VDD
156 VSS
157 AVSS1
158 SPLLVSSR
159 SPLLRREF
160 SPLLFILT
161 AVDD1
162 SYSEL
163 RD
164 WR0
165 A0/WR1
166 DMAP
167 LWD
168 RESET
169 DACK
170 CSREG
171 CSMEM
172 A1
173 A2
174 A3
175 A4
176 NC

Top view

ν PIN FUNCTIONS

<CPU interface>

λ D15–0 （I/O: PULL UP）

This is a data bus for connecting with external processor. D15–D8 are not used when the CPU bus with 8 bit type (when low level is inputted to LWD). At this time, keep the D15–D8 open. These pins are provided with pull-up resistors respectively.

λ A22–1 （I）

This is an address bus to be connected with external general purpose microcomputer. In the indirect access mode (high level inputted to $\overline{\text{DMAP}}$ pin), input to A22–A4 pins are ignored when accessing $\overline{\text{CSREG}}$ space.
In the direct access mode (low level inputted to $\overline{\text{DMAP}}$ pin), input to A22–A8 pins are ignored when accessing $\overline{\text{CSREG}}$ space.
YGV627 can be used as a YGV617B compatible device when A22 and A21 pins are fixed to low level. Unused pins must be set to low level or high level.

λ $\overline{\text{CSREG}}$ （I）

It is a chip select signal input to register space (I/O). When this chip select signal is active, the read / write pulses inputted are made valid so that the registers in the YGV627 are accessed.
The function of this pin is the same as that of $\overline{\text{CSIO}}$ pin of YGV617B.

λ $\overline{\text{CSMEM}}$ （I）

This is a chip select signal input pin for video memory port. The read / write pulse inputted while this signal is active can be used to directly access the video memory controlled by YGV627.
It is possible not to use $\overline{\text{CSMEM}}$ because the video memory can also be accessed from registers. In such case, it is necessary to input high level to $\overline{\text{CSMEM}}$ pin.

λ A0 / $\overline{\text{WR1}}$, $\overline{\text{WR0}}$ （I）

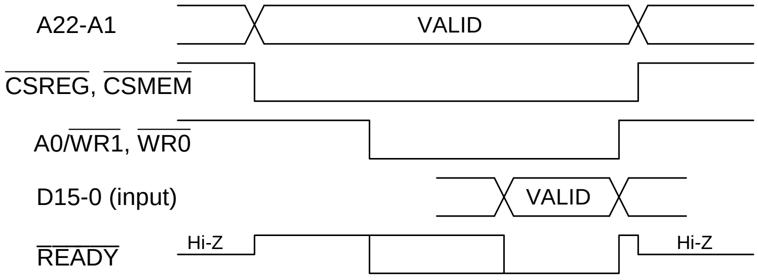
When chip select input is active, these pins control write access to YGV627.
D15–D8 are controlled by A0 / $\overline{\text{WR1}}$, and D7–D0 by $\overline{\text{WR0}}$.
When the CPU is 8 bit type, A0 / $\overline{\text{WR1}}$ functions as CPU address bit 0.

λ $\overline{\text{RD}}$ （I）

When chip select input is active, $\overline{\text{RD}}$ controls read access from YGV627.
D15–D0 are in Output State in the period while both this signal and chip select signals are active.

λ $\overline{\text{READY}}$ （O: PULL UP, 3-state output）

This is data ready signal output to CPU. The $\overline{\text{READY}}$ signal is made low when the internal state of YGV627 is accessible. $\overline{\text{READY}}$ is a 3-state output. When $\overline{\text{CSREG}}$ or $\overline{\text{CSMEM}}$ is not active, it is high impedance state, and when $\overline{\text{CSREG}}$ or $\overline{\text{CSMEM}}$ is active and $\overline{\text{RD}}$ or $\overline{\text{WR1}}$, $\overline{\text{WR0}}$ is not active, high level is outputted from $\overline{\text{READY}}$.
Some CPU must use $\overline{\text{WAIT}}$ signal instead of this signal.


A22-A1
VALID
$\overline{\text{CSREG}}$, $\overline{\text{CSMEM}}$
A0/$\overline{\text{WR1}}$, $\overline{\text{WR0}}$
D15-0 (input)
VALID
$\overline{\text{READY}}$
Hi-Z
Hi-Z

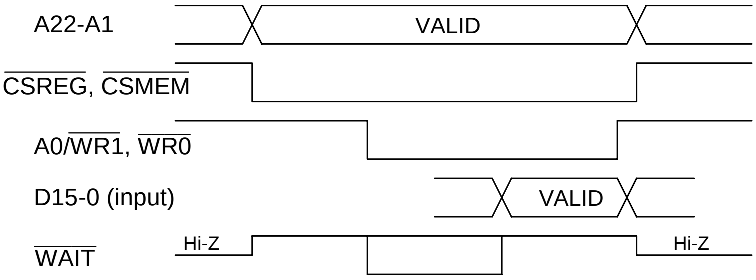
$\overline{\text{READY}}$ signal at write access

λ **$\overline{\text{WAIT}}$ （O: PULL UP, 3-state output）**

This is data wait signal output to CPU. When $\overline{\text{CSREG}}$ or $\overline{\text{CSMEM}}$ is active, the level of $\overline{\text{WAIT}}$ signal is made low once with respect to $\overline{\text{RD}}$ or $\overline{\text{WR1}}$, $\overline{\text{WR0}}$ in accordance with the internal state of YGV627, and in accessible state, it outputs high level.

When $\overline{\text{CSREG}}$ or $\overline{\text{CSMEM}}$ is not active, it is in high impedance state, and when $\overline{\text{CSREG}}$ or $\overline{\text{CSMEM}}$ is active and $\overline{\text{RD}}$ or $\overline{\text{WR1}}$, $\overline{\text{WR0}}$ is not active, high level is outputted from this pin.

Some CPU must use $\overline{\text{READY}}$ signal instead of this signal.



$\overline{\text{WAIT}}$ signal at write access

λ **$\overline{\text{INT}}$ （O: Open drain output）**

This is interrupt request signal output to CPU.

This signal is made low when the internal state of YGV627 coincides with the setting conditions of registers.

This signal is reset with access to YGV627's internal register.

λ **$\overline{\text{INT2}}$ （O: High speed bus interrupt output）**

This is an interrupt request signal output to CPU, and its output logical value is the same as that of $\overline{\text{INT}}$.

For high speed CPU bus, this output signal is used to avoid the influence of transit time caused by the pull-up resistor when the interrupt signal is negated.

Use $\overline{\text{INT}}$ or $\overline{\text{INT2}}$ in accordance with the requirement of the system into which the YGV627 is built-in.

λ **LWD （I: PULL UP）**

This is used to select width of CPU data bus.

When this signal is high level input, the device is compatible with 16 bit system and when low level input, the device is compatible with 8 bit system respectively.

Since LWD is used for selection of a mode, always fix it to either level.

λ **$\overline{\text{RESET}}$ （I: PULL UP, with Schmitt）**

Initial reset signal is inputted to $\overline{\text{RESET}}$. The reset signal input resets the internal state of the device and the internal registers are cleared to "0". (Some registers are loaded with initial value.)

Be sure to input the reset signal after power up.

λ **$\overline{\text{DREQ}}$ （O）**

$\overline{\text{DREQ}}$ outputs command data request signal to external DMA controller.

λ **$\overline{\text{DACK}}$ （I: PULL UP）**

Command data transfer permission signal is inputted to $\overline{\text{DACK}}$ in response to $\overline{\text{DREQ}}$ signal to external DMA controller.

λ **$\overline{\text{DMAP}}$ （I: PULL UP）**

$\overline{\text{DMAP}}$ is used to select a register space mapping method.

When high level is inputted, 16 byte indirect mapping is selected. When low level is inputted, all the registers except CLUT are mapped directly in the 128 byte space. The input to $\overline{\text{DMAP}}$ determines the valid address when $\overline{\text{CSREG}}$ signal is active.

$\overline{\text{DMAP}}$ input signal is valid regardless of the state of $\overline{\text{ENH}}$ input signal.

When using YGV627 in YGV617B compatibility mode, input high level to $\overline{\text{DMAP}}$.

Since $\overline{\text{DMAP}}$ is for selection of a mode, always fix it to either level.

λ **$\overline{\text{ENH}}$ （I: PULL UP）**

This signal permits enhanced functions for YGV617B.

When high level is inputted, only the registers that are compatible with YGV617B are made valid, and the function of the enhanced registers are fixed to their default values. When low level is inputted, the function of the enhanced register is made valid.

This pin selects enable / disable of the enhanced functions and determines SDRAM access timing at the same time. In compatibility mode, the timing of access to SDRAM is equal to that of the performance of YGV617B, but in enhancement mode, the access performance is doubled.

Since $\overline{\text{ENH}}$ is for selection of a mode, always fix it to either level.

< Video memory interface>

λ **BA1–0, VA11–VA0 （O）**

These pins output address for SDRAM that is used as a video memory controlled by YGV627.

They output row address and column address on time sharing basis. BA1 and BA0 output bank address. However, when $\overline{\text{VR64}}$ is a high level input (16M bits SDRAM is connected), VA11 becomes bank select.

When a read command or write command is sent to the SDRAM, VA10 functions as auto-precharge enable.

Since these pins are always driven by YGV627, VRAM halt function of YGV617B cannot be used.

λ **VD15–VD0 （I/O: PULL UP）**

These pins constitute a data bus for SDRAM that is used as video memory controlled by YGV627.

VRAM halt function of YGV617B cannot be used.

λ **$\overline{\text{RAS}}$ （O）**

$\overline{\text{RAS}}$ outputs row address strobe signal for SDRAM that is used as a video memory controlled by YGV627.

Since $\overline{\text{RAS}}$ is always driven by YGV627, VRAM halt function of YGV617B cannot be used.

λ **$\overline{\text{CAS}}$ （O）**

$\overline{\text{CAS}}$ outputs column address strobe signal for SDRAM that is used as a video memory controlled by YGV627.

Since $\overline{\text{CAS}}$ is always driven by YGV627, VRAM halt function of YGV617B cannot be used.

λ **$\overline{\text{WE}}$ （O）**

$\overline{\text{WE}}$ outputs write strobe signal for SDRAM that is used as a video memory controlled by YGV627.

Since $\overline{\text{WE}}$ is always driven by YGV627, VRAM halt function of YGV617B cannot be used.

λ **DQMH, DQML （O）**

These pins output data mask signal for SDRAM that is used as a video memory controlled by YGV627.

DQMH is for VD15 – VD8, and DQML is for VD7–VD0.

λ **$\overline{\text{CS}}$ （O）**

This pin outputs chip select signal for SDRAM that is used as a video memory controlled by YGV627.

YGV627 requires connection to SDRAM because the device uses $\overline{\text{CS}}$ control for access to SDRAM for power saving purpose and against switching noise.

λ **SDCLK （O）**

This pin outputs clock for SDRAM that is used as a video memory controlled by YGV627.

Every output signal connected to SDRAM is outputted synchronizing with the rising edge of this clock. The read data from SDRAM is latched in the YGV627 at the rising edge of this clock. The clock enable pin of SDRAM should always be used in enable state.

λ **$\overline{\text{VR64}}$ （I: PULL UP）**

High level is inputted when the capacity of SDRAM that is used as a video memory controlled by YGV627 is 16M bits, or low level is inputted when the capacity is 64M bits. This signal determines the function of signal outputted from BA1, BA0, and VA11–VA0 pins. Connect with the SDRAM as specified below.

Since this pin is for selection of a mode, always fix it to either level.

☞ $\overline{\text{VR64}}$ = “H” (when connected with 16M bits SDRAM)

YGV627 pins	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	BA1	BA0	VA11	VA10	VA9	VA8	VA7–0
SDRAM pins	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$			A11	A10	A9	A8	A7–0

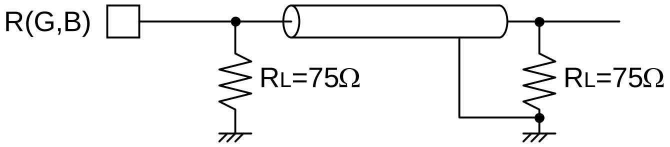
☞ $\overline{\text{VR64}}$ = “L” (when connected with 64M bits SDRAM)

YGV627 pins	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	BA1	BA0	VA11	VA10	VA9	VA8	VA7–0
SDRAM pins	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	A13	A12	A11	A10	A9	A8	A7–0

< Display monitor interface>

λ **R, G, B （O: Analog output）**

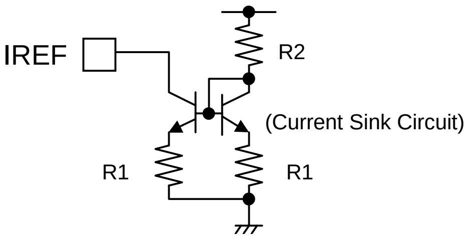
These pins output linear RGB signal. When a termination resistor of 37.5 Ω is connected, voltage amplitude with resolution of 8 bits (256 levels) is outputted. These pins can directly drive a monitor whose impedance is 75 Ω as shown below.



λ **IREF （I: Analog input）**

Reference current for RGB DAC is inputted to this pin. The reference current of – 9.38 mA provides amplitude of 0.7 Vp-p (typical value). When supplying the reference current, use a current sink circuit as shown below.

For the following circuit, adjust the values of R1 and R2 so that the pin potential of IREF (V_{IREF}) become approximately 1.37 V.



λ **$\overline{\text{CSYNC}}$ （O）**

This pin outputs a composite sync signal to external monitor. In interlace mode, it outputs equivalent pulse.

λ **$\overline{\text{VSYNC}}$ （O）**

This pin outputs vertical sync signal to external monitor.

λ **$\overline{\text{HSYNC}}$ （O）**

This pin outputs horizontal sync signal to external monitor.

λ **$\overline{\text{BLANK}}$ （O）**

This pin outputs a signal that indicates non-display period (blank period). Therefore, it can be used as a signal that indicates valid display period for LCD panel.

λ **FSC （O）**

This pin outputs sub-carrier clock for video encoder.

This pin can output a clock inputted to DTCKIN pin divided by 1, 2, 4 or 8 which may be selected in accordance with the register setting. Inputting a clock of 14.318 MHz into DTCKIN pin provides sub-carrier clock of 3.58 MHz when divided by 4.

λ **DOTCLK （O）**

Output signal of display data (analog R, G, B, DV17–DV0, YS, AT) is outputted synchronizing with DOTCLK.

λ **$\overline{\text{DVOUT}}$ （I: PULL UP）**

This pin selects input/output of external video data terminal.

The external video terminal becomes output when low level is inputted to this pin, or input when high level is inputted to this pin. The input/output of the external video data terminal can be changed with internal register EXIO(R#05). In such case, input high level to $\overline{\text{DVOUT}}$ or keep it open.

λ **DV17–0 （I/O: PULL UP）**

These are input/output pins for digital external video data.

These pins become input when high level is inputted to $\overline{\text{DVOUT}}$ and EXIO(R#05) ="0" is set, or becomes output when low level is inputted to $\overline{\text{DVOUT}}$ pin or EXIO(R#05) ="1" is set.

For the external video data, a format with 6 bits for digital RGB individually, or a format with 6 bits for CrYCb individually can be selected.

The format of the input / output data is as shown below.

DV17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R(Cr)5–0(I/O)						G(Y)5–0(I/O)						B(Cb)5–0(I/O)					

λ **YS （O）**

When performing superimposition, this pin outputs a signal that controls switching with external signal.

When displaying bitmap plane, this pin outputs inversion signal for YSN bits that can be set by dot.

In the border displaying period or blank period, this pin outputs inversion signal of border YS data.

λ **AT （O）**

This pin outputs 1 bit attribute data that can be set by display dot. When ATE(R#05) signal of internal register is set to "0", the value set in the ATD bit of register is outputted regardless the display data.

When "1" is set for ATE signal, B0 (LSB of Blue) that is inputted to DAC for blue is outputted from AT pin.

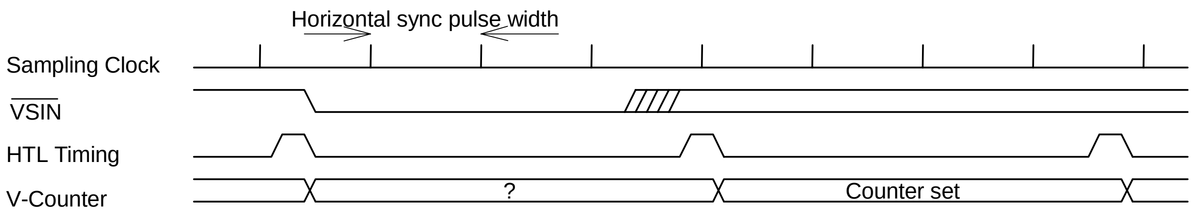
At this time, the same data of MSB is inputted to LSB of DAC for blue.

During the blank period, B0 of border is outputted when ATE signal is set to "1". When the signal is set to "1", the value set to ATD bit is outputted.

This signal can be used, for example, for specifying semi-transparency (YM) when externally mixing display data.

λ **$\overline{\text{VSIN}}$ （I: PULL UP）**

This signal resets the vertical timing of CRT controller block of YGV627. When this input signal is sampled with period equal to the pulse width of horizontal sync signal, and low level is detected three times consecutively, the internal V counter is set at the first HTL timing (horizontal sync signal start timing) immediately after the moment. In interlace mode, field identification is performed at the resetting of vertical timing by inputting composite sync signal of external video through this pin. This feature allows the superimposition synchronizing with frame period easily. If this signal is inputted during the display period, the display data of the next one field is not guaranteed. This pin can be kept open if this function is not used. The function of this pin is the same as that of $\overline{\text{VRESET}}$ pin of YGV617B.



- **$\overline{\text{HSIN}}$ （I: PULL UP）**

This signal resets the horizontal timing of CRT controller block of YGV627.

The horizontal timing is set to the horizontal sync starting position at the moment this signal falls from high level to low level, and at the same time, the phase of dot clock is reset.

When the built-in PLL is operated in the external sync mode, the input signal and output of $\overline{\text{HSYNC}}$ pin are locked.

If this signal is inputted during the display period, the display data of the next line is not guaranteed.

This pin can be kept open if this function is not used.

The function of this pin is the same as that of $\overline{\text{HRESET}}$ pin of YGV617B.

< Clocks>

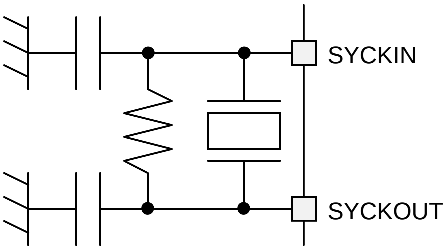
- **SYCKIN （I）, SYCKOUT （O）**

Crystal is connected to these pins to generate reference clock that is used in the system.

The built-in PLL produces SDRAM clock based on this clock. When supplying system clock and dot clock using the same clock through SYSEL pin (when low level is inputted to SYSEL), input the common clock through DTCKIN pin. At this time, input low level or high level signal into SYCKIN pin. SYCKOUT pin can be kept open.

When inputting externally generated clock, input it into SYCKIN pin.

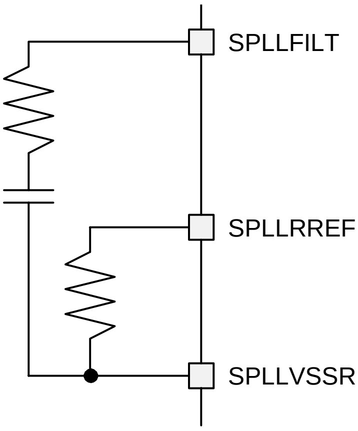
SYCKIN and SYCKOUT pins are the same as VCKIN and VCKOUT pins of YGV617B.



- **SPLLVSSR, SPLLRREF, SPLLFILT （Analog）**

These pins are used to connect external resistors and capacitors for the built-in PLL that produces SDRAM clock.

For the details of resistors and condensers value in the following figure, please refer to the Application Manual.



Notes:

1. Arrange the components so that the parasitic capacitance among SPLLFILT, SPLLRREF and SPLLVSSR is minimized and the signals do not cross each other.
2. PLL may not lock if there is a time difference between the rising moment of AVDD (for PLL) and the rising moment of VDD (for Digital Logic).

λ SYSEL （I: PULL UP）

This signal selects the source of reference clock to be used in the system.

When low level is inputted to SYSEL, the system clock and dot clock use the same source of the clock. In this case, the common clock is inputted into DTCKIN. Therefore, there is no need to input clock into SYCKIN. When high level is inputted to SYSEL, SYCKIN pin input is used as the reference system clock independent from the dot clock.

When SYSEL is used with low level input, be sure to input stable clock into DTCKIN even if the clock produced by the built-in PLL is used as the dot clock. Since SYSEL is used for selection of a mode, always fix it to either level. This pin has a pull-up resistor.

The function of this pin is the same as that of VCKS pin of YGV617B.

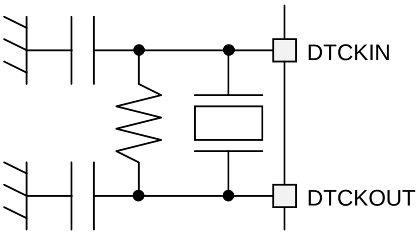
λ DTCKIN (I), DTCKOUT (O)

Crystal is connected to these pins to input dot clock.

When operating the built-in PLL in FSC sync mode, the reference clock is inputted to these pins. At this time, the clock with multiple of fsc is to be inputted. When PLL function is not used, this input clock is supplied directly to the CRTC block and displays data control block. When low level is inputted to SYSEL, it is also supplied as the reference system clock.

When inputted externally generated clock, input it into DTCKIN.

DTCKIN and DTCKOUT are the same as DCKIN and DCKOUT of YGV617B.

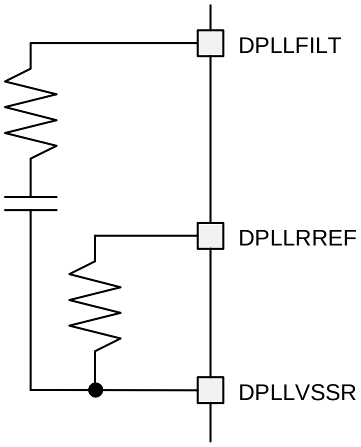


λ DPLLVSSR, DPLLRREF, DPLLFILT （Analog）

These pins are used to connect external resistors and capacitors for the built-in PLL that produces dot clock.

When directly using DTCKIN input signal as dot clock without using the built-in PLL, keep DPLLFILT open and short-circuit between DPLLRREF and DPLLVSSR.

For the details of resistors and condensers value in the following figure, please refer to the Application Manual.



Notes:

1. Arrange the components so that the parasitic capacitance among DPLLFILT, DPLLRREF and DPLLVSSR is minimized and the signals do not cross each other.
2. PLL may not lock if there is a time difference between the rising moment of AVDD (for PLL) and the rising moment of VDD (for Digital Logic).

<Other pins>

λ **$\overline{\text{TEST2-0}}$ （I: Pull Up）**

These pins are used for testing internal circuit of YGV627.

Be sure to keep them open (without connecting any component) when using the device.

λ **AVDD1, AVSS1 （I）**

These pins supply power to VCO analog circuit that generates SDRAM clock.

Connect +3.3 V to AVDD1 and ground level to AVSS1.

λ **AVDD2, AVSS2 （I）**

These pins supply power to VCO analog circuit that generates dot clock.

Connect +3.3 V to AVDD2 and ground level to AVSS2.

λ **AVDD3, AVSS3 （I）**

These pins supply power to analog circuit of RGB DAC section.

Connect +3.3 V to AVDD3 and ground level to AVSS3.

λ **VDD, VSS （I）**

These pins supply power to digital circuit of YGV627.

Connect +3.3 V to VDD and ground level to VSS. YGV627 has several VDD and VSS, all of which require power supply. Connect a bypass capacitor between VDD and VSS as a noise killer as close as possible to the pins.

Power supplies, VDD, AVDD1, AVDD2 and AVDD3 are to be turned on at the same time, in principle. Turning on the power supplies at the same time means that they are to be turned on before the potential difference between them reaches and exceeds 0.6 V. Avoid making the potential difference 0.6 V or over continuously (over approximately one second), or the reliability of this LSI may be deteriorated. If the potential difference among the power supplies cannot be avoided, be sure to turn on/off VDD, AVDD1, AVDD2 and AVDD3 so that their voltages do not exceed VDD.

ν ELECTRICAL CHARACTERISTICS

λ Absolute maximum ratings

Items	Symbol	Ratings	Unit
Supply Voltage (VDD, AVDD)	V_{DD}[*1]	–0.5 to +4.6	V
Input pin voltage (DTCKIN, SYCKIN, VD15–0)	V_I[*1]	–0.5 to V_{DD}+0.5	V
Input pin voltage (other than the above)	V_I[*1]	–0.5 to 5.5	V
Output pin voltage	V_O[*1]	–0.5 to V_{DD}+0.5	V
Output pin current	I_O	–20 to +20	mA
Storage temperature	T_{stg}	–50 to +125	°C

[*1]: Value with respect to VSS (GND) = 0V

λ Recommended operating conditions

Items	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage (VDD, AVDD)	V_{DD}[*1]	3.0	3.3	3.6	V
Supply Voltage	V_{SS}		0		V
Low level input voltage (VD15–0)	V_{IL}[*1]	–0.3		0.8	V
High level input voltage (VD15–0)	V_{IH}[*1]	2.2		V_{DD} +0.3	V
Low level input voltage (DTCKIN, SYCKIN)	V_{IL}[*1]	–0.3		0.3V_{DD}	V
High level input voltage (DTCKIN, SYCKIN)	V_{IH}[*1]	0.7V_{DD}		V_{DD} +0.3	V
Low level input voltage ($\overline{\text{RESET}}$ pin)	V_{IL}[*1]	–0.3		0.8	V
High level input voltage ($\overline{\text{RESET}}$ pin)	V_{IH}[*1]	2.4		5.3	V
Low level input voltage (other than the above)	V_{IL}[*1]	–0.3		0.8	V
High level input voltage (other than the above)	V_{IH}[*1]	2.2		5.3	V
Ambient operating temperature	T_{OP}	–40		+85	°C

[*1]: Value with respect to V_{SS} (GND) = 0V

λ Electrical characteristics under recommended operating conditions

● DC characteristics

Items	Symbol	Min.	Typ.	Max.	Unit
Low level output voltage	V_{OL}[*1]			0.4	V
High level output voltage [*2]	V_{OH}[*3]	2.4			V
Input leakage current	I_{LI}			10	μA
Output leakage current	I_{LO}			25	μA
Current consumption[*4 *5]	I_{DD}		180	220	mA

[*1]: Measurement condition I_{OL}=1.6mA

[*2]: Except Open Drain pin

[*3]: Measurement condition I_{OH}= –1.0mA

[*4]: Typical value means average value obtained when a general image is displayed.

[*5]: Maximum value means instantaneous maximum value obtained when the internal circuit is fully operated.

● Pin capacity

Items	Symbol	Min.	Typ.	Max.	Unit
Input pin capacity	C_I			8	pF
Output pin capacity	C_O			10	pF
Input / Output pin capacity	C_{IO}			12	pF

AC characteristics

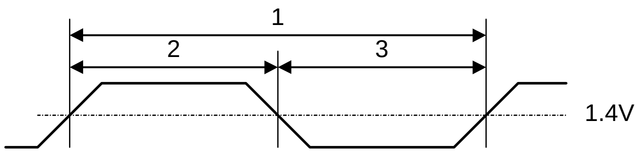
NOTE: When measuring timing, the input signal reference level is 1.4 V and transition time tT=1 ns. The transition time is measured at the time of V_{IH} and V_{IL}. When the transition time is over 1 ns, the input signal reference level is V_{IH} (minimum value) and V_{IL} (maximum value).

Clock input

No.	Items	Symbol	Min.	Typ.	Max.	Unit
1	DTCKIN : Input Clock Frequency	f_{DTCK}	1	14.32[*1]	40[*2]	MHz
	DTCKIN : Clock Cycle Time	t_{DCK}	25		1000	ns
2	DTCKIN : Clock High Level Pulse Width	twh_{DCK}	11.25			
3	DTCKIN : Clock Low Level Pulse Width	twl_{DCK}	11.25			
	DTCKIN : Clock Duty	D_{DCK}	45	50	55	%
1	SYCKIN : Input Clock Frequency	f_{SCK}	1	16.6	33.3	MHz
	SYCKIN : Clock Cycle Time	t_{SCK}	30		1000	ns
2	SYCKIN : Clock High Level Pulse Width	twh_{SCK}	13.5			
3	SYCKIN : Clock Low Level Pulse Width	twl_{SCK}	13.5			
	SYCKIN : Clock Duty	D_{SCK}	45	50	55	%

[*1]: This is the case of NTSC. Use of other scanning mode allows optional selection of 13.5 MHz, 27 MHz, 28.6 MHz, 33 MHz or other frequency.

[*2]: When oscillating clock directly with XTAL, the maximum frequency is 33.3 MHz. When inputting clock over 33.3 MHz, input clock signal oscillated externally with clock module or other means into DTCKIN pin.

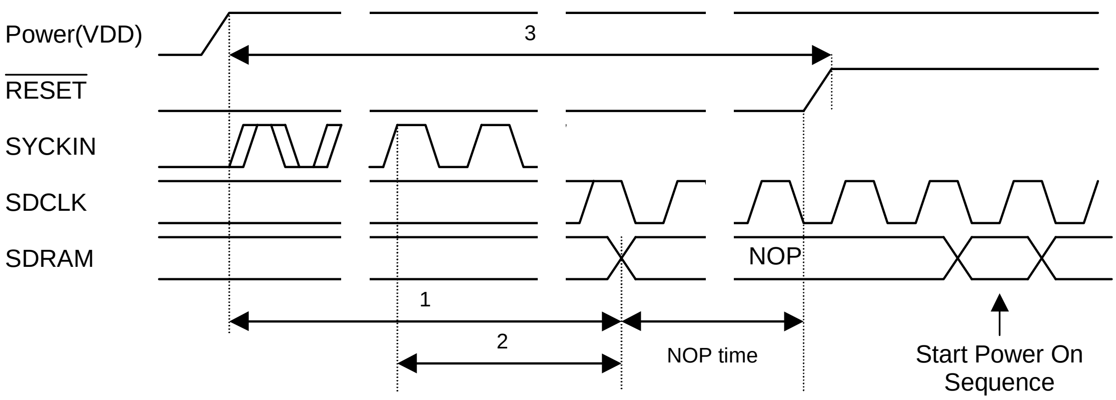


• Reset input

No.	Items	Symbol	Min.	Typ.	Max.	Unit
1	SDCLK stabilization time after VDD input[*1]		1			ms
2	SDCLK signal stabilization time after SYCKIN		1			ms
3	$\overline{\text{RESET}}$ Input Pulse Width	$\mathrm{tw}_{\mathrm{RS}}$	1.5			ms[*2]

Since YGV627 produces SDRAM clock with PLL, it requires approximately 1ms after stabilization of power supply level and SYCKIN pin input clock for stabilization of clock. Moreover, in power on sequence of SDRAM, NOP state[*3] of 100 μs to 500 μs or over is needed after stabilization of the power supply level and clock frequency. Keep these times with assert time of $\overline{\text{RESET}}$ pin (low level pulse width tWRS).

After negating $\overline{\text{RESET}}$ signal, power on sequence of SDRAM is started by issuing Precharge All command (PALL).



[*1]: This rule applies from the moment all power supplies, VDD pin, AVDD1 pin, AVDD2 pin, and AVDD3 pin are turned on.

[*2]: The value when stabilization time of SDRAM is 500 μs

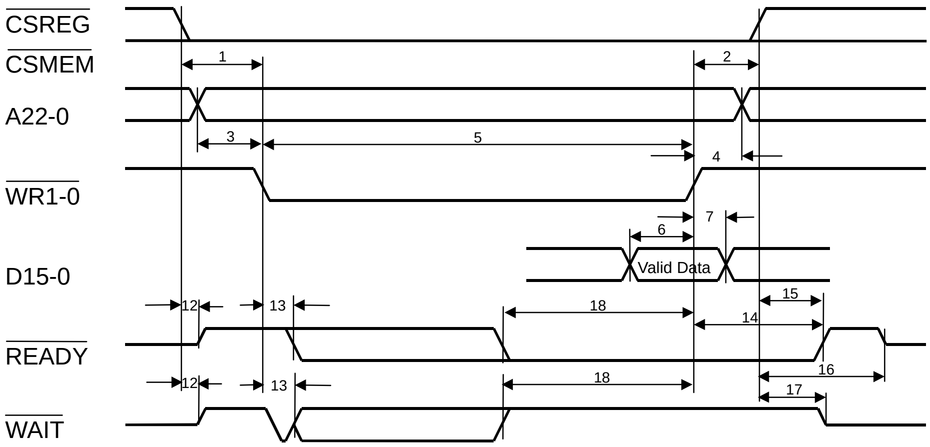
[*3]: For the time needed for NOP state, confirm the specification of SDRAM to be adopted.

- **System interface (Measurement condition: C_L=50 pF)**

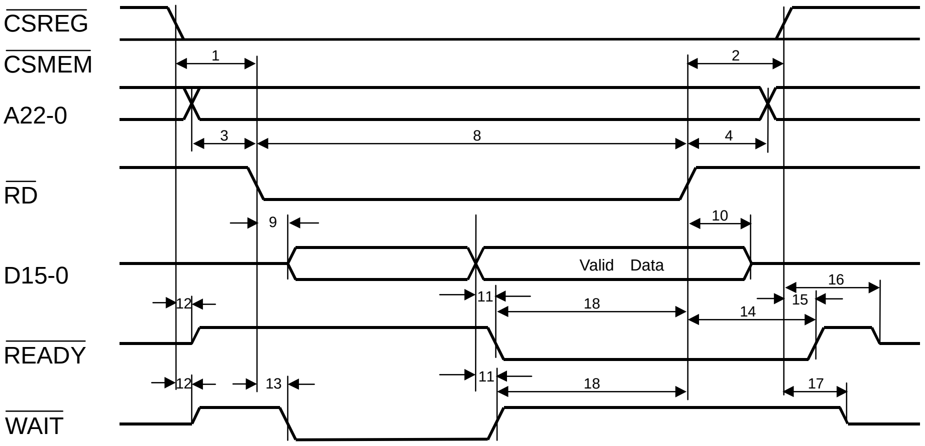
No.	Items	Symbol	Min.	Typ.	Max.	Unit	Note
1	$\overline{CSREG}$,$\overline{CSMEM}$ setup time	ts_{CS}	2			ns	
2	$\overline{CSREG}$,$\overline{CSMEM}$ hold time	th_{CS}	0				
3	A22–0 setup time	ts_{A}	5				
4	A22–0 hold time	th_{A}	0				
5	$\overline{WR1\text{-}0}$ pulse width (@no wait access)	tw_{IWR}	20				7
6	D15–0 setup time (@write access)	ts_{D}	10				
7	D15–0 hold time (@write access)	th_{D}	3				
8	$\overline{RD}$ pulse width (@no wait access)	tw_{IRD}	$2t_{SCK}+15$				1
9	D15–0 turn on time (@read access)	ton_{D}	0		15		
10	D15–0 turn off time (@read access)	$toff_{D}$	5		15		
11	D15–0 valid data output delay time (@read access)	td_{D}			0		
12	$\overline{READY}$,$\overline{WAIT}$ turn on time (Z to H)	ton_{RW}	0		5		
13	$\overline{READY}$,$\overline{WAIT}$ delay time from $\overline{WR1\text{-}0}$ active (H to L)	td_{RW}			45		6
14	$\overline{READY}$ hold time from $\overline{WR1\text{-}0}$,$\overline{RD}$ inactive (L to H)	th_{REWR}	3		18		
15	$\overline{READY}$ hold time from$\overline{CSREG}$,$\overline{CSMEM}$ inactive	th_{RECS}	3		18		
16	$\overline{READY}$ turn off time after$\overline{CSREG}$,$\overline{CSMEM}$ inactive	$toff_{RC}$	7		18		
17	$\overline{WAIT}$ turn off time after$\overline{CSREG}$,$\overline{CSMEM}$ inactive	$toff_{WC}$			5		
18	$\overline{WR1\text{-}0}$,$\overline{RD}$ hold time after $\overline{READY}$ active or $\overline{WAIT}$ inactive	th_{WR}			0		
19	$\overline{WR1\text{-}0}$,$\overline{RD}$ “high” level width after write access	twh_{WRW}	10				2
19	$\overline{WR1\text{-}0}$,$\overline{RD}$ “high” level width after write access	twh_{WRW}	$2.5t_{SCK}+15$				3
19	$\overline{WR1\text{-}0}$,$\overline{RD}$ “high” level width after write access	twh_{WRW}	$5.5t_{SCK}+15$				4
20	$\overline{WR1\text{-}0}$,$\overline{RD}$ “high” level width after read access	twh_{WRR}	10				
21	$\overline{DREQ}$ hold time	th_{DRQ}	0				
22	$\overline{DACK}$ pulse width	tw_{IDAK}	20				
23	$\overline{DACK}$ high level width (@ 8bits system bus (LWD= “0”))	twh_{DAK}	10				5
24	$\overline{DACK}$ cycle time (@ 8bits system bus (LWD= “0”))	tcy_{DAK}	$2t_{SCK}$				5
25	D15–0 setup time (@DMA access)	ts_{DMA}	10				
26	D15–0 hold time (@DMA access)	th_{DMA}	10				
27	$\overline{DACK}$ delay time after $\overline{CS}$ inactive	td_{DAK}	5				
28	$\overline{CSREG}$,$\overline{CSMEM}$delay time after $\overline{DACK}$ inactive	th_{CAK}	5				

Note 1 : Defined with time from the fall of $\overline{RD}$ to the time settled read data is outputted. Actually, it is necessary to keep setup time for the rise of $\overline{RD}$.
Note 2 : When hardware wait is permitted
Note 3 : After write access to other than R#00-0E when hardware wait is prohibited (No Wait mode)
Note 4 : After write access to R#00-0E when hardware wait is prohibited (No Wait mode)
Note 5 : Valid only when system bus is 8 bits (low level is inputted to LWD pin)
Note 6 : Value at the time when sufficient time elapses from write access immediately before
Note 7 : Conditions of both $tw_{IWR} \geq 20$ns and $tw_{IWR} \geq td_{RW}$ must be met when $\overline{WAIT}$ and $\overline{READY}$ are used.

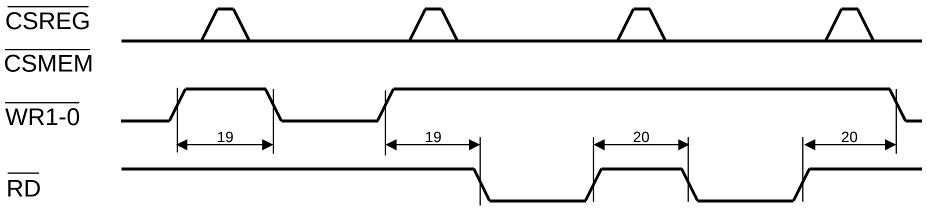
- Write cycle ($\overline{\text{WR1-0}}$ control)


CSREG
CSMEM
A22-0
WR1-0
D15-0
READY
WAIT
1
2
3
5
4
7
6
Valid Data
12
13
18
15
14
12
13
18
16
17

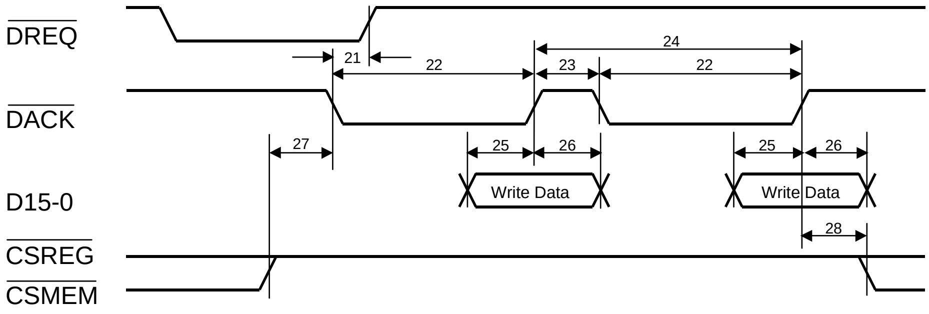
- Read cycle ($\overline{\text{RD}}$ control)


CSREG
CSMEM
A22-0
RD
D15-0
READY
WAIT
1
2
3
8
4
9
10
Valid Data
16
12
11
18
15
14
12
13
11
18
17

- $\overline{\text{WR1-0}}$, $\overline{\text{RD}}$ input prohibited period


CSREG
CSMEM
WR1-0
RD
19
19
20
20

- DMA access


DREQ
DACK
D15-0
CSREG
CSMEM
24
21
22
23
22
27
25
26
25
26
Write Data
Write Data
28

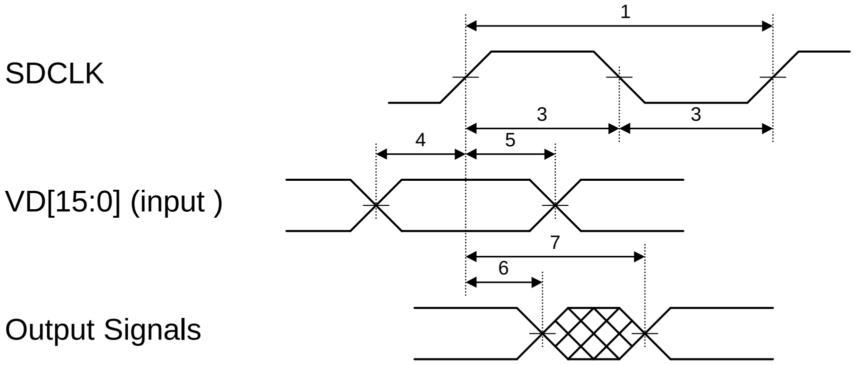
- **SDRAM interface (Measurement condition C_L=30 pF)**

No.	Items	Symbol	Min.	Typ.	Max.	Unit	Note
1	SDCLK:cycle time	tcSDCLK	15			ns	1,2
2	SDCLK:clock jitter	-			±1		1
3	SDCLK:clock width	twSDCLK	5				1
4	VD[15:0]:input data setup time	tsVD	2				1
5	VD[15:0]:input data hold time	thVD	2				1
6	Output signal:hold time	thSDO	2				3
7	Output signal:delay time	tdSDO			12		3

Note 1: PLL must be in stabilized state.

Note 2: SDCLK is oscillated with built-in VCO. Oscillated frequency range of VCO ranges from 110 MHz to 134 MHz. Therefore, the frequency range of SDCLK must be set for 55 MHz through 66.6 MHz.

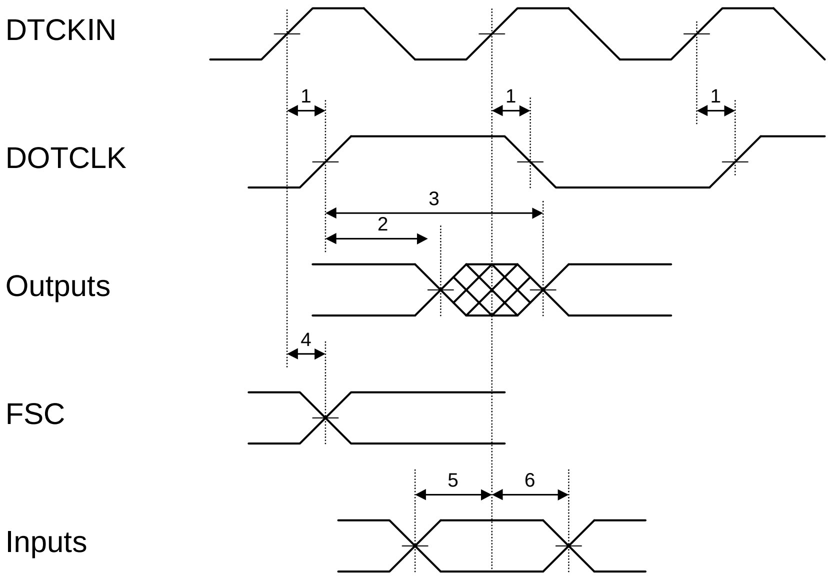
Note 3: Output signals are those outputted from the following pins. BA1–0, VA11–0, VD15–0, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQMH, or DQML



• Monitor interface (Measurement condition C_L=30 pF)

No.	Items	Symbol	Min.	Typ.	Max.	Unit	Note
1	DOTCLK:delay time	tdDOTCLK			15	ns	1
2	$\overline{\mathrm{CSYNC}}$, $\overline{\mathrm{VSYNC}}$, $\overline{\mathrm{HSYNC}}$, DV17–0 (out) :output hold time	thDISP	0				
3	$\overline{\mathrm{CSYNC}}$, $\overline{\mathrm{VSYNC}}$, $\overline{\mathrm{HSYNC}}$, DV17–0 (out) :output delay time	tdDISP			15		
4	FSC:delay time	tdFSC			15		
5	$\overline{\mathrm{HSIN}}$, $\overline{\mathrm{VSIN}}$, DV17–0 (in) :input setup time	tsSIN	10				
6	$\overline{\mathrm{HSIN}}$, $\overline{\mathrm{VSIN}}$, DV17–0 (in) :input hold time	thSIN	5				

Note 1: When PLL is not used (R#22:DCKS= “0”)

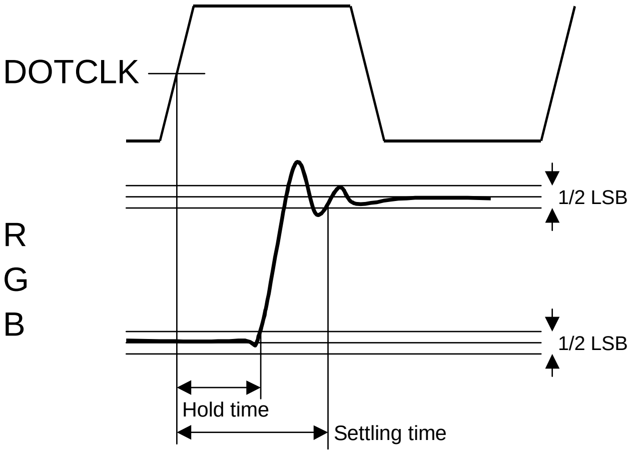


- **Characteristics of RGB output pins**

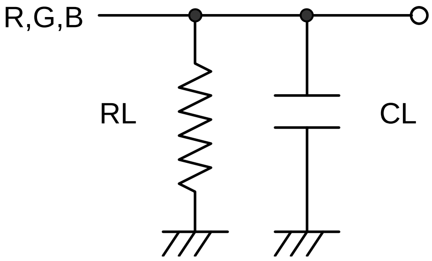
Items	Symbol	Min.	Typ.	Max.	Unit
Resolution	R_L=37.5Ω C_L=30pF IREF=–9.38mA			8	bit
Settling time				24	ns
Output hold time		5			ns
Amplitude of output voltage			0.7		V
Deviation of Vp-p of R, G and B				3	%

Settling time is defined as the period from the rise of DOTCLK to the time when output level of DAC enters in the range of ±1/2 LSB of the DOTCLK level after changing.

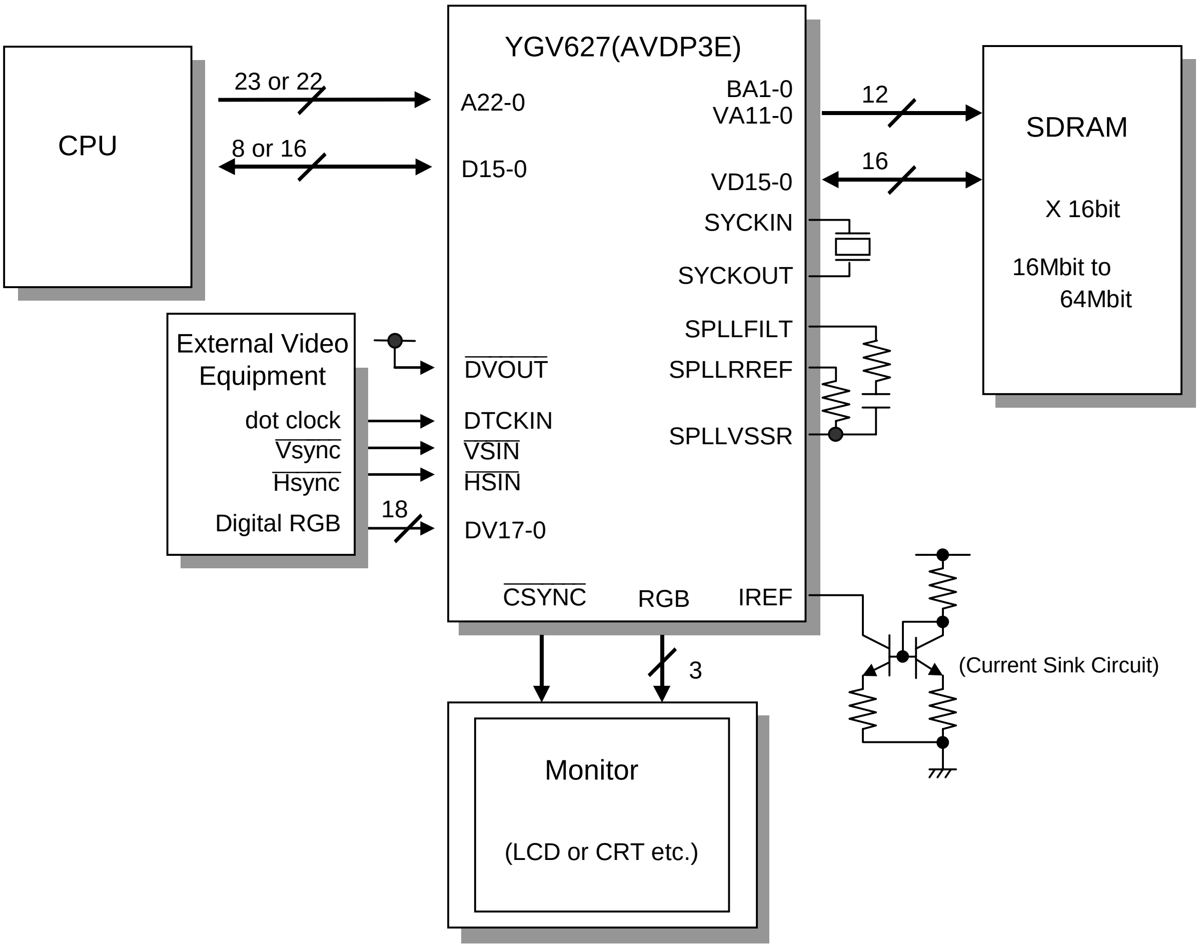
Output hold time is defined as the period from the rise of DOTCLK to the time when output level of DAC goes out of the range of ±1/2 LSB of the DOTCLK level after changing.



Measurement circuit

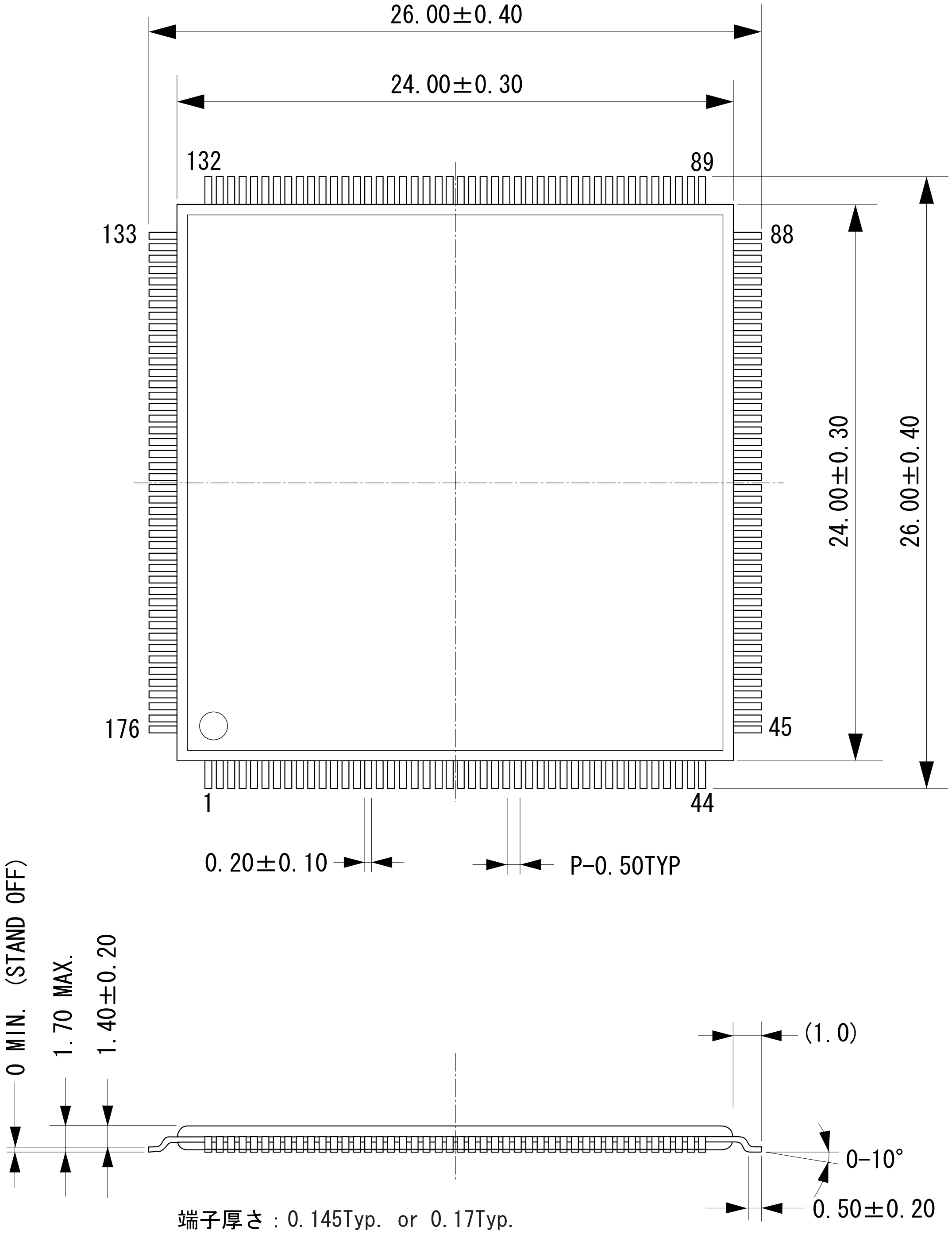


ν Example of System Configuration


YGV627(AVDP3E)
CPU
23 or 22
8 or 16
A22-0
D15-0
BA1-0
VA11-0
12
16
VD15-0
SDRAM
X 16bit
16Mbit to
64Mbit
SYCKIN
SYCKOUT
SPLLFILT
SPLLRREF
SPLLVSSR
External Video
Equipment
dot clock
Vsync
Hsync
Digital RGB
18
DVOUT
DTCKIN
VSIN
HSIN
DV17-0
CSYNC
RGB
IREF
3
(Current Sink Circuit)
Monitor
(LCD or CRT etc.)

ν External Dimensions of Package

C-PK176VP-2


26.00±0.40
24.00±0.30
132
89
133
88
176
45
1
44
24.00±0.30
26.00±0.40
0.20±0.10
P-0.50TYP
0 MIN. (STAND OFF)
1.70 MAX.
1.40±0.20
(1.0)
0-10°
0.50±0.20

端子厚さ：0.145Typ. or 0.17Typ.
LEAD THICKNESS

モールドコーナー形状は、この図面と若干異なるタイプのものもあります。
カッコ内の寸法値は参考値とする。
モールド外形寸法はバリを含まない。
単位(UNIT)：mm(millimeters)

The shape of the molded corner may slightly different from the shape in this diagram.
The figure in the parenthesis ( ) should be used as a reference.
Plastic body dimensions do not include burr of resin.
UNIT: mm

注）　表面実装LSIは保管条件及び、半田付けについての特別な配慮が必要です。
詳しくはヤマハ代理店までお問い合わせ下さい。

Note: The LSIs for surface mount need special consideration on storage and soldering conditions.
For detailed information, Please contact your nearest Yamaha agent.

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Notice The specifications of this product are subject to improvement changes without prior notice.

AGENT

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