ANALOG DEVICES

FEATURES
Four Complete Voltage Output DACs
Data Register Readback Feature
"Reset to Zero" Override
Multiplying Operation
Double-Buffered Latches
Surface Mount and DIP Packages
MIL-STD-883 Compliant Versions Available

APPLICATIONS
Automatic Test Equipment
Robotics
Process Control
Disk Drives
Instrumentation
Avionics

PRODUCT DESCRIPTION
The AD664 is four complete 12-bit, voltage-output DACs on one monolithic IC chip. Each DAC has a double-buffered input latch structure and a data readback function. All DAC read and write operations occur through a single microprocessor-compatible I/O port.

The I/O port accommodates 4-, 8- or 12-bit parallel words allowing simple interfacing with a wide variety of microprocessors. A reset to zero control pin is provided to allow a user to simultaneously reset all DAC outputs to zero, regardless of the contents of the input latch. Any one or all of the DACs may be placed in a transparent mode allowing immediate response by the outputs to the input data.

The analog portion of the AD664 consists of four DAC cells, four output amplifiers, a control amplifier and switches. Each DAC cell is an inverting R-2R type. The output current from each DAC is switched to the on-board application resistors and output amplifier. The output range of each DAC cell is programmed through the digital I/O port and may be set to unipolar or bipolar range, with a gain of one or two times the reference voltage. All DACs are operated from a single external reference.

The functional completeness of the AD664 results from the combination of Analog Devices' BiMOS II process, laser-trimmed thin-film resistors and double-level metal interconnects.

PRODUCT HIGHLIGHTS
1. The AD664 provides four voltage-output DACs on one chip offering the highest density 12-bit D/A function available.
2. The output range of each DAC is fully and independently programmable.
3. Readback capability allows verification of contents of the internal data registers.
4. The asynchronous RESET control returns all D/A outputs to zero volts.
5. DAC-to-DAC matching performance is specified and tested.
6. Linearity error is specified to be 1/2 LSB at room temperature and 3/4 LSB maximum for the K, B and T grades.
7. DAC performance is guaranteed to be monotonic over the full operating temperature range.
8. Readback buffers have three-state outputs.
9. Multiplying-mode operation allows use with fixed or variable, positive or negative external references.
10. The AD664 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD664/883B data sheet for detailed specifications.

ORDERING GUIDE

Model[1]	Temperature Range	Output Range	Gain Error	Linearity Error	Package Options[2]
AD664JN-UNI	0°C to +70°C	0 to +V_{REF}	±7 LSB	±0.75 LSB	N-28
AD664JN-BIP	0°C to +70°C	V_{REF} to +V_{REF}	±7 LSB	±0.75 LSB	N-28
AD664JP	0°C to +70°C	Programmable	±7 LSB	±0.75 LSB	P-44A
AD664KN-UNI	0°C to +70°C	0 to +V_{REF}	±5 LSB	±0.5 LSB	N-28
AD664KN-BIP	0°C to +70°C	V_{REF} to +V_{REF}	±5 LSB	±0.5 LSB	N-28
AD664KP	0°C to +70°C	Programmable	±5 LSB	±0.5 LSB	P-44A
AD664AD-UNI	-40°C to +85°C	0 to +V_{REF}	±7 LSB	±0.75 LSB	D-28
AD664AD-BIP	-40°C to +85°C	V_{REF} to +V_{REF}	±7 LSB	±0.75 LSB	D-28
AD664AJ	-40°C to +85°C	Programmable	±7 LSB	±0.75 LSB	J-44
AD664BD-UNI	-40°C to +85°C	0 to +V_{REF}	±5 LSB	±0.5 LSB	D-28
AD664BD-BIP	-40°C to +85°C	V_{REF} to +V_{REF}	±5 LSB	±0.5 LSB	D-28
AD664BJ	-40°C to +85°C	Programmable	±5 LSB	±0.5 LSB	J-44
AD664BE	-40°C to +85°C	Programmable	±5 LSB	±0.5 LSB	E-44A
AD664SD-UNI	-55°C to +125°C	0 to +V_{REF}	±7 LSB	±0.75 LSB	D-28
AD664SD-BIP	-55°C to +125°C	V_{REF} to +V_{REF}	±7 LSB	±0.75 LSB	D-28
AD664TD-UNI	-55°C to +125°C	0 to +V_{REF}	±5 LSB	±0.5 LSB	D-28
AD664TD-BIP	-55°C to +125°C	V_{REF} to +V_{REF}	±5 LSB	±0.5 LSB	D-28

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD664/883B data sheet.
[2]D = Ceramic DIP; E = Leadless Ceramic Chip Carrier; J = Leaded Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD664—SPECIFICATIONS

(V_{LL} = +5 V, V_{CC} = +15 V, V_{EE} = -15 V, V_{REF} = +10 V, T_A = +25°C unless otherwise noted)

Model	JN/JP/AD/AJ/SD			KN/KP/BD/BJ/BE/TD/TE			Units
	Min	Typ	Max	Min	Typ	Max	
RESOLUTION		12	12		*	*	Bits
ANALOG OUTPUT							
Voltage Range[1]							
UNI Versions	0		V_{CC} 2.0[2]	*		*	Volts
BIP Versions	V_{EE} + 2.0[2]		V_{CC} 2.0[2]	*		*	Volts
Output Current	5			*			mA
Load Resistance		2			*		kΩ
Load Capacitance			500			*	pF
Short-Circuit Current		25	40		*	*	mA
ACCURACY							
Gain Error	-7	±3	7	-5	±2	5	LSB
Unipolar Offset	-2	+1/2	2	-1	±1/4	1	LSB
Bipolar Zero[3]	-3	±3/4	3	-2	±1/2	2	LSB
Linearity Error[3]	-3/4	±1/2	3/4	-1/2	±1/4	1/2	LSB
Linearity T_{MIN} to T_{MAX}	-1	±3/4	1	-3/4	±1/2	3/4	LSB
Differential Linearity	-3/4		3/4	-1/2		1/2	LSB
Differential Linearity T_{MIN} to T_{MAX}	Monotonic @ All Temperatures			Monotonic @ All Temperatures			
Gain Error Drift							
Unipolar 0 V to +10 V Mode	-12	±7	12	-10	±5	10	ppm of FSR[4,5]/°C
Bipolar 5 V to +5 V Mode	-12	±7	12	10	±5	10	ppm of FSR/°C
Bipolar 10 V to +10 V Mode	-12	±7	12	-10	±5	10	ppm of FSR/°C
Unipolar Offset Drift							
Unipolar 0 V to +10 V Mode	-3	+1.5	3	-2	±1	2	ppm of FSR/°C
Bipolar Zero Drift							
Bipolar 5 V to +5 V Mode	12	±7	12	-10	±5	10	ppm of FSR/°C
Bipolar -10 V to +10 V Mode	-12	±7	12	-10	±5	10	ppm of FSR/°C
REFERENCE INPUT							
Input Resistance	1.3		2.6	*		*	kΩ
Voltage Range[6]	V_{EE} + 2.0[2]		V_{CC} 2.0[2]	*		*	Volts
POWER REQUIREMENTS							
V_{LL}	4.5	5.0	5.5	*	*	*	Volts
I_{LL}							
@ V_{IH}, V_{IL} = 5 V, 0 V		0.1	1		*	*	mA
@ V_{IH}, V_{IL} = 2.4 V, 0.4 V		3	6		*	*	mA
V_{CC}/V_{EE}	±11.4		±16.5	*		*	Volts
I_{CC}		12	15		*	*	mA
I_{EE}		15	19		*	*	mA
Total Power		400	525		*	*	mW
ANALOG GROUND CURRENT[7]	600	±400	+600	*	*	*	μA
MATCHING PERFORMANCE							
Gain[8]	-6	±3	6	-4	±2	4	LSB
Offset[9]	-2	+1/2	2	-1	±1/4	1	LSB
Bipolar Zero[10]	-3	±1	3	-2	±1	2	LSB
Linearity[11]	-1.5	±1/2	1.5	-1	±1/2	1	LSB
CROSSTALK							
Analog			-90			*	dB
Digital			60			*	dB
DYNAMIC PERFORMANCE (R_l = 2 kΩ, C_L = 500 pF)							
Settling Time to ±1/2 LSB							
Off←Bits→On, GAIN = 1, V_{REF} = 10		8	10		*		μs
Settling Time to ±1/2 LSB							
10←V_{REF} →10 V, GAIN = 1, Bits On		10			*		μs
Glitch Impulse			500			*	nV-sec
MULTIPLYING MODE PERFORMANCE							
Reference Feedthrough @ 1 kHz		75			*		dB
Reference -3 dB Bandwidth		70			*		kHz
POWER SUPPLY GAIN SENSITIVITY							
11.4 V←V_{CC}→16.5 V		±2	±5		*	*	ppm/%
16.5 V←V_{EE}→ 11.4 V		±2	±5		*	*	ppm/%
4.5 V←V_{LL}→5.5 V		±2	±5		*	*	ppm/%

Specifications subject to change without notice.