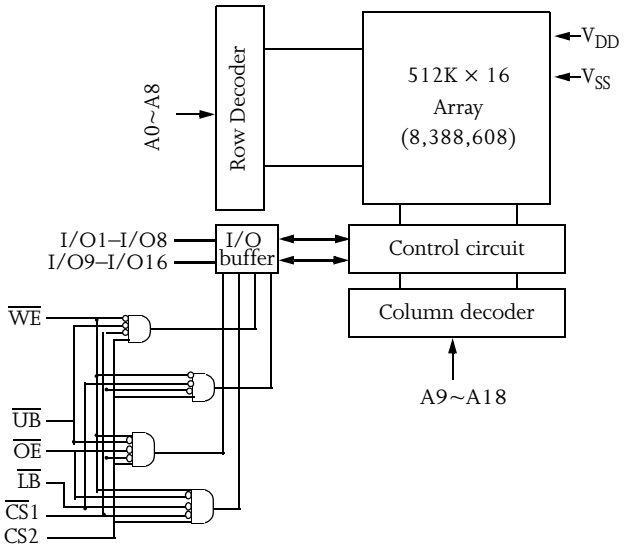
1.65V to 2.2V 512K × 16 Intelliwatt™ Super Low-Power CMOS SRAM

Features

- AS6YB51216
- Intelliwatt™ active power circuitry
- Industrial temperature range (-40° - +85° C)
- Organization: 524,288 words x 16 bits
- 1.65V to 2.2V power supply range
- Fast access time of 70 ns
- Low power consumption: ACTIVE
  - 33 mW max at 2.2 V and 70 ns
- Low power consumption: STANDBY
  - 33 µW max at 2.2V
- 1.0V data retention
- Equal access and cycle times
- Easy memory expansion with $\overline{CS}1$, CS2, $\overline{OE}$ inputs
- Smallest footprint package
  - 48-ball FBGA; 7.0 x 9.0 mm
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA

Logic block diagram



Pin arrangement (top view)

48-CSP Ball-Grid-Array Package

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A0	A1	A2	CS2
B	I/O9	$\overline{UB}$	A3	A4	$\overline{CS}1$	I/O1
C	I/O10	I/O11	A5	A6	I/O2	I/O3
D	V_{SS}	I/O12	A17	A7	I/O4	V_{CC}
E	V_{CC}	I/O13	V_{SS}	A16	I/O5	V_{SS}
F	I/O15	I/O14	A14	A15	I/O6	I/O7
G	I/O16	DNU	A12	A13	$\overline{WE}$	I/O8
H	A18	A8	A9	A10	A11	DNU

Note: DNU = Do Not Use

Selection guide

Product	V_{CC} Range			Speed (ns)	Power Dissipation	
	Min (V)	Typ (V)	Max (V)		Operating (I_{CC1}) Max (mA)	Standby (I_{SB1}) Max (µA)
AS6YB51216	1.65	1.8	2.2	70/85	2	15

Functional description

The AS6YB51216 is a low-power CMOS 8,388,608-bit Static Random Access Memory (SRAM) device organized as 524,288 words x 16 bits. It is designed for memory applications where slow data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA}, t_{RC}, t_{WC}) of 70/85 ns are ideal for low-power applications. Active high and low chip enables ($\overline{CS}1$ and CS2) permit easy memory expansion with multiple-bank memory systems.

When $\overline{CS}1$ is high or CS2 is low, or $\overline{UB}$ and $\overline{LB}$ are high, the device enters standby mode. The AS6YB51216 is guaranteed not to exceed 33µW at 2.2V. The device also retains data when V_{CC} is reduced to 1.0V for even lower power consumption.

The device can also be put into standby mode when deselected ($\overline{CS}1$ is high or CS2 is low). The input/output pins (I/O0 through I/O15) are placed in a high-impedance state when deselected ($\overline{CS}1$ is high or CS2 is low), outputs are disabled ($\overline{OE}$ High), $\overline{UB}$ and $\overline{LB}$ are disabled ($\overline{UB}$, $\overline{LB}$ High), or during a write operation ($\overline{CS}1$ is low or CS2 is high and $\overline{WE}$ Low).

Writing to the device is accomplished by taking Chip Enables $\overline{CS}1$ Low, CS2 High and Write Enable ($\overline{WE}$) input Low. If Byte Low Enable ($\overline{LB}$) is Low, then data from I/O pins (I/O0 through I/O7), is written into the location specified on the address pins (A0 through A18). If Byte High Enable ($\overline{UB}$) is Low, then data from I/O pins (I/O8 through I/O15) is written into the location specified on the address pins (A0 through A18). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

Reading from the device is accomplished by taking Chip Enable $\overline{CS}1$ Low, CS2 High and Output Enable ($\overline{OE}$) Low while forcing the Write Enable ($\overline{WE}$) High. If Byte Low Enable ($\overline{LB}$) is Low, then data from the memory location specified by the address pins will appear on I/O0 to I/O7. If Byte High Enable ($\overline{UB}$) is Low, then data from memory will appear on I/O8 to I/O15.

These devices provide multiple center power and ground pins, and separate byte enable controls, allowing individual bytes to be written and read. LB controls the lower bits, I/O1–I/O8, and UB controls the higher bits, I/O9–I/O16.

All chip inputs and outputs are CMOS-compatible, and operation is from a single 1.65V to 2.2V supply. Device is available in the JEDEC 48-ball FBGA packages.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Voltage on V_{CC} relative to V_{SS}	V_{tIN}	–0.5	V_{CC} + 0.5	V
Voltage on any I/O pin relative to GND	$V_{tI/O}$	–0.5		V
Power dissipation	P_D	–	1.0	W
Storage temperature (plastic)	T_{stg}	–65	+150	°C
Temperature with V_{CC} applied	T_{bias}	–55	+125	°C
DC output current (low)	I_{OUT}	–	20	mA

Note: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Supply Current	I/O1–I/O8	I/O9–I/O16	Mode
H	X	X	X	X	X	I_{SB}	High Z	High Z	Standby (I_{SB})
X	L	X	X	X	X				
X	X	X	X	H	H				
L	H	H	H	L	X	I_{CC}	High Z	High Z	Output disable (I_{CC})
L	H	H	H	X	L				
L	H	H	L	L	H	I_{CC}	D_{OUT}	High Z	Read (I_{CC})
				H	L		High Z	D_{OUT}	
				L	L		D_{OUT}	D_{OUT}	
L	H	L	X	L	H	I_{CC}	D_{IN}	High Z	Write (I_{CC})
				H	L		High Z	D_{IN}	
				L	L		D_{IN}	D_{IN}	

Key: X = Don't care, L = Low, H = High.Recommended operating condition (over the operating range)

DC Recommended operating condition (over the operating range)

Parameter	Description	Test Conditions		Min	Max	Unit
Vcc	Supply voltage	-	-	1.65	2.2	V
V_{OH}	Output HIGH Voltage	I_{OH} = –0.1mA	V_{CC} = 1.65V	1.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1mA	V_{CC} = 1.65V		0.2	V
V_{IH}	Input HIGH Voltage		V_{CC} = 2.2V	1.4	V_{CC} + 0.2	V
V_{IL}	Input LOW Voltage		V_{CC} = 1.65V	–0.2	0.4	V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}		–1	+1	µA
I_{OZ}	Output Load Current	GND ≤ V_O ≤ $V_{CC;}$ Outputs High Z		–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	I_{OUT} = 0mA, f = 0	V_{CC} = 2.2V		1	mA
I_{CC1} @ 1 MHz	Average V_{CC} Operating Supply Current at 1 MHz	I_{OUT} = 0mA, f =1MHz	V_{CC} = 2.2V		2	mA
I_{CC2}	Average V_{CC} Operating Supply Current	I_{OUT} = 0mA, f = f_{Max}	V_{CC} = 2.2V		15 mA at 70ns 10 mA at 85ns	mA
I_{SB}	$\overline{CS}$ Power Down Current; TTL Inputs	$\overline{CS1}$ ≥ V_{CC} – 0.2V or CS2≤ 0.2V or $\overline{UB}$ = $\overline{LB}$ ≥ V_{IH}, other inputs = V_{IL} or V_{IH}, f = 0	V_{CC} = 2.2V		100	µA
I_{SB1}	$\overline{CS}$ Power Down Current; CMOS Inputs	$\overline{CS1}$ ≥ V_{CC} – 0.2V or CS2≤ 0.2V $\overline{UB}$ = $\overline{LB}$ ≥ V_{CC} – 0.2V other inputs = 0V – V_{CC}, f = f_{Max}	V_{CC} = 2.2V		15	µA

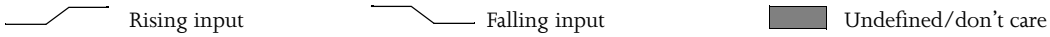
Capacitance (f = 1 MHz, T_a = Room temperature, V_{CC} = NOMINAL)[2]

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	A, $\overline{CS}1$, CS2, $\overline{WE}$, $\overline{OE}$, $\overline{LB}$, $\overline{UB}$	V_{IN} = 0V	5	pF
I/O capacitance	$C_{I/O}$	I/O	V_{IN} = V_{OUT} = 0V	7	pF

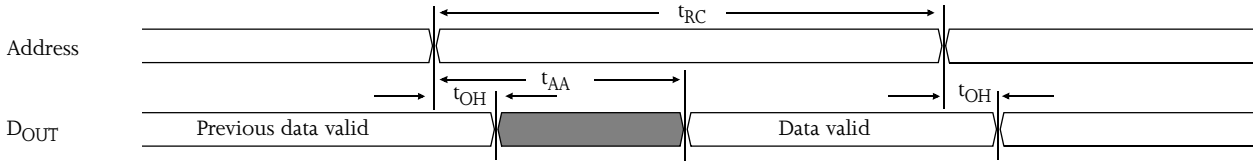
Read cycle (over the operating range)[3,9]

Parameter	Symbol	–70/85		Unit	Notes
		Min	Max		
Read cycle time	t_{RC}	70/85	–	ns	
Address access time	t_{AA}	–	70/85	ns	3
Chip select to output access time	t_{ACS}	–	70/85	ns	3
Output enable ($\overline{OE}$) access time	t_{OE}	–	35/40	ns	
Output hold from address change	t_{OH}	10	–	ns	5
Chip select to low Z output	t_{CLZ}	10	–	ns	4, 5
Chip disable to high Z output	t_{CHZ}	–	20	ns	4, 5
$\overline{OE}$ low to low Z output	t_{OLZ}	5	–	ns	4, 5
$\overline{UB}$/$\overline{LB}$ access time	t_{BA}	–	70/85	ns	
$\overline{UB}$/$\overline{LB}$ low to low Z	t_{BLZ}	10	–	ns	4, 5
$\overline{UB}$/$\overline{LB}$ high to high Z	t_{BHZ}	–	20	ns	4, 5
$\overline{OE}$ high to output in high Z	t_{OHZ}	–	20	ns	4, 5
Power up time	t_{PU}	0	–	ns	4, 5
Power down time	t_{PD}	–	55	ns	4, 5

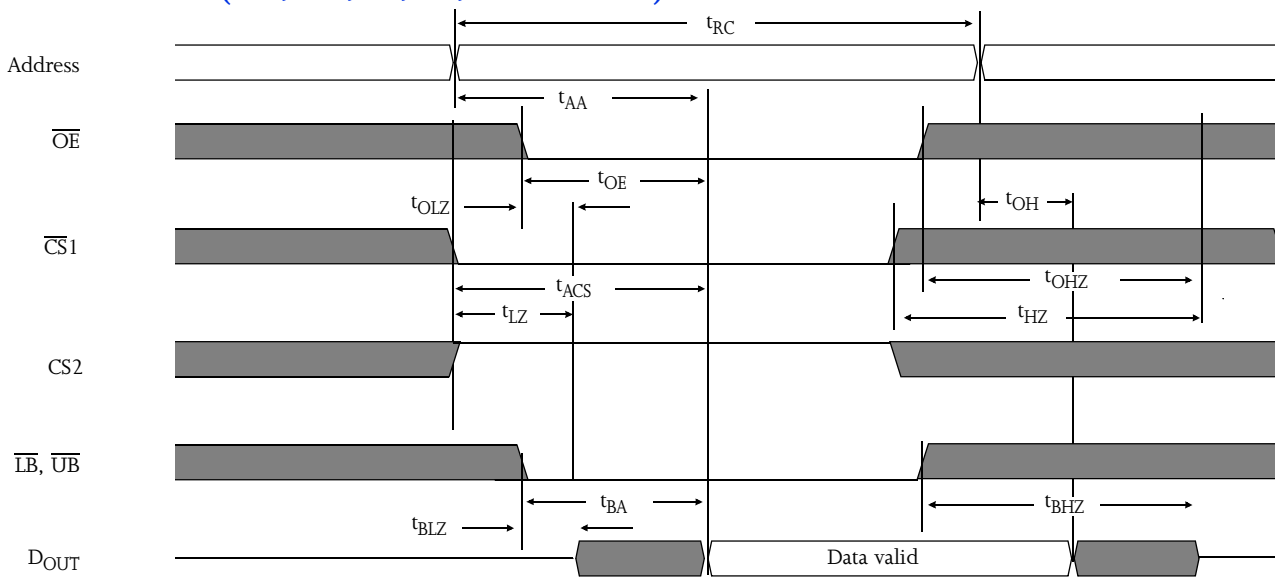
Key to switching waveforms



Read waveform 1 (address controlled)[3,6,7,9]



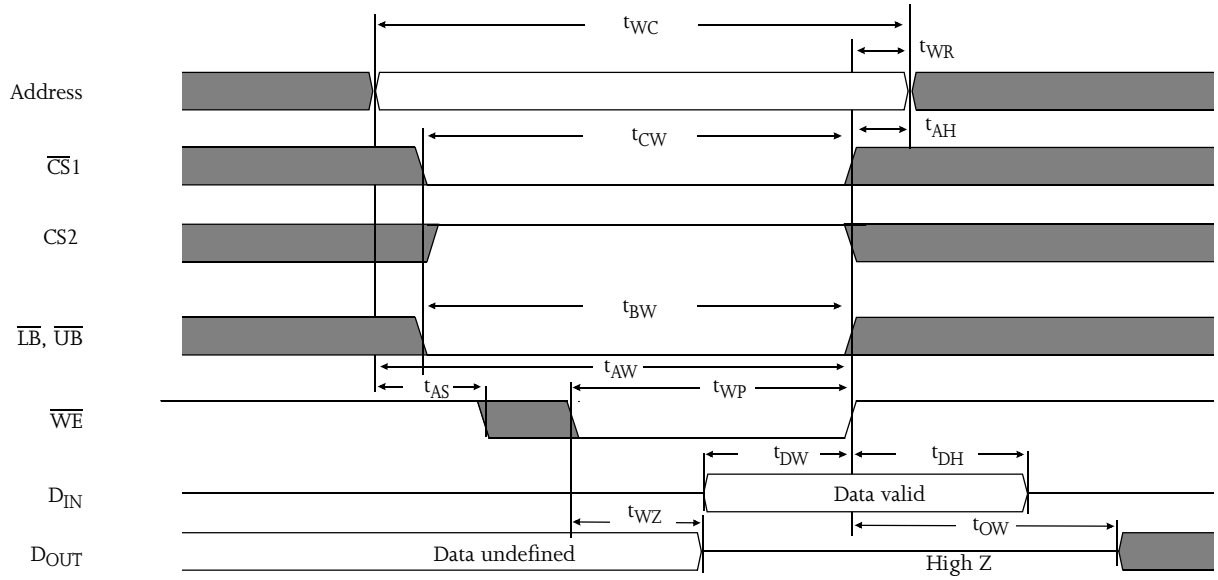
Read waveform 2 ($\overline{CS}1$, CS2, $\overline{OE}$, $\overline{UB}$, $\overline{LB}$ controlled)[3,6,8,9]



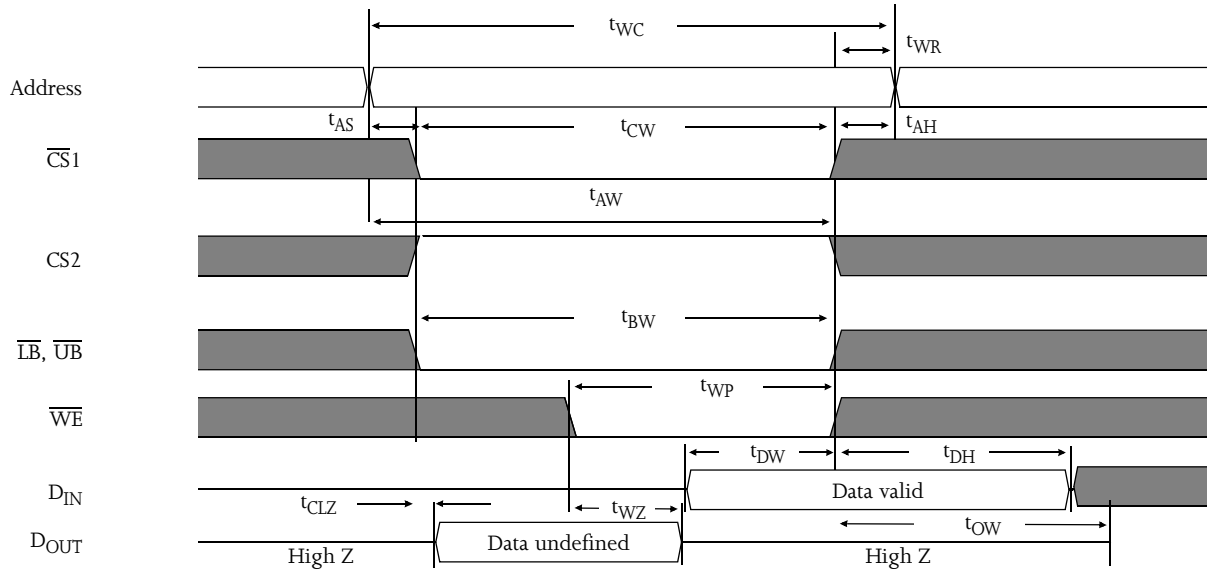
Write cycle (over the operating range)[11]

Parameter	Symbol	–70/85		Unit	Notes
		Min	Max		
Write cycle time	t_{WC}	70/85	–	ns	
Chip enable to write end	t_{CW}	60/70	–	ns	12
Address setup to write end	t_{AW}	60/70	–	ns	
Address setup time	t_{AS}	0	–	ns	12
Write pulse width	t_{WP}	50/60	–	ns	
Write recovery time	t_{WR}	0	–	ns	
Address hold from end of write	t_{AH}	0	–	ns	
Data valid to write end	t_{DW}	30/35	–	ns	
Data hold time	t_{DH}	0	–	ns	4, 5
Write enable to output in high Z	t_{WZ}	–	20	ns	4, 5
Output active from write end	t_{OW}	5	–	ns	4, 5
$\overline{UB}$/$\overline{LB}$ low to end of write	t_{BW}	60/70	–	ns	

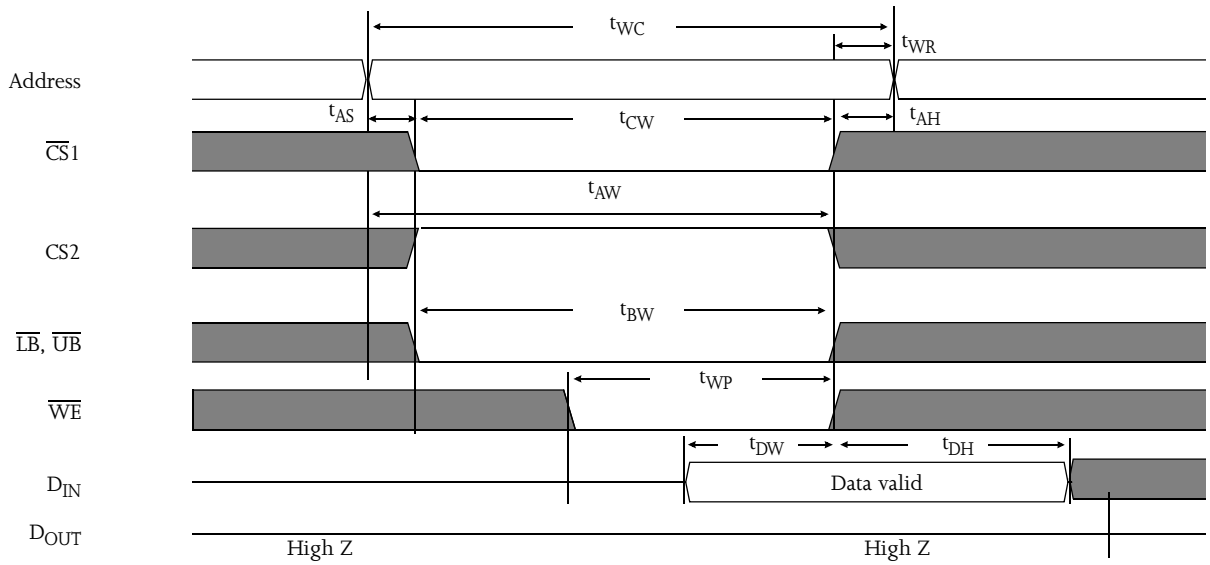
Write waveform 1 ($\overline{WE}$ controlled)[10,11]



Write waveform 2 ($\overline{CS}1$ controlled)[10,11]



Write waveform 3 ($\overline{LB}$, $\overline{UB}$ controlled)



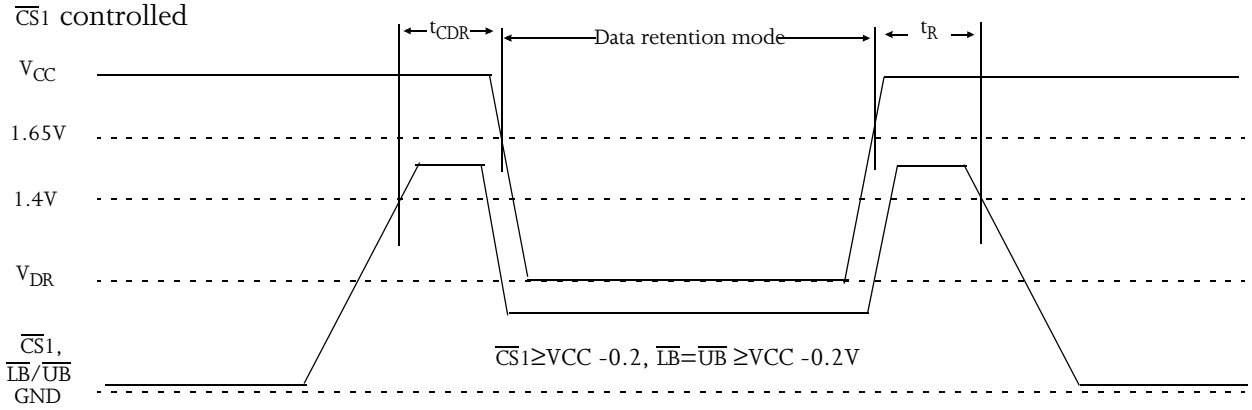
Data retention characteristics (over the operating range)[13,5]

Parameter	Symbol	Test conditions	Min	Max	Unit
V_{CC} for data retention	V_{DR}	V_{CC} = 1.0V Chip select controlled[A B] or $\overline{LB}$ / $\overline{UB}$ controlled[C] $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	1.0V	2.2	V
Data retention current	I_{CCDR}		–	8	µA
Chip deselect to data retention time	t_{CDR}		0	–	ns
Operation recovery time	t_R		t_{RC}	–	ns

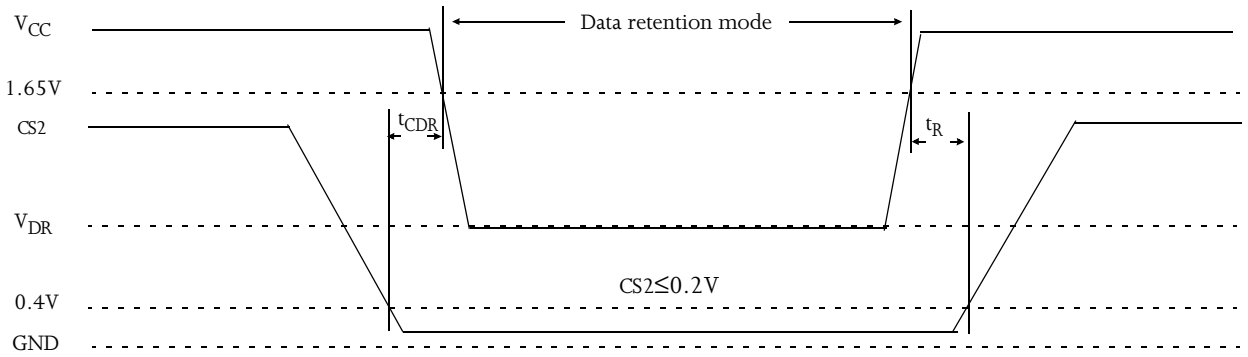
A : $\overline{CS}1$ controlled: $\overline{CS}1 \geq$ Vcc-0.2V; CS2 $\leq$ 0.2V
B : CS2 controlled: CS2 $\leq$ 0.2V
C : $\overline{LB}$ / $\overline{UB}$ controlled: $\overline{LB} = \overline{UB} \geq$ Vcc - 0.2V, CS2 $\geq$ Vcc - 0.2V

Data retention waveform

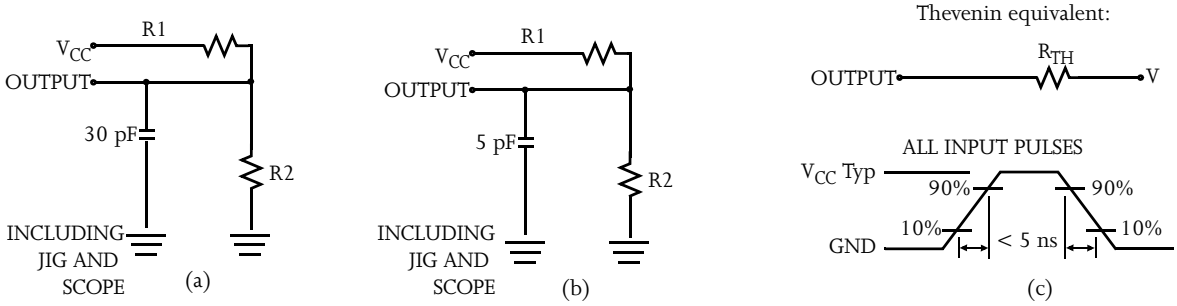
$\overline{CS}1$ controlled



CS2 controlled



AC test loads and waveforms



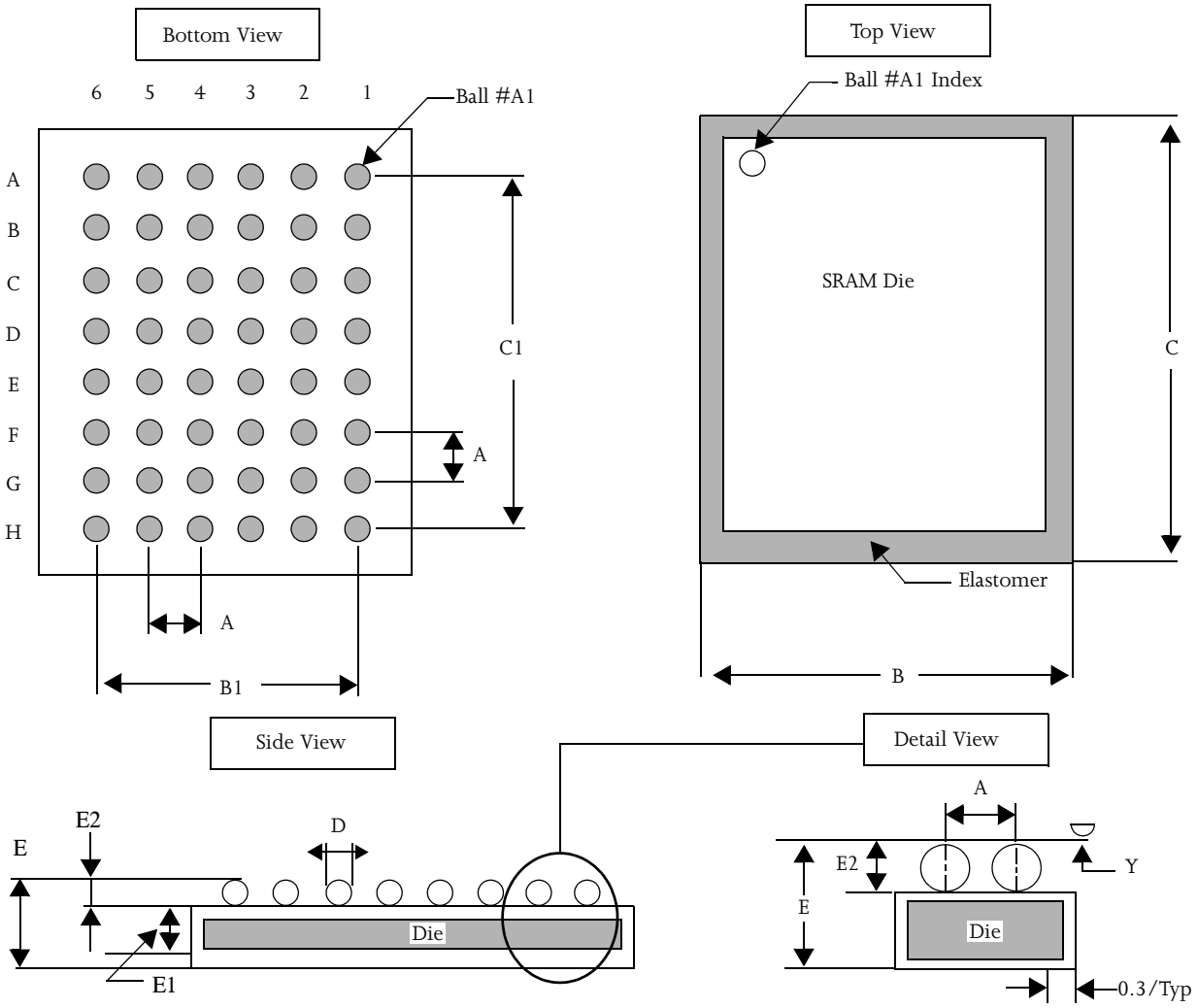
Parameters	V_{CC} = 1.8V	Unit
R1	13500	Ohms
R2	10800	Ohms
R_{TH}	6000	Ohms
V_{TH}	0.8V	Volts

Notes

1 During V_{CC} power-up, a pull-up resistor to V_{CC} on $\overline{CS}$ is required to meet I_{SB} specification.
2 This parameter is sampled, but not 100% tested.
3 For test conditions, see *AC Test Conditions*.
4 t_{CLZ} and t_{CHZ} are specified with C_L = 5pF as in Figure C. Transition is measured ±500 mV from steady-state voltage.
5 This parameter is guaranteed, but not tested.
6 $\overline{WE}$ is HIGH for read cycle.
7 $\overline{CS}1$ and $\overline{OE}$ are LOW for read cycle.
8 Address valid prior to or coincident with $\overline{CS}1$ transition LOW.
9 All read cycle timings are referenced from the last valid address to the first transitioning address.
10 $\overline{CS}1$ or $\overline{WE}$ must be HIGH during address transitions. Either $\overline{CS}1$ or $\overline{WE}$ asserting high terminates a write cycle.
11 All write cycle timings are referenced from the last valid address to the first transitioning address.
12 N/A.
13 1.0V data retention applies industrial temperature range operations.
14 C = 30pF, except at high Z and low Z parameters, where C = 5pF.

Package diagrams and dimensions

48-ball FBGA



	Minimum	Typical	Maximum
A	–	0.75	–
B	6.90	7.00	7.10
B1	–	3.75	–
C	8.4	9.0	8.6
C1	–	5.25	–
D	0.30	0.35	0.40
E	–	–	1.20
E1	–	0.68	–
E2	0.22	0.25	0.27
Y	–	–	0.08

Notes

1. Bump counts: 48 (8 row × 6 column).
2. Pitch: (x,y) = 0.75 mm × 0.75 mm (typ).
3. Units: millimeters.
4. All tolerance are ± 0.050 unless otherwise specified.
5. Typ: typical.
6. Y is coplanarity: 0.08 (max).

Ordering codes

Speed (ns)	Ordering Code	Package Type	Operating Range
70	AS6YB51216-70BI	48-ball fine pitch BGA	Industrial
85	AS6YB51216-85BI	48-ball fine pitch BGA	Industrial
70	AS6YB51216-70BC	48-ball fine pitch BGA	Commercial
85	AS6YB51216-85BC	48-ball fine pitch BGA	Commercial

Part numbering system

AS6YA	51216	B	C orI
SRAM Intelliwatt™ prefix	Device number	Package: B: CSP / BGA	Temperature range: C: Commercial: 0° C to 70° C I: Industrial: –40° C to 85° C