data sheet

fcCSP

fcCSP Packages:

Amkor Technology is now offering the Flip Chip CSP (*fc*CSP) package — a flip chip solution in a CSP package format. This package construction utilizes eutectic tin/lead (63Sn/37Pb) flip chip interconnect technology, in either area array or peripheral bump layout, replacing standard wirebond interconnect. The advantages of flip chip interconnect are twofold: it provides enhanced electrical performance over standard wirebond technology, and it allows for a smaller form factor due to increased routing density, the ability to use area array die bumps and the elimination of wirebond loops. Current wafer bump technology and flip chip assembly process allows for a minimum of 150 µm peripheral flip chip bumping, or 250 µm area array bumping.

The *fc*CSP is based on Amkor's proprietary ChipArray® BGA (CABGA) package construction, using cutting edge thin core laminate substrates. The package is assembled in strip format, gang molded and saw singulated for manufacturing efficiency and cost minimization. Laser ablated solder mask technology, via-in-pad substrate structure, and thin core substrate panel processing allow for increased routing density and enhanced electrical performance, making the *fc*CSP an attractive option for advanced CSP applications where electrical performance is a critical factor.

The *fc*CSP is available in both thin core laminate substrate technology, as well as ceramic substrate technology. Package size ranges from 3 mm to 15 mm, accommodating BGA ball pitches from 0.5 mm to 1.0 mm. In addition to BGA technology, the *fc*CSP is also available in LGA format, allowing for a lower minimum package thickness.

The Ceramic flip chip package provides maximum flexibility for designers for number of layers and routing. Current production is from 300 - 1800 I/O in LGA, BGA or SCI (solder column interposer) formats, 1.27 mm and 1.0 mm pitch. AlSiC lids can be attached for maximum thermal dissipation.

Features:

- Designed for high frequency applications
- 49 - 1800 ball counts
- Target Market - Cell Phones, Hand-held Electronics
- Thin core laminate or ceramic package construction
- Overmolded for handling and second level reliability
- Accommodates package sizes from 3 mm to 15 mm
- Flip Chip bump pitches of 150 µm min. for peripheral array, 250 µm min. for area array
- Available in 0.5 mm - 1.0 mm BGA ball pitch, as well as LGA interconnect
- Minimum nominal package thickness of 0.80 mm for LGA interconnect, 1.0 mm for 0.5 mm BGA pitch, 1.2 mm for 0.8 mm pitch
- Turnkey Solution - Design, bumping, bumped wafer probe, backgrind, assembly, test
- Much better signal to noise ratio at higher frequencies (>1Ghz)
- Low inductance of flip chip bumps - short, direct signal path
- Flexible customized substrate routing

Thermal Performance:

Theta JA (°CW)

- 8 x 8 mm, 64 lead package with 1.75 mm x 2.27 mm die, 0.8 mm pitch, 0.6 mm mold cap
- 0 LFPM, 4 layer PC board
- Junction ambient thermal resistance = 48.1 °C/W

Electrical:

8 x 8 mm body, 64 ld, 0.8 mm ball pitch

	Min	Max
Inductance	0.26 nH	2.16 nH
Capacitance	0.18 pF	0.38 pF
Resistance	7 mΩ	53.9 mΩ

Simulated results @ at 100 MHz

Reliability:

Package Level:

• Laminate Moisture Sensitivity	JEDEC Level 3 @ 240 °C 30 °C/60% RH, 192 hours
• Ceramic Moisture Sensitivity	JEDEC Level 1 @ 260 °C 85 °C/85% RH, 168 hours
• PCT	121 °C/100% RH, 96 hours
• Temp/Humidity	85 °C/85% RH, 1000 hours
• High temp storage	150 °C, 1000 hours
• Temp cycle	-55 °C/+125 °C, 1000 cycles

Board Level:

• Thermal cycle	-40 °C/+125 °C, 1 cycle/hour, 3000 cycles*
• Thermal cycle	-40 °C/+125 °C, 2 cycles/hour, 2500 cycles*

*Data for 8 x 8 mm body, 64 lead, 0.33 mm PWB NSMD pad size

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Amkor Technology®

data sheet

*fc*CSP

*fc*BGA (Flip Chip BGA):

Moderate routing density, lowest cost flip chip package in intermediate ball counts. Bare die or Single Piece Lid. Qualified with both BU and 4L thin core substrates. Ball Count range is 256 - 1900 and Body Size range is 17 - 45 mm.

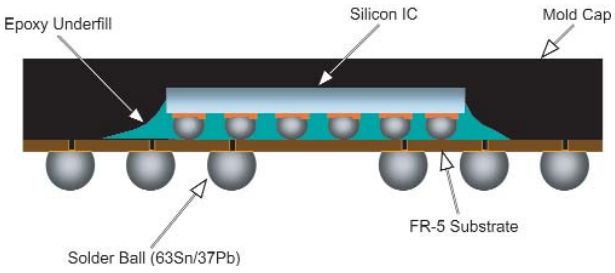
Ceramic *fc*BGA (Ceramic Flip Chip BGA):

Alumina or HiTCE flip chip packages with BGA, LGA, or SCI interconnect format. Capability for high layer count enables most flexible format for different ground and power planes. Available in bare die, AlSiC Lid, or low cost Flat Lid. Qualified in body sizes ti 45 mm HiTCE (BGA), 45 mm alumina (SCI) and 31 mm alumina (BGA).

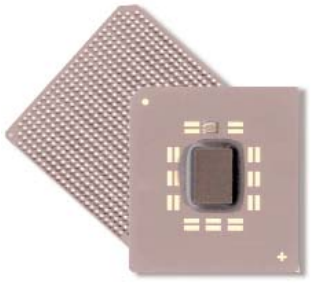
Applications:

The fcCSP package is targeted to high-performance workstations, servers, data communication products, internet routers and at high frequency and RF packaging applications where electrical performance is critical. The elimination of wirebond loops allows for a low inductance connection to the die, while the increased routing density enables optimized electrical paths for critical high frequency signal lines. The fcCSP is also an attractive option for portable and handheld electronics where, in addition to performance, package size is critical.

Cross-section *fc*CSP



Ceramic *fc*BGA



Process Highlights

Die size (max)	Pkg size - 1 mm
Bump pitch (min)	Pkg size - 1 mm
In-line	150 µm
Minimum array	250 µm

Standard Materials

Package substrate	Hitachi FR5 E679 / BT
Bump	63/37 Sn/Pb
Encapsulant	Epoxy mold compound
Solder balls	Eutectic SnPb

Test Services

- Program generation/conversion
- Product engineering
- Wafer sort
- -55 °C to +165 °C test available
- Burn-in

Shipping

JEDEC trays
Tape and reel services

Configuration Options:

Package Offering (units in mm)

Body Size	Pitch	Ball Count	Matrix
8 x 8	1.0	49	Full
9 x 9	1.0	64	Full
10 x 10	1.0	81	Full
11 x 11	1.0	100	Full
12 x 12	1.0	121	Full
13 x 13	1.0	144	Full
14 x 14	1.0	169	Full
15 x 15	1.0	196	Full
6 x 6	0.8	49	Full
7 x 7	0.8	64	Full
8 x 8	0.8	64	Full
8 x 8	0.8	81	Full
9 x 9	0.8	100	Full
10 x 10	0.8	144	Full
11 x 11	0.8	169	Full
12 x 12	0.8	196	Full
3 x 3	0.5	25	Full
4 x 4	0.5	36	Full
5 x 5	0.5	48	2 Row
5 x 5	0.5	64	Full
6 x 6	0.5	64	2 Row
6 x 6	0.5	84	3 Row
7 x 7	0.5	80	2 Row
7 x 7	0.5	108	3 Row
8 x 8	0.5	96	2 Row
8 x 8	0.5	132	3 Row
9 x 9	0.5	156	3 Row
10 x 10	0.5	180	3 Row