SIEMENS

3.3V 256 K x 16-Bit Dynamic RAM — HYB 314171BJ-50/-60/-70

3.3V Low Power 256 K x 16-Bit Dynamic RAM with Self Refresh — HYB 314171BJL-50/-60/-70

- 262 144 words by 16-bit organization
- 0 to 70 °C operating temperature
- Fast access and cycle time
- $\overline{RAS}$ access time:
  50 ns (-50 version)
  60 ns (-60 version)
  70 ns (-70 version)
- $\overline{CAS}$ access time:
  15ns (-50,-60 version)
  20 ns (-70 version)
- Cycle time:
  95 ns (-50 version)
  110 ns (-60 version)
  130 ns (-70 version)
- Fast page mode cycle time
  35 ns (-50 version)
  40 ns (-60 version)
  45 ns (-70 version)
- Single + 3.3 V (± 0.3 V) supply with a built-in VBB generator
- Low Power dissipation
  max. 450 mW active (-50 version)
  max. 378 mW active (-60 version)
  max. 306 mW active (-70 version)
- Standby power dissipation
  7.2 mW standby (TTL)
  3.6 mW max. standby (CMOS)
  0.72 mW max. standby (CMOS) for Low Power Version
- Output unlatched at cycle end allows two-dimensional chip selection
- Read, write, read-modify write, CAS-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, hidden-refresh and fast page mode capability
- 2 $\overline{CAS}$ / 1 $\overline{WE}$ control
- Self Refresh (L-Version)
- All inputs and outputs TTL-compatible
- 512 refresh cycles / 16 ms
- 512 refresh cycles / 128 ms
  Low Power Version only
- Plastic Packages:
  P-SOJ-40-1 400mil width

The HYB 314171BJ/BJL is a 4 MBit dynamic RAM organized as 262 144 words by 16-bit. The HYB 314171BJ/BJL utilizes CMOS silicon gate process as well as advanced circuit techniques to provide wide operation margins, both internally and for the system user. Multiplexed address inputs permit the HYB 314171BJ/BJL to be packed in a standard plastic 400mil wide P-SOJ-40-1 package. This package size provides high system bit densities and is compatible with commonly used automatic testing and insertion equipment. System oriented features include Self Refresh (L-Version), single + 3.3 V (± 0.3 V) power supply, direct interfacing with high performance logic device families.

Ordering Information

Type	Ordering Code	Package	Description
HYB 314171BJ-50		P-SOJ-40-1	3.3V 50ns 256 K x 16 DRAM
HYB 314171BJ-60		P-SOJ-40-1	3.3V 60 ns 256 K x 16 DRAM
HYB 314171BJ-70		P-SOJ-40-1	3.3V 70 ns 256 K x 16 DRAM
HYB 314171BJL-50		P-SOJ-40-1	3.3V 50 ns 256 K x 16 DRAM
HYB 314171BJL-60		P-SOJ-40-1	3.3V 60 ns 256 K x 16 DRAM
HYB 314171BJL-70		P-SOJ-40-1	3.3V 70 ns 256 K x 16 DRAM

Truth Table

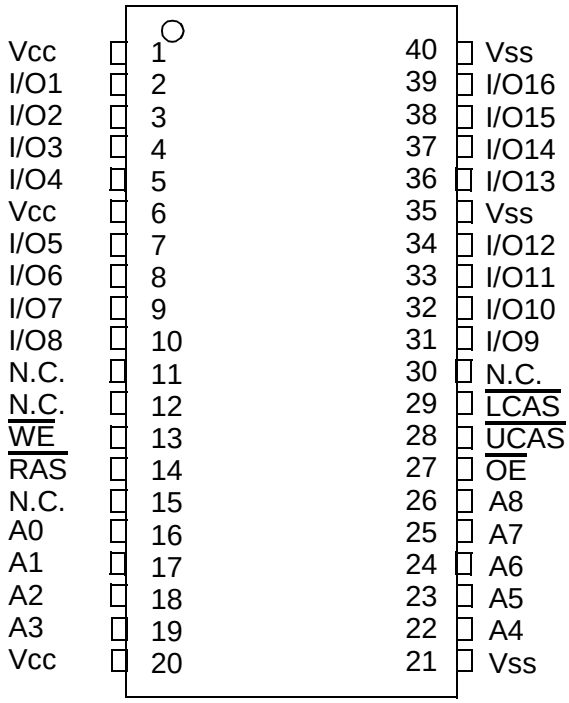
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	I/O1-I/O8	I/O9-I/O16	Operation
H	H	H	H	H	High-Z	High-Z	Standby
L	H	H	H	H	High-Z	High-Z	Refresh
L	L	H	H	L	Dout	High-Z	Lower byte read
L	H	L	H	L	High-Z	Dout	Upper byte read
L	L	L	H	L	Dout	Dout	Word read
L	L	H	L	H	Din	Don't care	Lower byte write
L	H	L	L	H	Don't care	Din	Upper byte write
L	L	L	L	H	Din	Din	Word write
L	L	L	H	H	High-Z	High-Z	

Pin Names

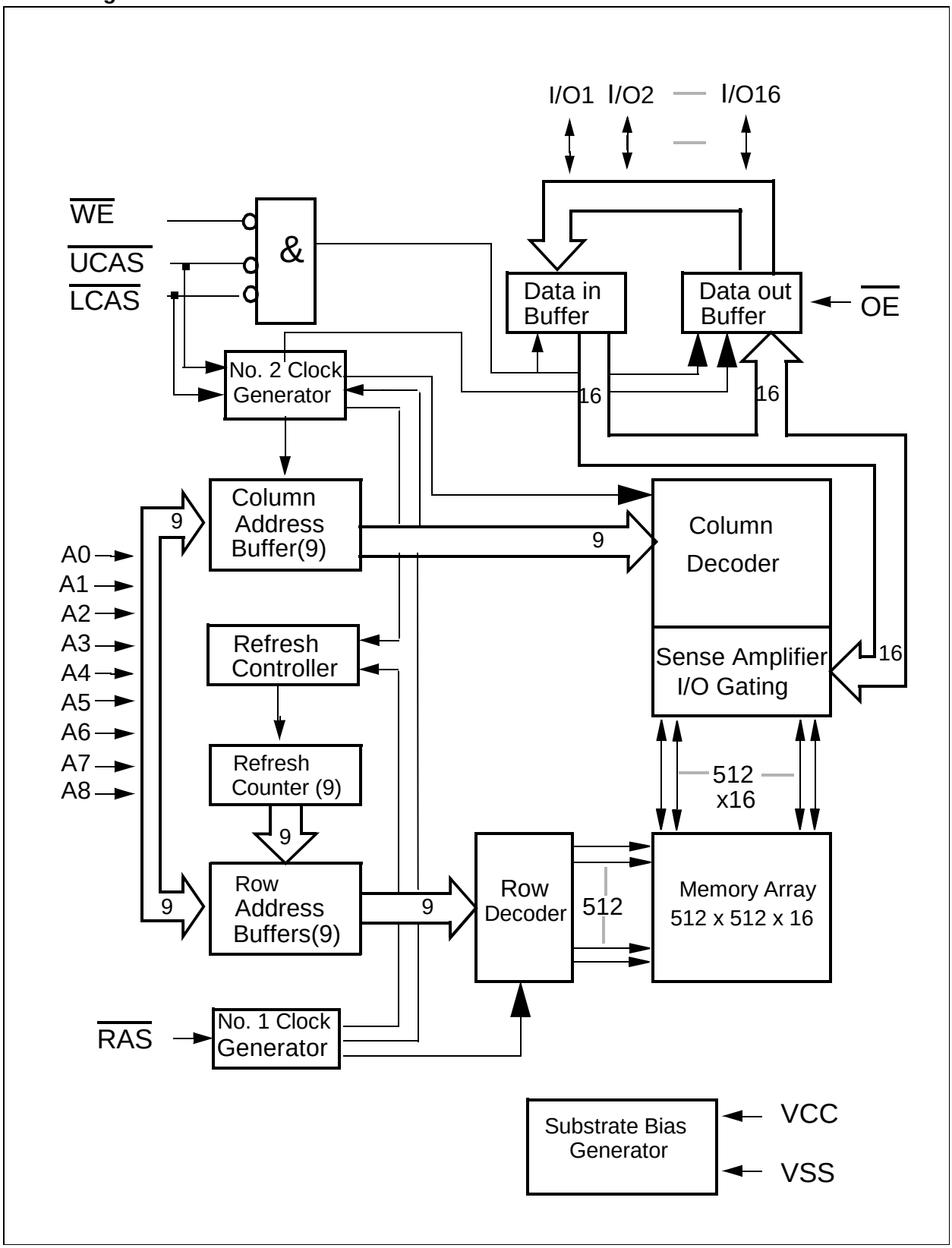
A0-A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$, $\overline{LCAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1 – I/O16	Data Input/Output
V_{CC}	Power Supply (+ 3.3 V)
V_{SS}	Ground (0 V)
N.C.	No Connection

Pin Configuration

P-SOJ-40-1



Block Diagram



Absolute Maximum Ratings

Operating temperature range .....0 to + 70 °C
Storage temperature range.....– 55 to + 150 °C
Input/output voltage .....– 1 to (Vcc+0.5, 4.6) V
Power supply voltage.....– 1 to +4.6 V
Data out current (short circuit) ..... 50 mA

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC Characteristics

lV T_A = 0 to 70 °C; V_{SS} = 0 V; V_{CC} = 3.3 V ± 0.3 V, t_T = 5 ns

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input high voltage	V_{IH}	2.0	Vcc+0.5	V	1
Input low voltage	V_{IL}	– 1.0	0.8	V	1
LVTTL Output high voltage (I_{OUT} = – 2.0 mA)	V_{OH}	2.4	–	V	1
LVTTL Output low voltage (I_{OUT} = 2 mA)	V_{OL}	–	0.4	V	1
Input leakage current, any input (0 V < V_{IN} < Vcc+0.3 V, all other inputs = 0 V)	$I_{I(L)}$	– 10	10	µA	1
Output leakage current (DO is disabled, 0 V < V_{OUT} < V_{CC} + 0.3 V)	$I_{O(L)}$	– 10	10	µA	1
Average V_{CC} supply current: -50 version -60 version -70 version	I_{CC1}		125 105 85	mA	2, 3, 4
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{LCAS}$ = $\overline{UCAS}$ = $\overline{WE}$ = V_{IH})	I_{CC2}		2	mA	
Average V_{CC} supply current during $\overline{RAS}$-only refresh cycles: -50 version -60 version -70 version	I_{CC3}		125 105 85	mA	2, 4

DC Characteristics (cont'd)

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Average V_{CC} supply current during fast page mode operation: -50 version -60 version -70 version	I_{CC4}		70 65 60	mA	2, 3, 4
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{LCAS}$ = $\overline{UCAS}$ = $\overline{WE}$ = V_{CC} – 0.2 V)	I_{CC5}		1	mA	1
Average V_{CC} supply current during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode: -50 version -60 version -70 version	I_{CC6}		125 105 85	mA	2, 4
Standby V_{CC} current (L-version) ($\overline{RAS}$ = $\overline{LCAS}$ = $\overline{UCAS}$ = $\overline{WE}$= V_{CC} – 0.2 V)	I_{CC5}		200	µA	
Self Refresh Current (L-version) ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$ = 0.2V A0 – A8 = V_{CC} – 0.2 V or 0.2 V)	I_{CCS}		250	µA	

Capacitance

T_A = 0 to 70 °C; V_{CC} = 3.3 V ± 0.3 V, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A8)	C_{I1}	–	6	pF
Input capacitance ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WE}$, $\overline{OE}$)	C_{I2}	–	7	pF
Output capacitance (I/O1 to I/O16)	C_{IO}	–	7	pF

AC Characteristics [5)6)]

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{CC} = 3.3 V ± 0.3 V, t_T = 5 ns

Parameter	Symbol	Limit Values						Unit	Note
		- 50		- 60		- 70			
		min.	max.	min.	max.	min.	max.		
common parameters									
Random read or write cycle time	t_{RC}	95	–	110	–	130	–	ns	
$\overline{RAS}$ precharge time	t_{RP}	35	–	40	–	50	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10k	60	10k	70	10k	ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10k	15	10k	20	10k	ns	
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns	
Row address hold time	t_{RAH}	10	–	10	–	10	–	ns	
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns	
Column address hold time	t_{CAH}	10	–	15	–	15	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	35	20	45	20	50	ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	ns	
$\overline{RAS}$ hold time	t_{RSH}	15	–	15	–	20	–	ns	
$\overline{CAS}$ hold time	t_{CSH}	50	–	60	–	70	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	5	–	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	7
Refresh period	t_{REF}	–	16	–	16	–	16	ms	
Refresh period (L-version)	t_{REF}	–	128	–	128	–	128	ms	
Read Cycle									
Access time from $\overline{RAS}$	t_{RAC}	–	50	–	60	–	70	ns	8, 9
Access time from $\overline{CAS}$	t_{CAC}	–	15	–	15	–	20	ns	8, 9
Access time from column address	t_{AA}	–	25	–	30	–	35	ns	8,10
$\overline{OE}$ access time	t_{OEA}	–	15	–	15	–	20	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	–	30	–	35	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	0	–	ns	11
Read command hold time ref. to $\overline{RAS}$	t_{RRH}	0	–	0	–	0	–	ns	11
$\overline{CAS}$ to output inlow-Z	t_{CLZ}	0	–	0	–	0	–	ns	8

Parameter	Symbol	Limit Values						Unit	Note
		- 50		- 60		- 70			
		min.	max.	min.	max.	min.	max.		
Output buffer turn-off delay from $\overline{CAS}$	t_{OFF}	0	15	0	20	0	20	ns	12
Output buffer turn-off delay from $\overline{OE}$	t_{OEZ}	0	15	0	20	0	20	ns	12
Data to $\overline{OE}$ low delay	t_{DZO}	0	–	0	–	0	–	ns	13
$\overline{CAS}$ high to datadelay	t_{CDD}	15	–	20	–	20	–	ns	14
$\overline{OE}$ high to data delay	t_{ODD}	15	-	20	–	20	–	ns	14
Write Cycle									
Write command hold time	t_{WCH}	10	–	10	–	15	–	ns	
Write command pulse width	t_{WP}	10	–	10	–	15	–	ns	
Write command setup time	t_{WCS}	0	–	0	–	0	–	ns	15
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	–	15	–	20	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	–	15	–	20	–	ns	
Data setup time	t_{DS}	0	–	0	–	0	–	ns	16
Data hold time	t_{DH}	10	–	15	–	15	–	ns	16
Data to $\overline{CAS}$ lowdelay	t_{DZC}	0	–	0	–	0	–	ns	13
Read-modify-Write Cycle									
Read-write cycle time	t_{RWC}	140	–	160	–	185	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	75	–	90	–	100	–	ns	15
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	40	–	45	–	50	–	ns	15
Column address to $\overline{WE}$ delay time	t_{AWD}	50	–	60	–	65	–	ns	15
$\overline{OE}$ command hold time	t_{OEH}	15	–	20	–	20	–	ns	
Fast Page Mode Cycle									
Fast page mode cycle time	t_{PC}	35	–	40	–	45	–	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	10	–	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	30	–	35	–	40	ns	7
$\overline{RAS}$ pulse width	t_{RASP}	50	200k	60	200k	70	200k	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30	–	35	–	40	–	ns	

Parameter	Symbol	Limit Values						Unit	Note
		- 50		- 60		- 70			
		min.	max.	min.	max.	min.	max.		
Fast Page Mode Read Modify Write Cycle									
Fast page mode read/write cycle time	t_{PRWC}	80	–	90	–	100	–	ns	
$\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	55	–	60	–	65	–	ns	
$\overline{CAS}$ before $\overline{RAS}$ refresh Cycle									
$\overline{CAS}$ setup time	t_{CSR}	5	–	5	–	5	–	ns	
$\overline{CAS}$ hold tim	t_{CHR}	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	0	–	0	–	0	–	ns	
Write to $\overline{RAS}$ precharge time	t_{WRP}	10	–	10	–	10	–	ns	
Write to $\overline{RAS}$ hold time	t_{WRH}	10	–	10	–	10	–	ns	
$\overline{CAS}$-before $\overline{RAS}$ counter test cycle									
$\overline{CAS}$ precharge time	t_{CPT}	25	–	30	–	40	–	ns	
Self Refresh Cycle (L-Version only)									
$\overline{RAS}$ pulse width	t_{RASS}	100	–	100	–	100	–	µs	
$\overline{RAS}$ precharge time	t_{RPS}	95	–	110	–	130	–	ns	
$\overline{CAS}$ hold time Self Refresh	t_{CHS}	35	–	40	–	50	–	ns	

Notes:

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.

4) Address can be changed once or less while RAS = Vil. In case of ICC4 it can be changed once or less during a page mode cycle

5) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using the internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6) AC measurements assume t_T = 5 ns.

7) $V_{IH\ (min.)}$ and $V_{IL\ (max.)}$ are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.

8) Measured with a load equivalent to 100 pF and at Voh=2.0V (Ioh=-2mA), Vol=0.8V (Iol=2mA).

9) Operation within the $t_{RCD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RCD\ (max.)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD\ (max.)}$ limit, then access time is controlled by t_{CAC}.

10) Operation within the $t_{RAD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RAD\ (max.)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD\ (max.)}$ limit, then access time is controlled by t_{AA}.

11) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

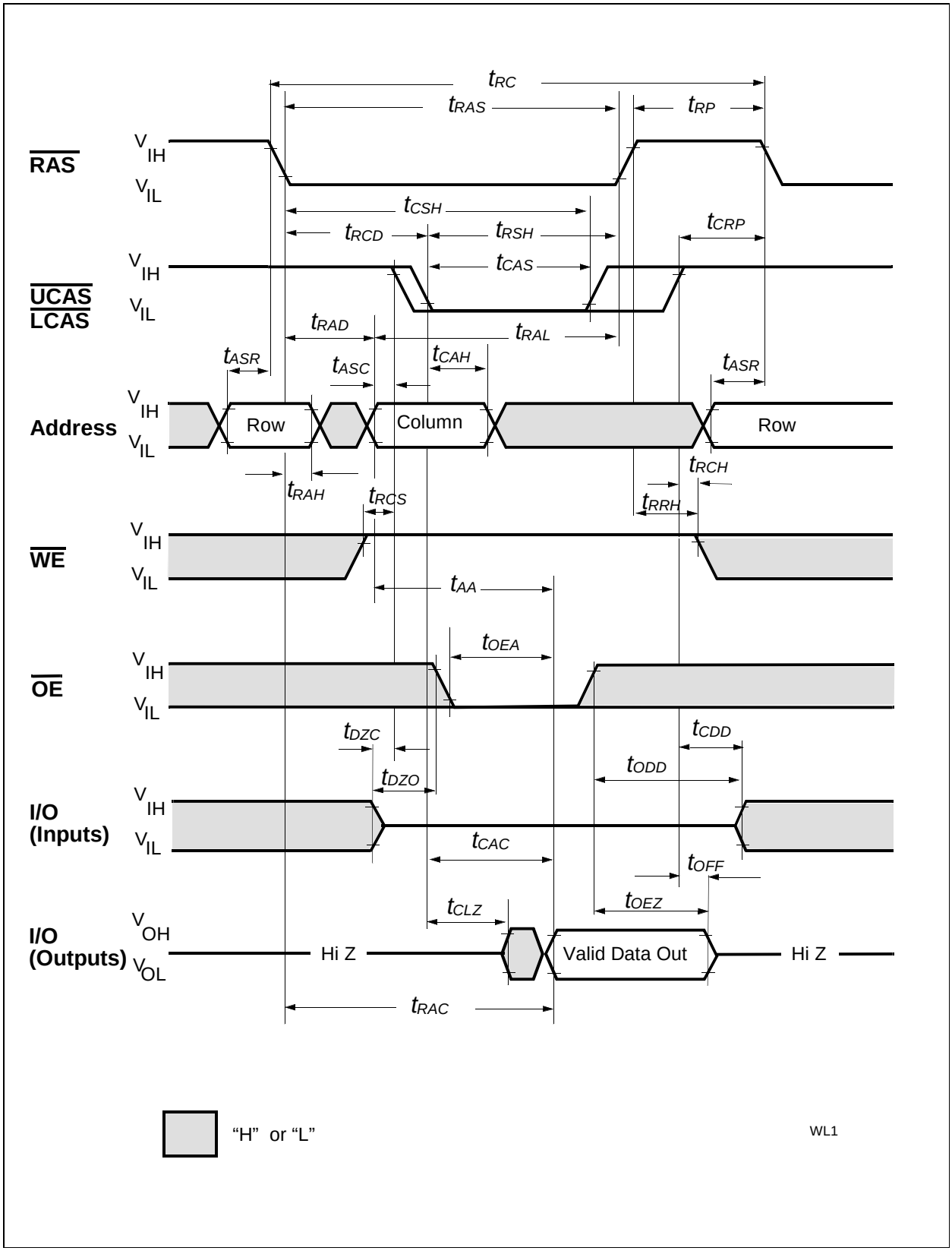
12) $t_{OFF\ (max.)}$, $t_{OEZ\ (max.)}$ define the time at which the output achieves the open-circuit conditions and are not referenced to output voltage levels.

13) Either t_{DZC} or t_{DZO} must be satisfied.

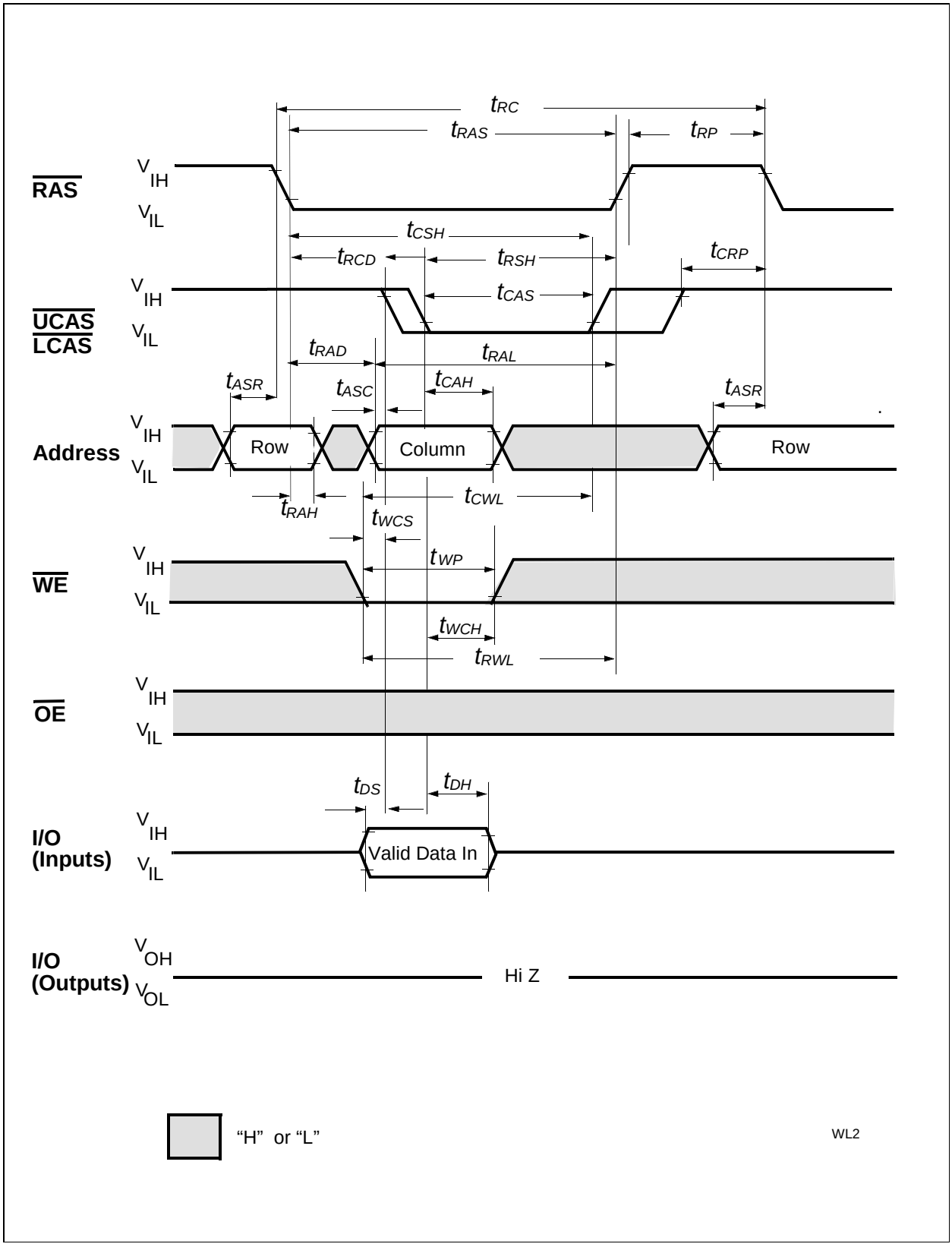
43) Either t_{CDD} or t_{ODD} must be satisfied.

15) t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS\ (min.)}$, the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} > t_{RWD\ (min.)}$, $t_{CWD} > t_{CWD\ (min.)}$ and $t_{AWD} > t_{AWD\ (min.)}$, the cycle is a read-write cycle and I/O will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of I/O (at access time) is indeterminate.

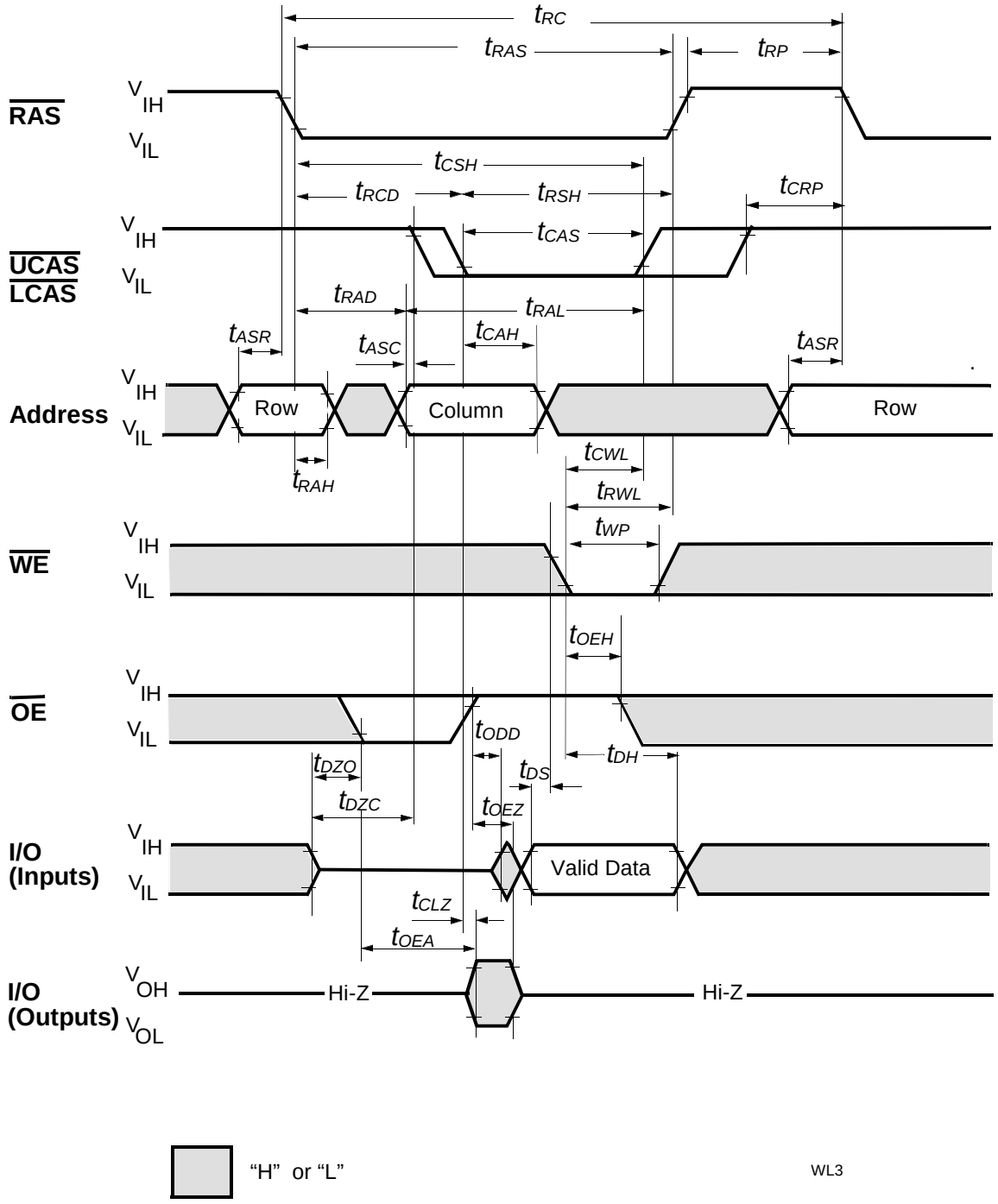
16) These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
tCAS
UCAS
LCAS
tRAD
tRAL
tASR
tASC
tCAH
tASR
Address
Row
Column
Row
tRCH
tRAH
tRCS
tRRH
WE
tAA
tOEA
OE
tDZC
tCDD
tDZO
tODD
I/O
(Inputs)
tCAC
tOFF
tOEZ
tCLZ
I/O
(Outputs)
VOH
VOL
Hi Z
Valid Data Out
Hi Z
tRAC
"H" or "L"
WL1

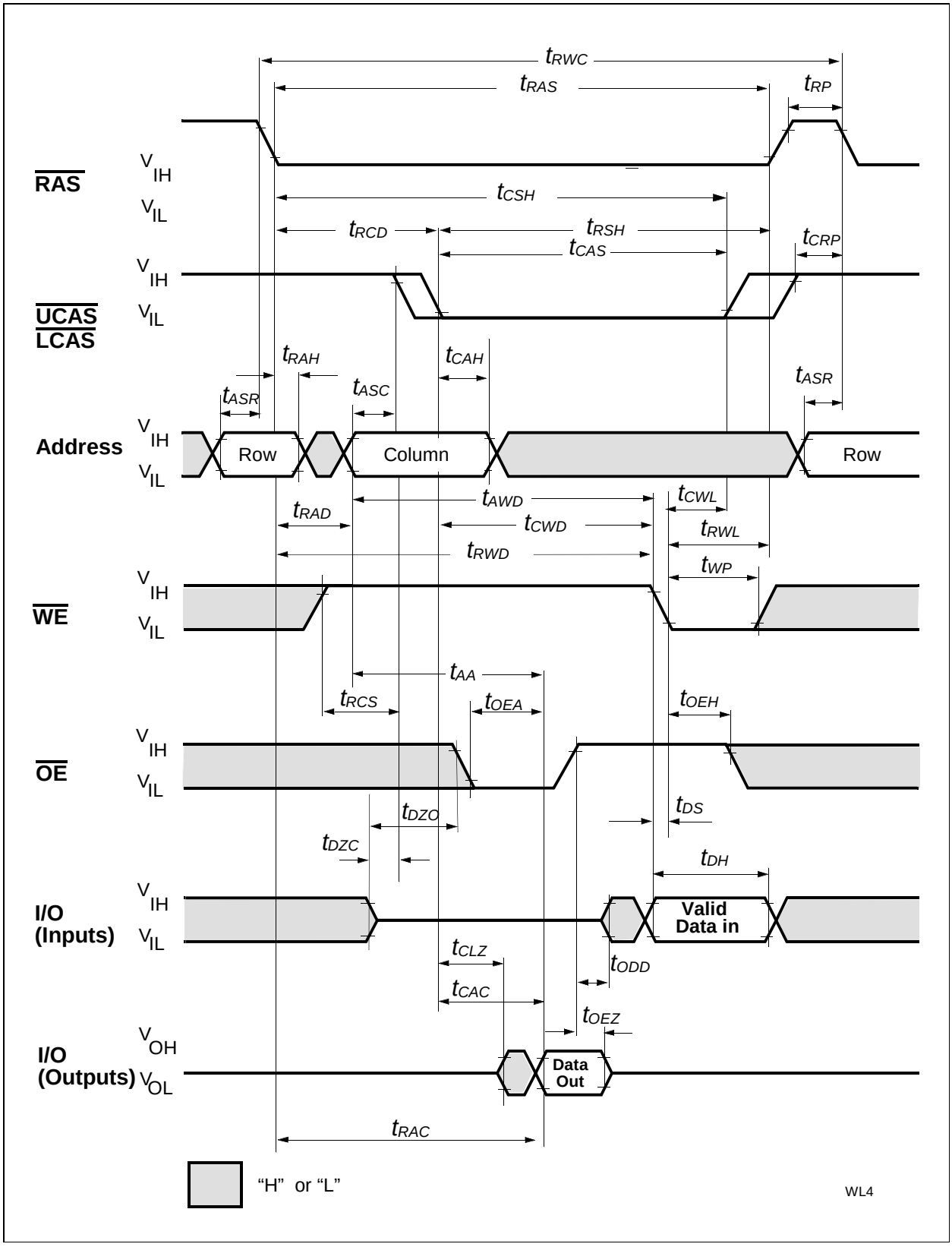
Read Cycle



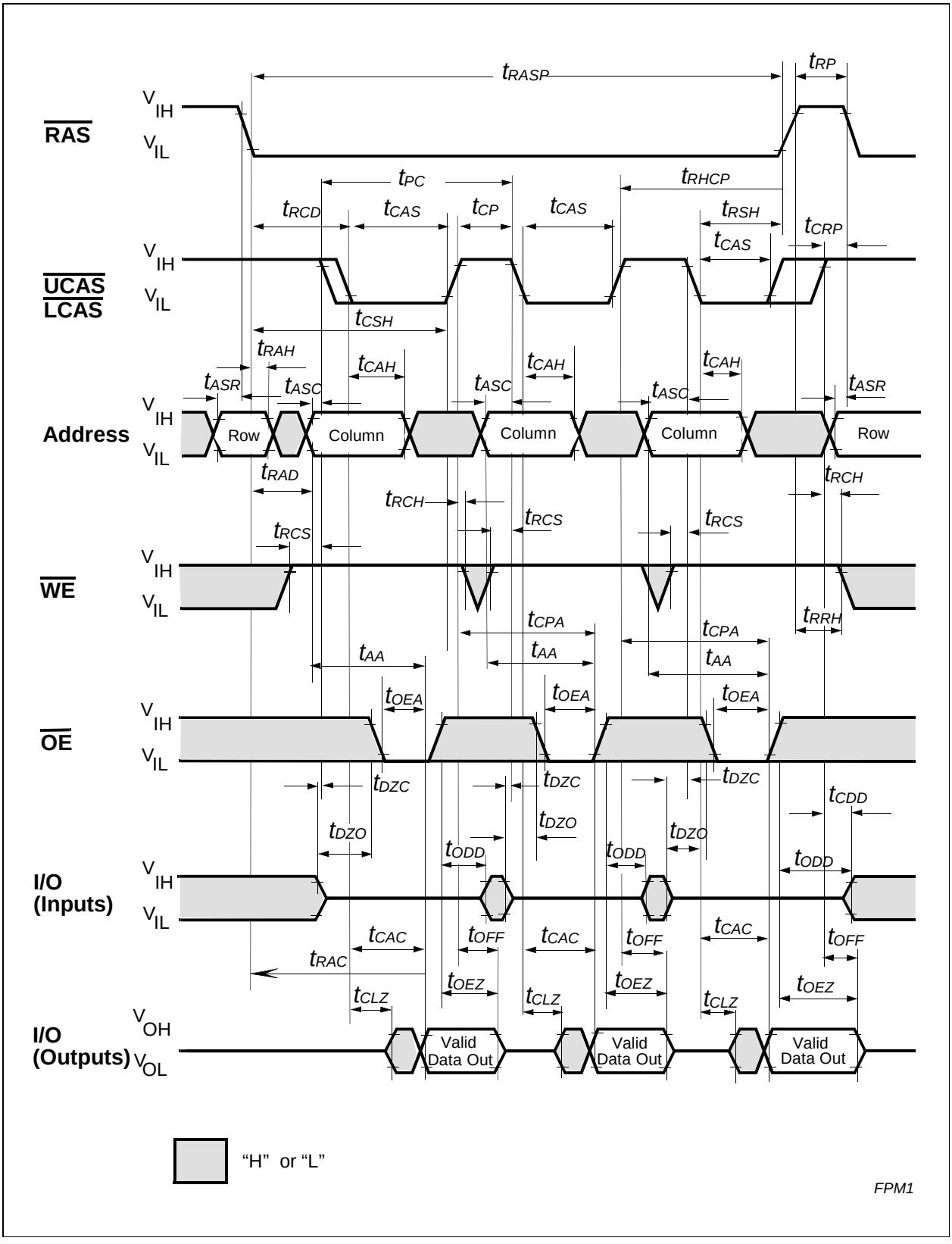
Write Cycle (Early Write)



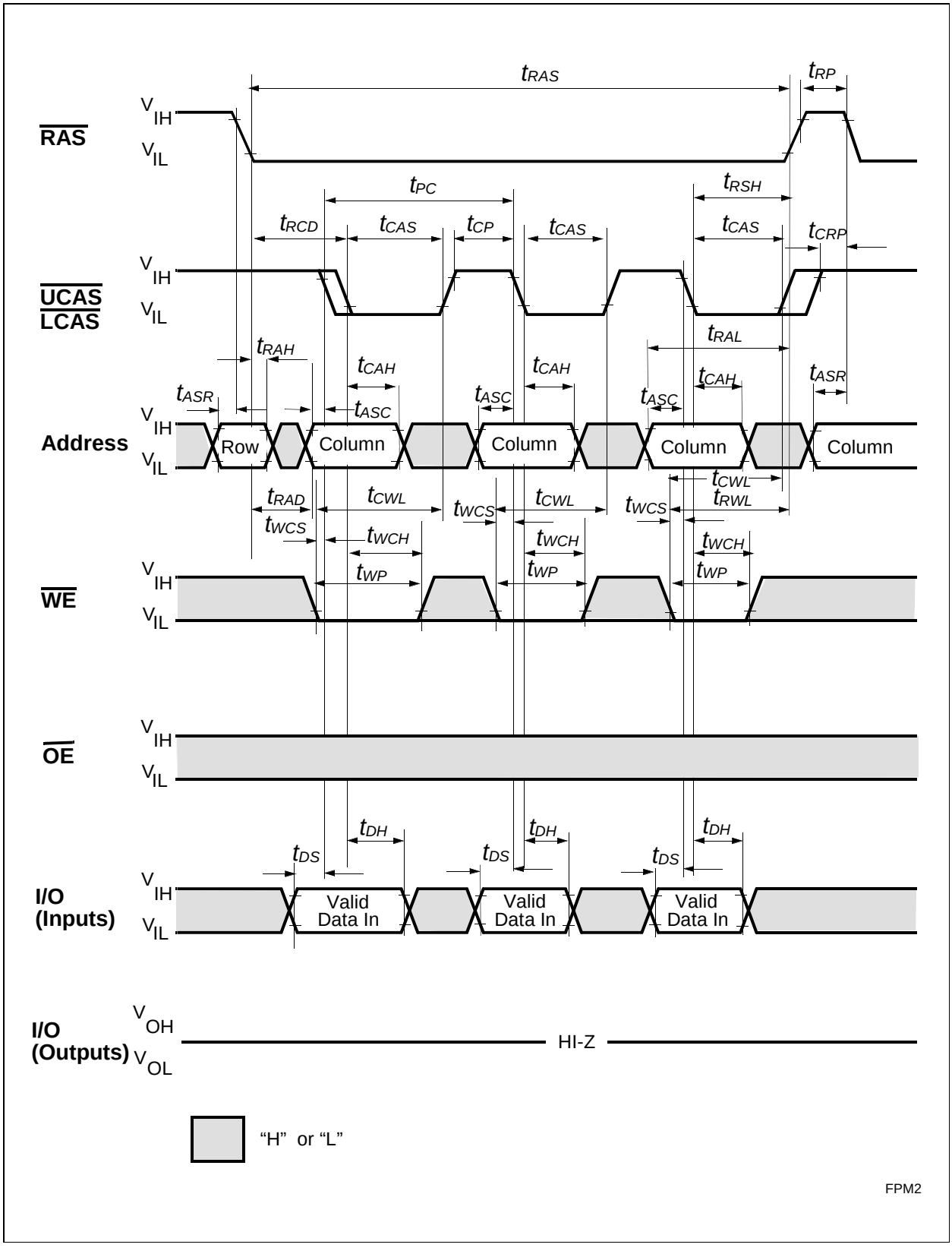
Write Cycle ($\overline{OE}$ Controlled Write)



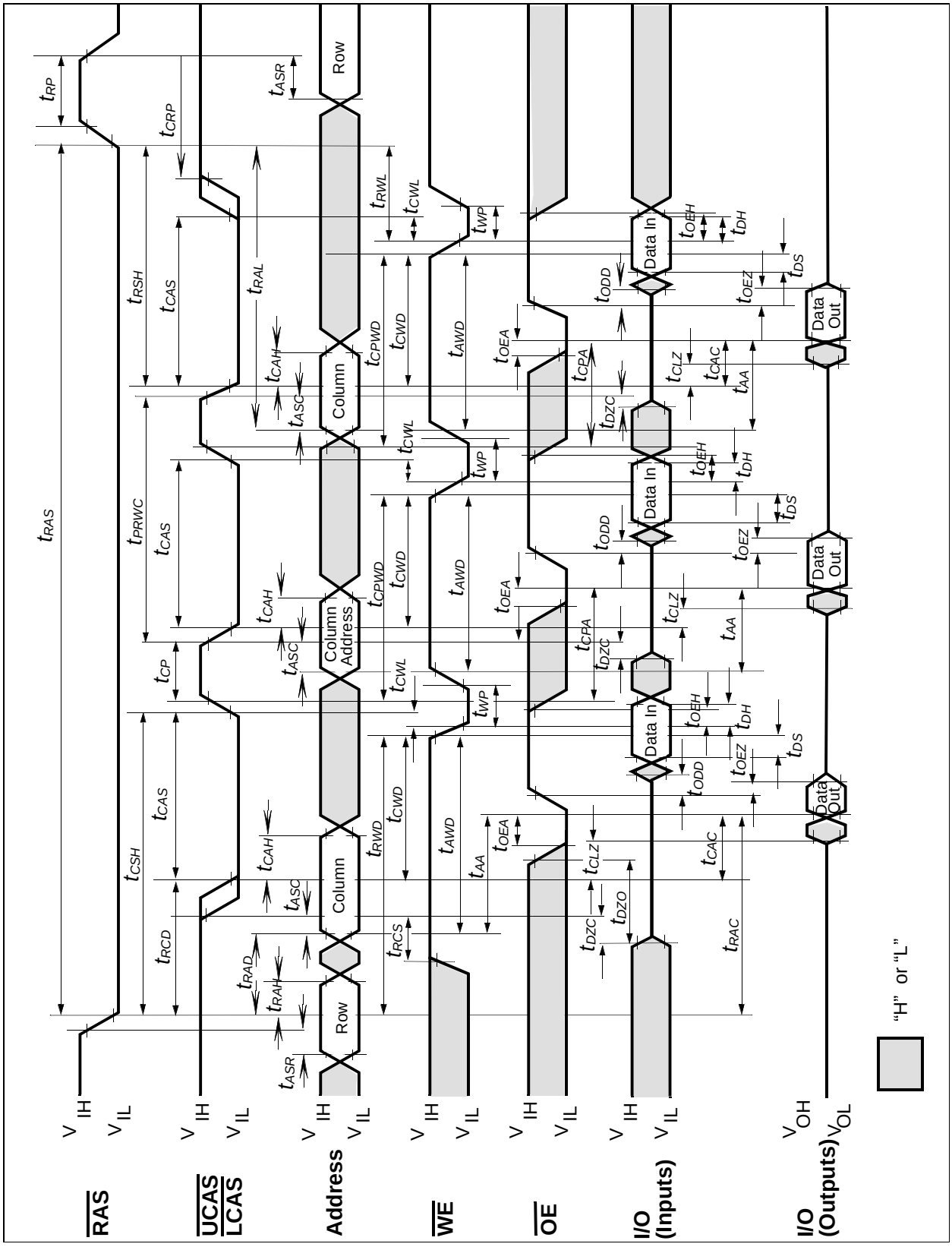
Read-Write (Read-Modify-Write) Cycle



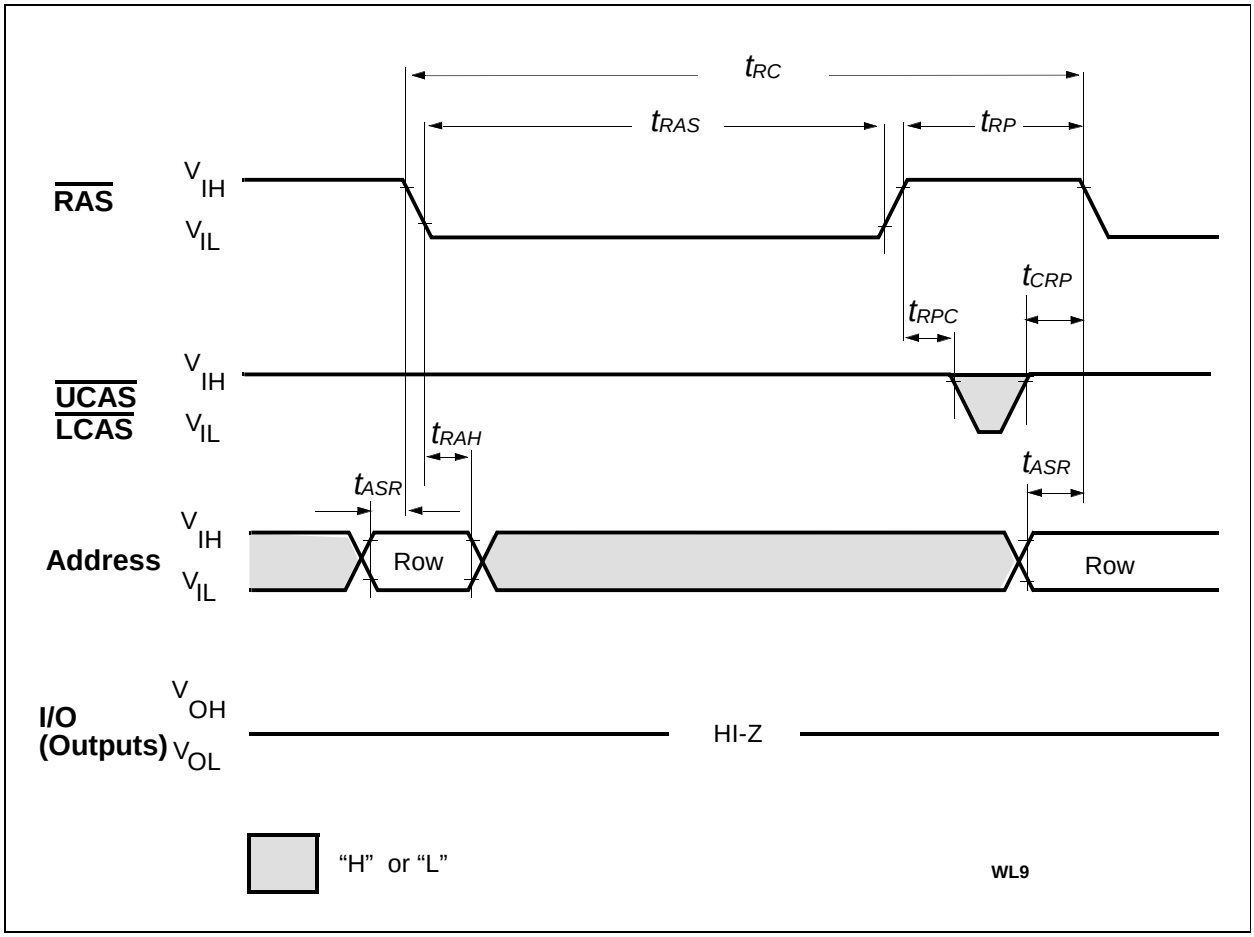
Fast Page Mode Read Cycle



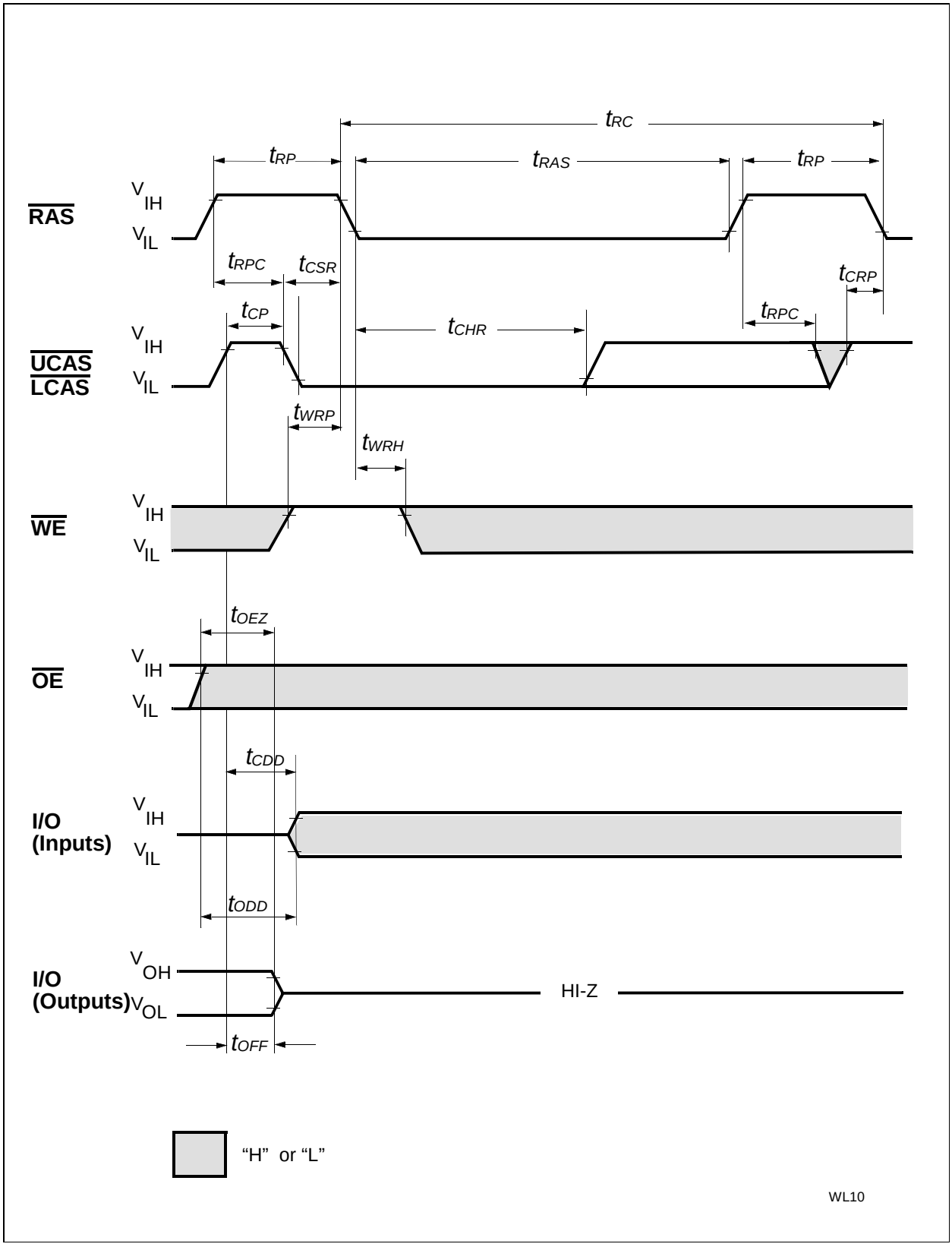
Fast Page Mode Early Write Cycle



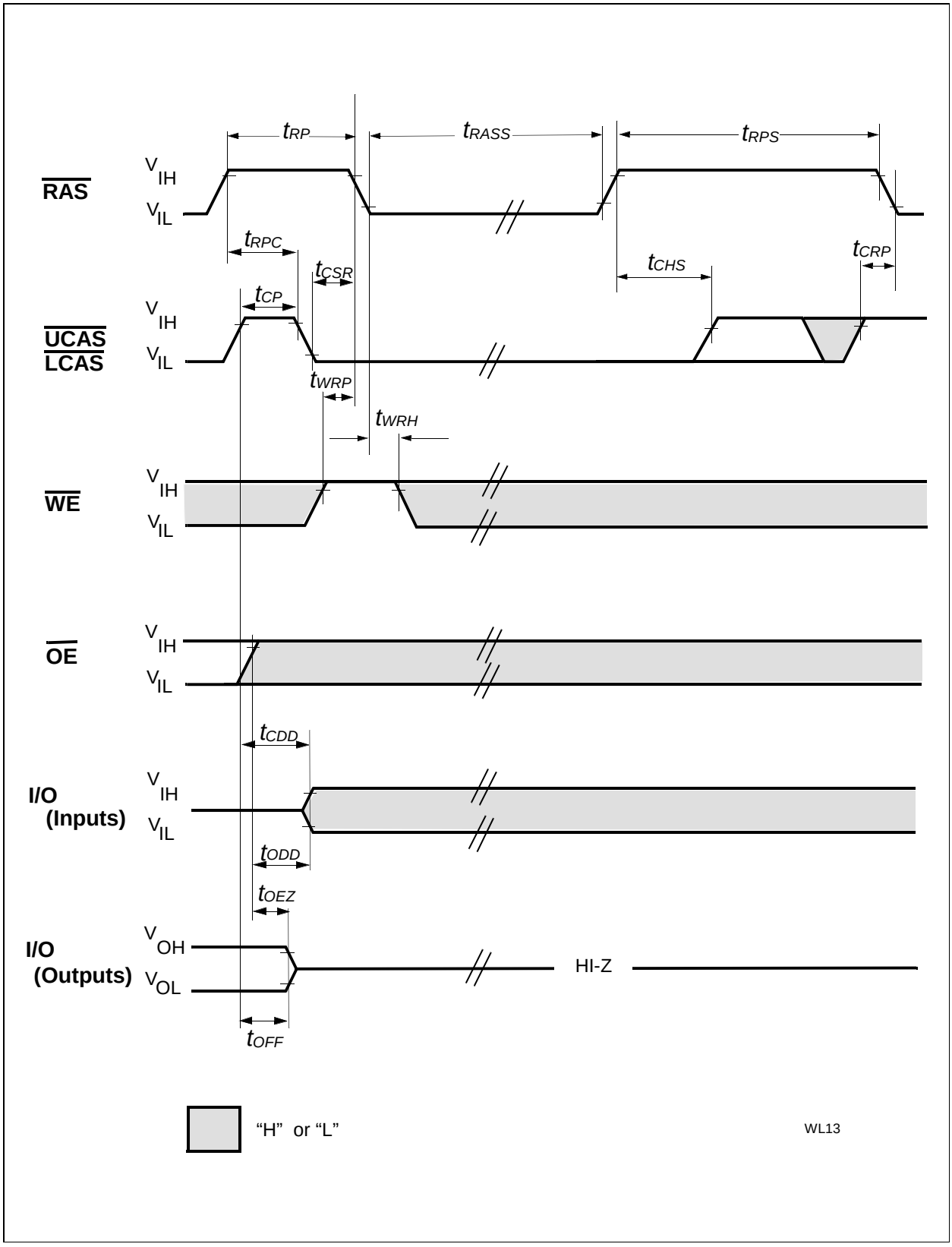
Fast Page Mode Read-Modify-Write Cycle



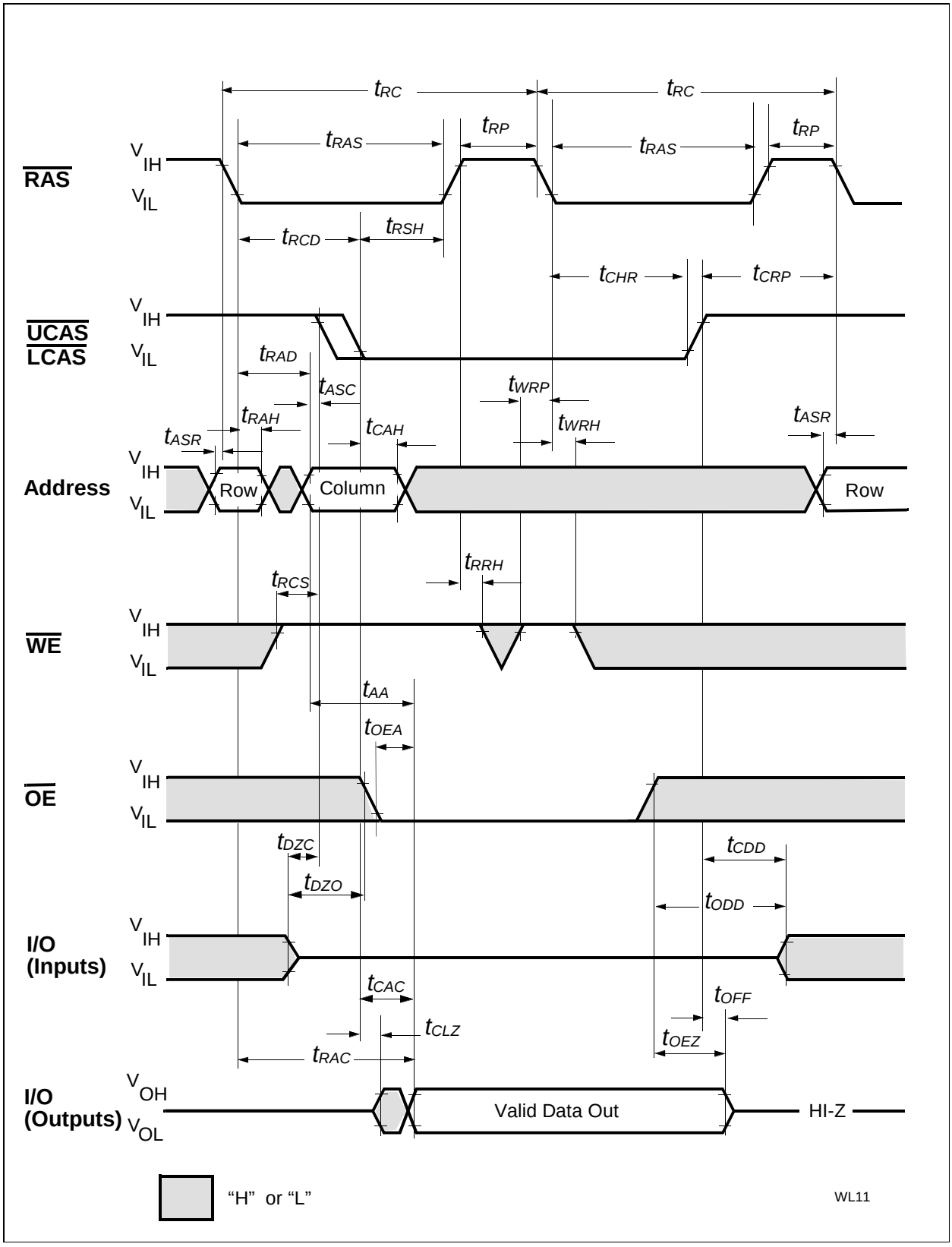
$\overline{\text{RAS}}$-Only Refresh Cycle



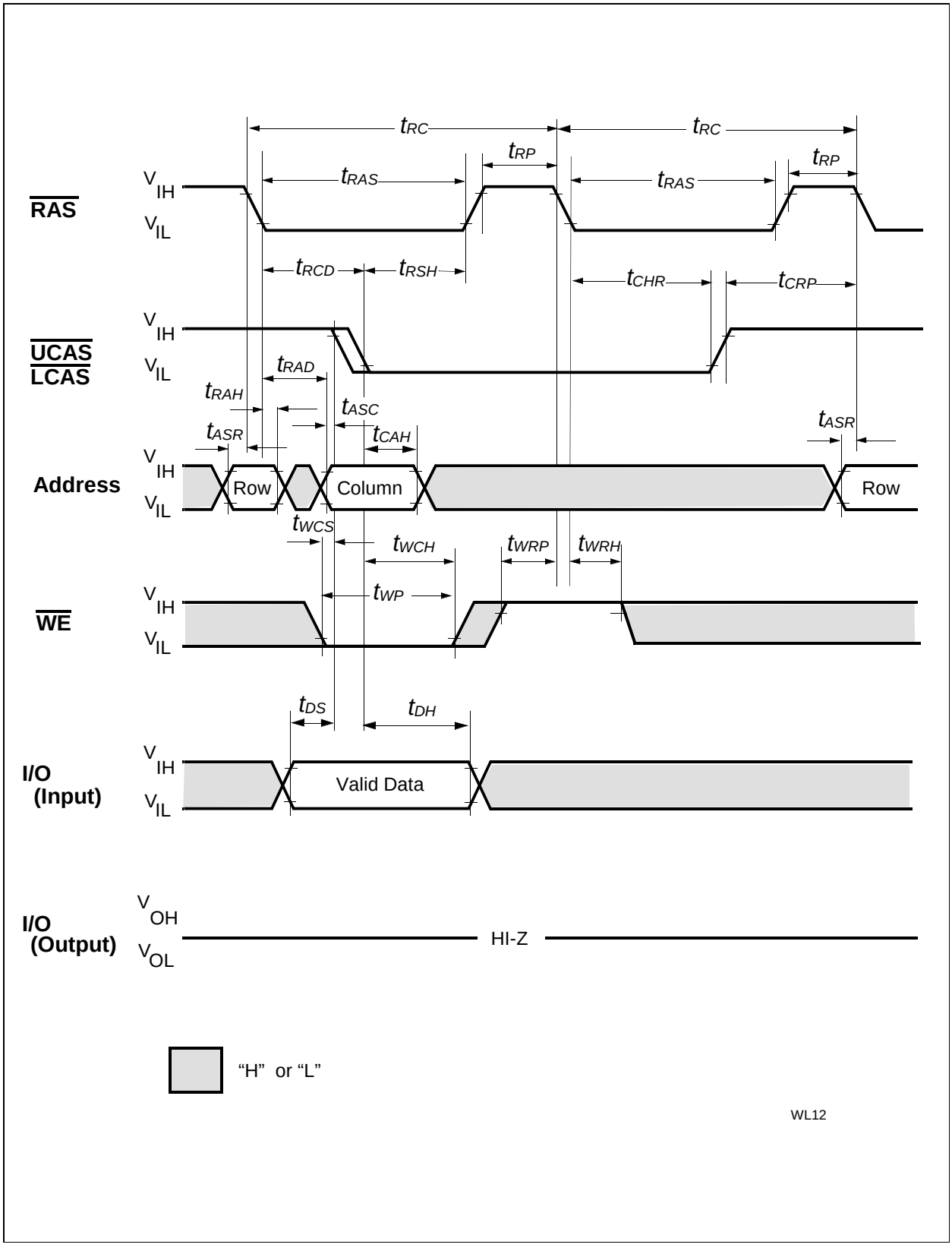
CAS-Before-RAS Refresh Cycle



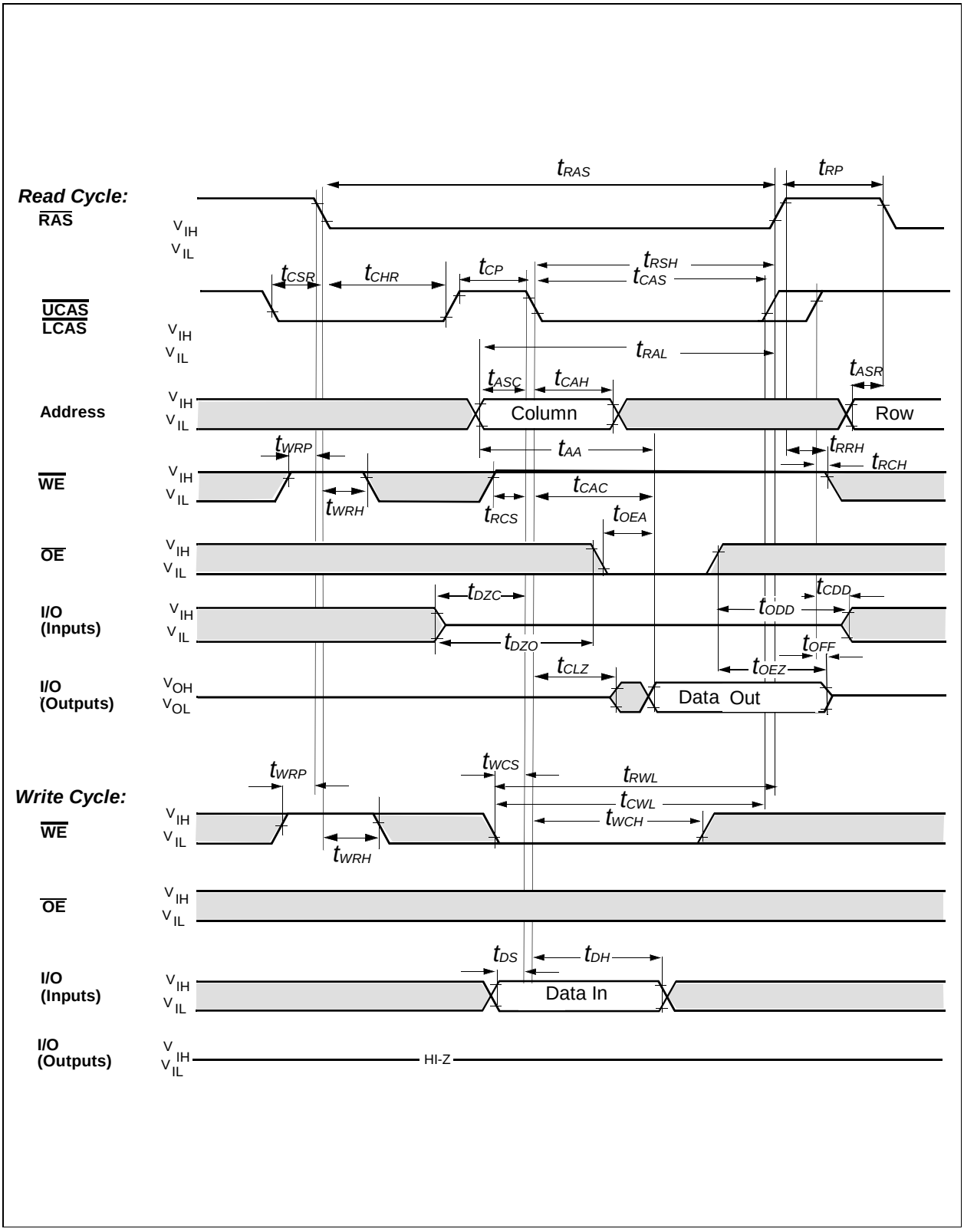
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self Refresh Cycle



Hidden Refresh Cycle (Read)

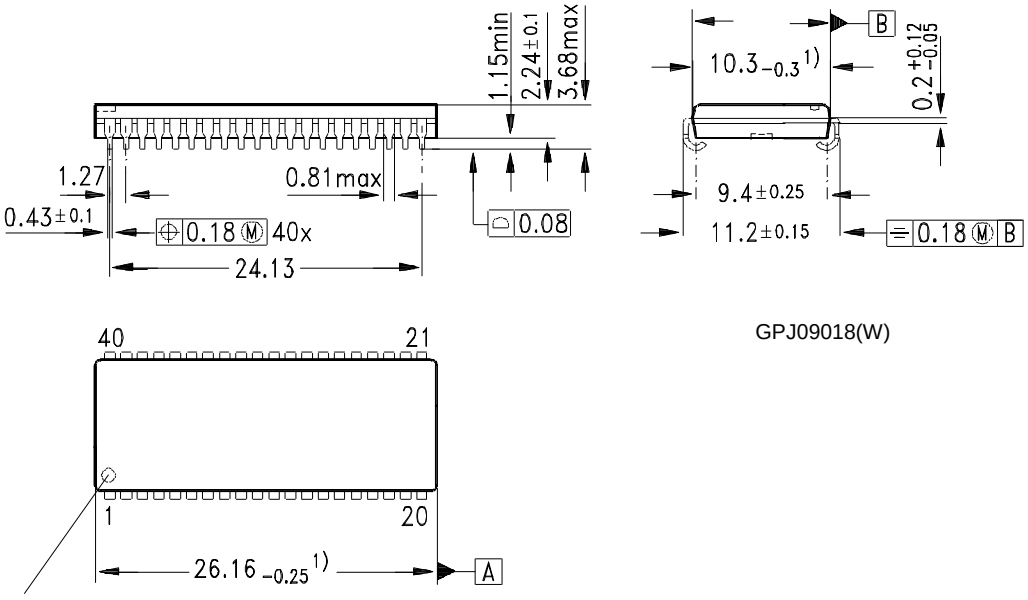


Hidden Refresh Cycle (Early Write)



CAS-Before-RAS Refresh Counter Test Cycle

Plastic Package, P-SOJ- 40-1 (SMD)
(Plastic small outline J-lead)



GPJ09018(W)

Index Marking

1) Does not include plastic or metal protrusions of 0.25 max per side

Dimensions in mm

Package Outline

REVISION CHANGES:

REV. 3.98	CMOS OUTPUT LEVELS REMOVED