16-bit Proprietary Microcontroller
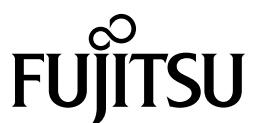
CMOS

F²MC-16FX MB96380 Series

MB96384*1/385*1
MB96F385*1/F386/F387/F388*1/F389*1

■ DESCRIPTION

MB96380 series is based on Fujitsu's advanced 16FX architecture (16-bit with instruction pipeline for RISC-like performance). The CPU uses the same instruction set as the established 16LX series enabling thus easy migration of 16LX Software to the new 16FX products. In comparison with the previous generation, the 16FX products include significantly improved performance even at the same operation frequency, a reduced power consumption and a faster start-up time.

For highest processing speed at optimized power consumption an internal PLL can be selected to supply the CPU with up to 56MHz operation frequency from an external 4MHz resonator. The result is a minimum instruction cycle time of 17.8ns going together with excellent EMI behavior. An on-chip clock modulation circuit significantly reduces emission peaks in the frequency spectrum. The emitted power is minimized by the on-chip voltage regulator that reduces the internal CPU voltage. A flexible clock tree allows to select suitable operation frequencies for peripheral resources independent of the CPU speed.

*1: These devices are under development. All information in this datasheet is preliminary for the devices under development.

FUJITSU

■ FEATURES

Feature	Description
Technology	• 0.18μm CMOS
CPU	• F2MC-16FX CPU • Up to 56 MHz internal, 17.8 ns instruction cycle time • Optimized instruction set for controller applications (bit, byte, word and long-word data types; 23 different addressing modes; barrel shift; variety of pointers) • 8-byte instruction execution queue • Signed multiply (16-bit × 16-bit) and divide (32-bit/16-bit) instructions available
System clock	• On-chip PLL clock multiplier (x1..25, x1 when PLL stop) • 3-16 MHz external quartz clock • Up to 56 MHz external clock for devices with fast clock input feature • 32-100 kHz subsystem quartz clock • 100kHz/2MHz internal RC clock for quick and safe startup, oscillator stop detection, watchdog • Clock source selectable from main- and subclock oscillator (part number suffix "W") and on-chip RC oscillator, independently for CPU and 2 clock domains of peripherals. • Low Power Consumption - 13 operating modes : (different Run, Sleep, Timer modes, Stop mode) • Clock modulator
On-chip voltage regulator	• Internal voltage regulator supports reduced internal MCU voltage, offering low EMI and low power consumption figures
Low voltage reset	• Reset is generated when supply voltage is below minimum.
Code Security	• Protects ROM content from unintended read-out
Memory Patch Function	• Replaces ROM content • Can also be used to implement embedded debug support
DMA	• Automatic transfer function independent of CPU, can be assigned freely to resources
Interrupts	• Fast Interrupt processing • 8 programmable priority levels • Non-Maskable Interrupt (NMI)
Timers	• Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer) • Watchdog Timer

Feature	Description
CAN	• Supports CAN protocol version 2.0 part A and B • ISO16845 certified • Bit rates up to 1 Mbit/s • 32 message objects • Each message object has its own identifier mask • Programmable FIFO mode (concatenation of message objects) • Maskable interrupt • Disabled Automatic Retransmission mode for Time Triggered CAN applications • Programmable loop-back mode for self-test operation
USART	• Full duplex USARTs (SCI/LIN) • Wide range of baud rate settings using a dedicated reload timer • Special synchronous options for adapting to different synchronous serial protocols • LIN functionality working either as master or slave LIN device
I2C	• Up to 400 kbit/s • Master and Slave functionality, 8-bit and 10-bit addressing
A/D converter	• SAR-type • 10-bit resolution • Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger or reload timer
A/D Converter Reference Voltage switch	• 2 independent positive A/D converter reference voltages available
Reload Timers	• 16-bit wide • Prescaler with $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$ of peripheral clock frequency • Event count function
Free Running Timers	• Signals an interrupt on overflow, supports timer clear upon match with Output Compare (0, 4), Prescaler with 1, $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$, $1/2^7$, $1/2^8$ of peripheral clock frequency
Input Capture Units	• 16-bit wide • Signals an interrupt upon external event • Rising edge, falling edge or rising & falling edge sensitive
Output Compare Units	• 16-bit wide • Signals an interrupt when a match with 16-bit I/O Timer occurs • A pair of compare registers can be used to generate an output signal.

Feature	Description
Programmable Pulse Generator	• 16-bit down counter, cycle and duty setting registers • Interrupt at trigger, counter borrow and/or duty match • PWM operation and one-shot operation • Internal prescaler allows 1, 1/4, 1/16, 1/64 of peripheral clock as counter clock and Reload timer overflow as clock input • Can be triggered by software or reload timer
Stepper Motor Control-ler	• Stepper Motor Controller with integrated high current output drivers • Four high current outputs for each channel • Two synchronized 8/10-bit PWMs per channel • Internal prescaling for PWM clock: 1, 1/4, 1/5, 1/6, 1/8, 1/10, 1/12, 1/16 of peripheral clock • Separate power supply for high current output drivers
LCD Controller	• LCD controller with up to 4 COM $\times$ 65 SEG • Internal or external voltage generation • Duty cycle: Selectable from options: 1/2, 1/3 and 1/4 • Fixed 1/3 bias • Programmable frame period • Clock source selectable from three options (peripheral clock, subclock or RC oscillator clock) • On-chip drivers for internal divider resistors or external divider resistors • On-chip data memory for display • LCD display can be operated in Timer Mode • Blank display: selectable • All SEG, COM and V pins can be switched between general and specialized purposes • External divided resistors can be also used to shut off the current when LCD is deactivated
Sound Generator	• 8-bit PWM signal is mixed with tone frequency from 16-bit reload counter • PWM clock by internal prescaler: 1, 1/2, 1/4, 1/8 of peripheral clock • Tone frequency: PWM frequency / 2 / (reload value + 1)
Real Time Clock	• Can be clocked either from sub oscillator (devices with part number suffix "W"), main oscillator or from the RC oscillator • Facility to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration) • Read/write accessible second/minute/hour registers • Can signal interrupts every half second/second/minute/hour/day • Internal clock divider and prescaler provide exact 1s clock

Feature	Description
External Interrupts	• Edge sensitive or level sensitive • Interrupt mask and pending bit per channel • Each available CAN channel RX has an external interrupt for wake-up • Selected USART channels SIN have an external interrupt for wake-up
Non Maskable Interrupt	• Disabled after reset • Once enabled, can not be disabled other than by reset. • Level high or level low sensitive • Pin shared with external interrupt 0.
External bus interface	• 8-bit or 16-bit bidirectional data • Up to 24-bit addresses • 6 chip select signals • Multiplexed address/data lines • Non-multiplexed address/data lines • Wait state request • External bus master possible • Timing programmable
Alarm comparators	• Monitors an external voltage and generates an interrupt in case of a voltage lower or higher than the defined thresholds • Threshold voltages defined externally or generated internally • Status is readable, interrupts can be masked separately
I/O Ports	• Virtually all external pins can be used as general purpose I/O • All push-pull outputs (except when used as I2C SDA/SCL line) • Bit-wise programmable as input/output or peripheral signal • Bit-wise programmable input enable • Bit-wise programmable input levels (Automotive / CMOS-Schmitt trigger / TTL) • Bit-wise programmable pull-up resistor • Bit-wise programmable output driving strength for EMI optimization
Package	• 120-pin plastic LQFP
Flash Memory	• Supports automatic programming, Embedded Algorithm[TM*1] • Write/Erase/Erase-Suspend/Resume commands • A flag indicating completion of the algorithm • Number of erase cycles: 10,000 times • Data retention time: 20 years • Erase can be performed on each sector individually • Sector protection • Flash Security feature to protect the content of the Flash • Low voltage detection during Flash erase

*1: Embedded Algorithm is a trade mark of Advanced Micro Devices Inc.

■ PRODUCT LINEUP
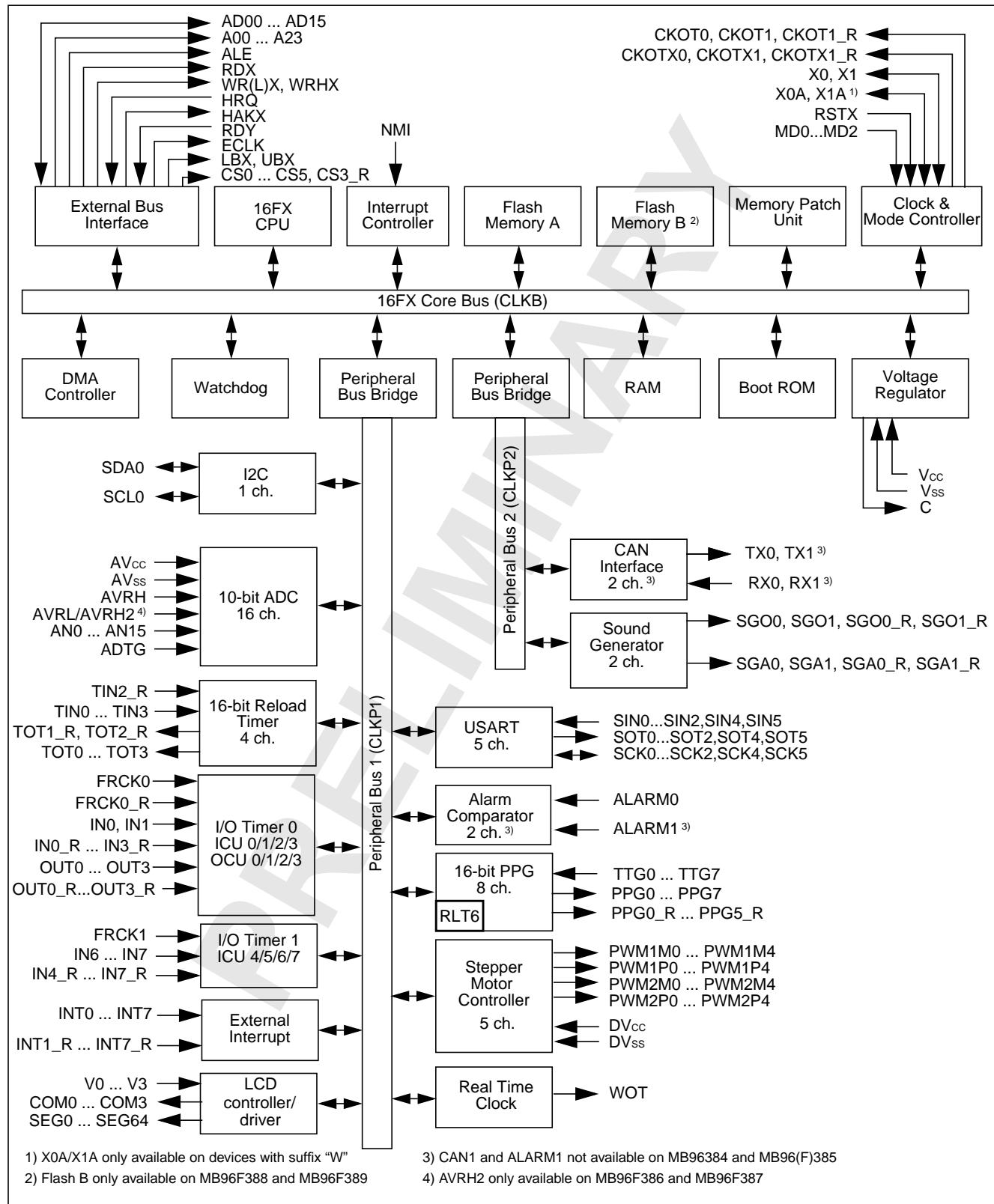
Features		MB96V300B	MB9638x
Product type		Evaluation sample	Flash product: MB96F38x Mask ROM product: MB9638x
Product options			
YS			LVD persistently on / Single clock devices
RS			LVD can be disabled / Single clock devices
YW		NA	LVD persistently on / Dual clock devices
RW			LVD can be disabled / Dual clock devices
TS			32kB Data Flash / LVD persistently on / Single clock devices
HS			32kB Data Flash / LVD can be disabled / Single clock devices
TW			32kB Data Flash / LVD persistently on / Dual clock devices
HW			32kB Data Flash / LVD can be disabled / Dual clock devices
Flash/ROM	RAM		
128kB	6kB		MB96384Y[1], MB96384R[1]
160kB	8kB		MB96385Y[1], MB96385R[1], MB96F385Y[1], MB96F385R[1]
288kB	16kB	ROM/Flash memory emulation by external RAM, 92kB internal RAM	MB96F386Y, MB96F386R
416kB	16kB		MB96F387Y, MB96F387R
576kB [Flash A: 544kB, Flash B (Data Flash): 32kB]	28kB		MB96F388T[1], MB96F388H[1]
832kB [Flash A: 544kB, Flash B: 288kB]	32kB		MB96F389Y[1], MB96F389R[1],
Package		BGA416	FPT-120P-M21
DMA		16 channels	7 channels
USART		10 channels	5 channels
I2C		2 channels	1 channel
A/D Converter		40 channels	16 channels
A/D Converter Reference Voltage switch		yes	Only for MB96F386Y, MB96F386R, MB96F387Y, MB96F387R
16-bit Reload Timer		6 channels + 1 channel (for PPG)	4 channels + 1 channel (for PPG)
16-bit Free-Running Timer		4 channels	2 channels
16-bit Output Compare		12 channels	4 channels

Features	MB96V300B	MB9638x
16-bit Input Capture	12 channels	8 channels
16-bit Programmable Pulse Generator	20 channels	8 channels
CAN Interface	5 channels	2 channels MB96384Y[1], MB96384R[1], MB96(F)385Y[1], MB96(F)385R[1],: 1 channel
Stepping Motor Controller	6 channels	5 channels
External Interrupts	16 channels	8 channels
Non-Maskable Interrupt	1 channel	
Sound generator	2 channels	2 channels
LCD Controller	4 COM x 72 SEG	4 COM x 65 SEG
Real Time Clock	1	
I/O Ports	136	94 for part number with suffix "W", 96 for part number with suffix "S"
Alarm comparator	2 channels	2 channels MB96384Y[1], MB96384R[1], MB96(F)385Y[1], MB96(F)385R[1],: 1 channel
External bus interface	Yes	
Chip select	6 signals	
Clock output function	2 channels	
Low voltage reset	Yes	
On-chip RC-oscillator	Yes	

*1: These devices are under development. All information in this datasheet is preliminary for the devices under development.

■ BLOCK DIAGRAMS
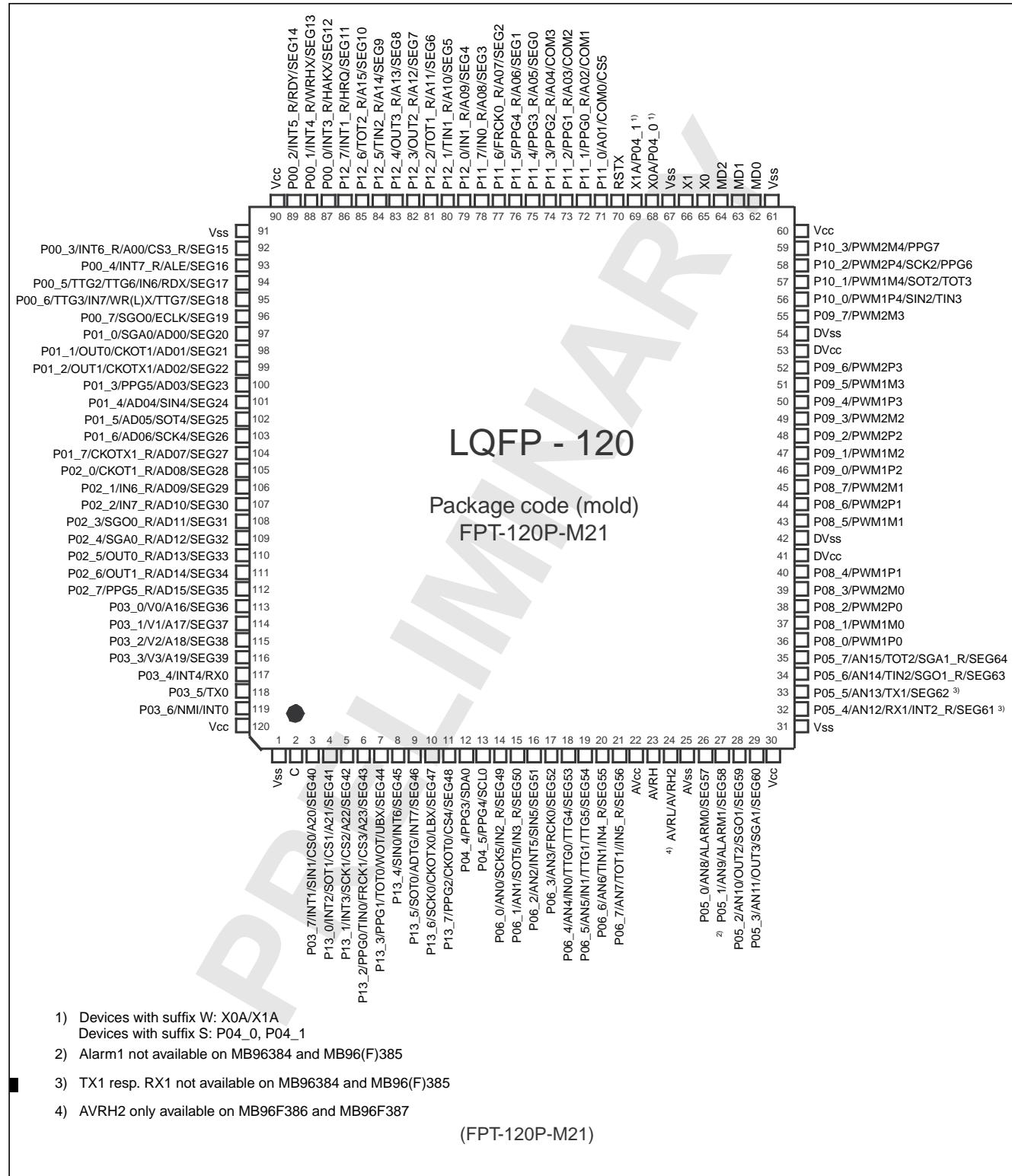
Block diagram of MB96(F)38x

1) X0A/X1A only available on devices with suffix "W"
2) Flash B only available on MB96F388 and MB96F389
3) CAN1 and ALARM1 not available on MB96384 and MB96(F)385
4) AVRH2 only available on MB96F386 and MB96F387

■ PIN ASSIGNMENTS

Pin assignment of MB96(F)38x

LQFP - 120

Package code (mold)
FPT-120P-M21

1) Devices with suffix W: X0A/X1A
   Devices with suffix S: P04_0, P04_1

2) Alarm1 not available on MB96384 and MB96(F)385

3) TX1 resp. RX1 not available on MB96384 and MB96(F)385

4) AVRH2 only available on MB96F386 and MB96F387

(FPT-120P-M21)

PRELIMINARY

■ PIN FUNCTION DESCRIPTION

Pin Function description (1 / 3)

Pin name	Feature	Description
ADn	External bus	External bus interface (non multiplexed mode) data input/output. External bus interface (multiplexed mode) address output and data input/output
ADTG	ADC	A/D converter trigger input
ALARMn	Alarm comparator	Alarm Comparator n input
ALE	External bus	External bus Address Latch Enable output
An	External bus	External bus non-multiplexed address output
ANn	ADC	A/D converter channel n input
AV$_{CC}$	Supply	Analog circuits power supply
AVRH	ADC	A/D converter high reference voltage input
AVRH2	ADC	Alternative A/D converter high reference voltage input
AVRL	ADC	A/D converter low reference voltage input
AV$_{SS}$	Supply	Analog circuits power supply
C	Voltage regulator	Internally regulated power supply stabilization capacitor pin
CKOTn	Clock output function	Clock Output function n output
CKOTn_R	Clock output function	Relocated Clock Output function n output
CKOTXn	Clock output function	Clock Output function n inverted output
CKOTXn_R	Clock output function	Relocated Clock Output function n inverted output
COMn	LCD	LCD COM pins
ECLK	External bus	External bus clock output
CSn	External bus	External bus chip select n output
CSn_R	External bus	Relocated External bus chip select n output
DV$_{CC}$	Supply	SMC pins power supply
FRCKn	Free Running Timer	Free Running Timer n input
FRCKn_R	Free Running Timer	Relocated Free Running Timer n input
HAKX	External bus	External bus Hold Acknowledge
HRQ	External bus	External bus Hold Request
INn	ICU	Input Capture Unit n input
INn_R	ICU	Relocated Input Capture Unit n input
INTn	External Interrupt	External Interrupt n input

Pin Function description (2 / 3)

Pin name	Feature	Description
INTn_R	External Interrupt	Relocated External Interrupt n input
LBX	External bus	External Bus Interface Lower Byte select strobe output
MDn	Core	Input pins for specifying the operating mode.
NMI	External Interrupt	Non-Maskable Interrupt input
OUTn	OCU	Output Compare Unit n waveform output
OUTn_R	OCU	Relocated Output Compare Unit n waveform output
Pxx_n	GPIO	General purpose IO
PPGn	PPG	Programmable Pulse Generator n output
PPGn_R	PPG	Relocated Programmable Pulse Generator n output
PWMn	SMC	SMC PWM high current
RDX	External bus	External bus interface read strobe output
RDY	External bus	External bus interface external wait state request input
RSTX	Core	Reset input
RXn	CAN	CAN interface n RX input
SCKn	USART	USART n serial clock input/output
SCLn	I2C	I2C interface n clock I/O input/output
SDAn	I2C	I2C interface n serial data I/O input/output
SEGn	LCD	LCD segment n
SGA	Sound Generator	SG amplitude output
SGO	Sound Generator	SG sound/tone output
SGA_R	Sound Generator	Relocated SG amplitude output
SGO_R	Sound Generator	Relocated SG sound/tone output
SINn	USART	USART n serial data input
SOTn	USART	USART n serial data output
TINn	Reload Timer	Reload Timer n event input
TINn_R	Reload Timer	Relocated Reload Timer n event input
TOTn	Reload Timer	Reload Timer n output
TOTn_R	Reload Timer	Relocated Reload Timer n output
TTGn	PPG	Programmable Pulse Generator n trigger input
TXn	CAN	CAN interface n TX output

Pin Function description (3 / 3)

Pin name	Feature	Description
UBX	External bus	External Bus Interface Upper Byte select strobe output
Vn	LCD	LCD voltage references
V_{CC}	Supply	Power supply
V_{SS}	Supply	Power supply
WOT	RTC	Real Timer clock output
WRHX	External bus	External bus High byte write strobe output
WRLX/WRX	External bus	External bus Low byte / Word write strobe output
X0	Clock	Oscillator input
X0A	Clock	Subclock Oscillator input (only for devices with suffix "W")
X1	Clock	Oscillator output
X1A	Clock	Subclock Oscillator output (only for devices with suffix "W")

■ PIN CIRCUIT TYPE

FPT-120P-M21	
Pin no.	Circuit type
1	Supply
2	F
3 to 11	J
12,13	N
14 to 21	K
22	Supply
23 to 24	G
25	Supply
26 to 29	K
30,31	Supply
32 to 35	K
36 to 40	M
41,42	Supply
43 to 52	M
53,54	Supply
55 to 59	M
60, 61	Supply
62 to 64	C
65, 66	A
67	Supply
68,69	B[1]
68,69	H[2]
70	E
71 to 89	J
90 to 91	Supply

[1] Devices with suffix "W"
[2] Devices without suffix "W"

FPT-120P-M21	
Pin no.	Circuit type
92 to 112	J
113 to 116	L
117 to 119	H
120	Supply
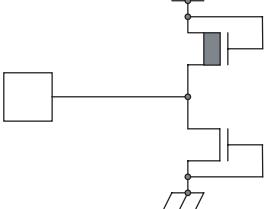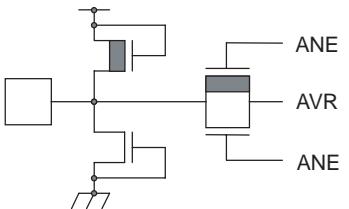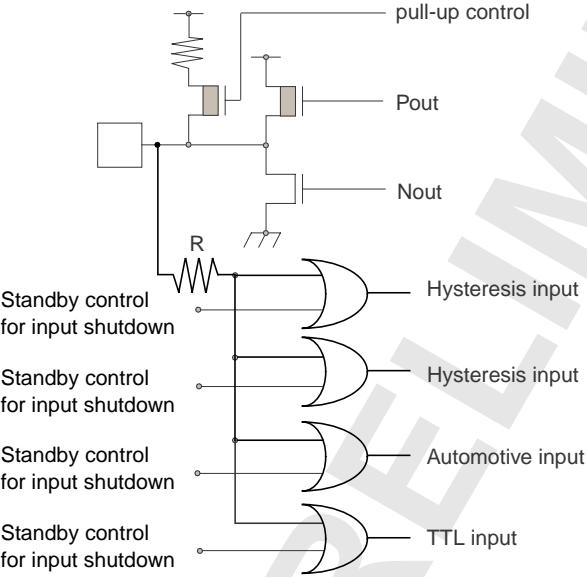
[1] Devices with suffix "W"

[2] Devices without suffix "W"
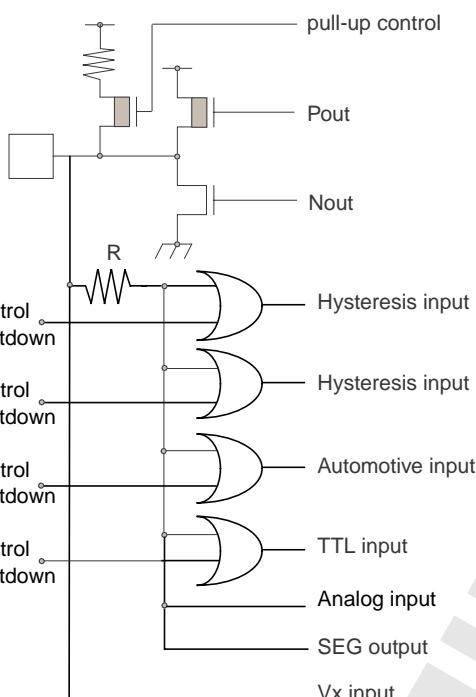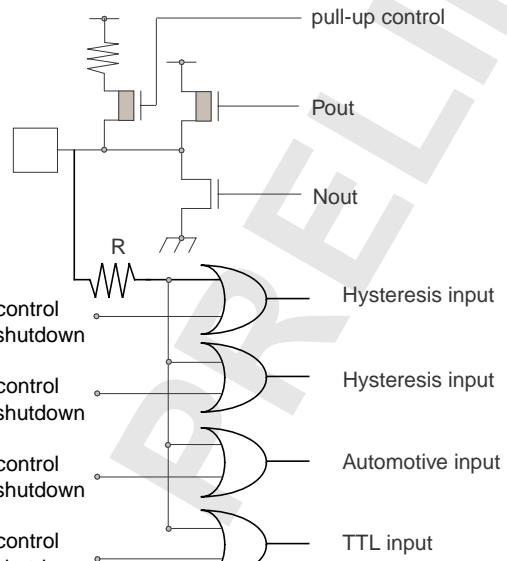
■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		High-speed oscillation circuit: • Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) • Programmable feedback resistor = approx. 2 * 0.5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode
B		Low-speed oscillation circuit: • Programmable feedback resistor = approx. 2 * 5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled
C		• Mask ROM and EVA device: CMOS Hysteresis input pin • Flash device: CMOS input pin
E		• CMOS Hysteresis input pin • Pull-up resistor value: approx. 50 kΩ

Type	Circuit	Remarks
F		• Power supply input protection circuit
G	ANE / AVR / ANE	• A/D converter ref+ (AVRH/AVRH2) power supply input pin with protection circuit • Flash devices do not have a protection circuit against VCC for pins AVRH/AVRH2 • Devices without AVRH reference switch do not have an analog switch for the AVRL pin
H	pull-up control / Pout / Nout / R / Standby control for input shutdown — Hysteresis input / Standby control for input shutdown — Hysteresis input / Standby control for input shutdown — Automotive input / Standby control for input shutdown — TTL input	• CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) • 2 different CMOS hysteresis inputs with input shutdown function • Automotive input with input shutdown function • TTL input with input shutdown function • Programmable pull-up resistor: 50kΩ approx.

Type	Circuit	Remarks
J	pull-up control Pout Nout R Standby control for input shutdown — Hysteresis input Standby control for input shutdown — Hysteresis input Standby control for input shutdown — Automotive input Standby control for input shutdown — TTL input SEG, COM output	• CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) • 2 different CMOS hysteresis inputs with input shutdown function • Automotive input with input shutdown function • TTL input with input shutdown function • Programmable pull-up resistor: 50kΩ approx. • SEG or COM output
K	pull-up control Pout Nout R Standby control for input shutdown — Hysteresis input Standby control for input shutdown — Hysteresis input Standby control for input shutdown — Automotive input Standby control for input shutdown — TTL input Analog input SEG output	• CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) • 2 different CMOS hysteresis inputs with input shutdown function • Automotive input with input shutdown function • TTL input with input shutdown function. • Programmable pull-up resistor: 50kΩ approx. • Analog input • SEG output

Type	Circuit	Remarks
L		• CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) • 2 different CMOS hysteresis inputs with input shutdown function • Automotive input with input shutdown function • TTL input with input shutdown function • Programmable pull-up resistor: 50kΩ approx. • Analog input • Vx input • SEG output
M		• CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA, I_{OL} = 30mA, I_{OH} = -30mA) • 2 different CMOS hysteresis inputs with input shutdown function • Automotive input with input shutdown function • TTL input with input shutdown function • Programmable pull-up resistor: 50kΩ approx.

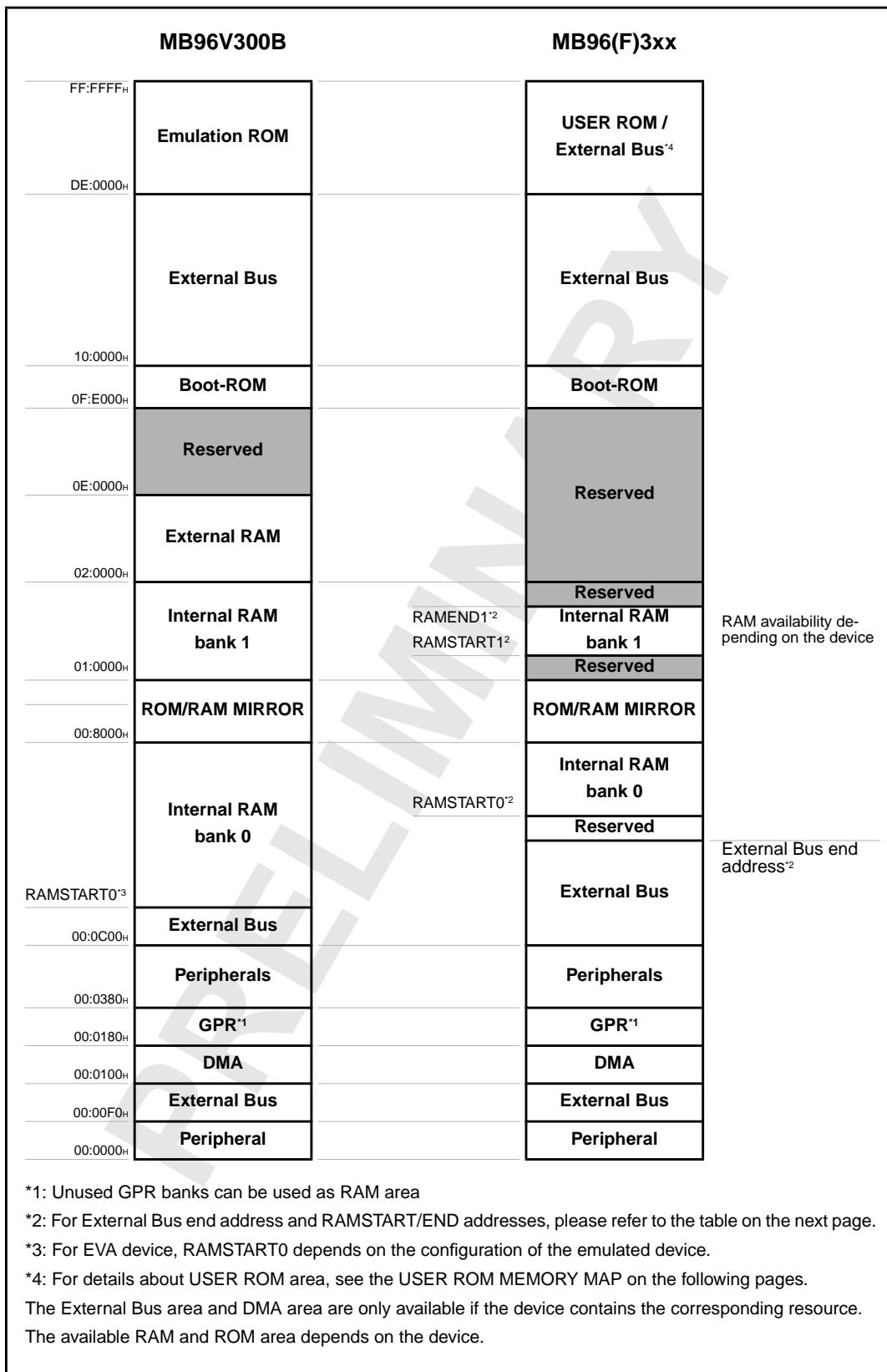| Type	Circuit	Remarks
N		• CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) • 2 different CMOS hysteresis inputs with input shutdown function • Automotive input with input shutdown function • TTL input with input shutdown function • Programmable pull-up resistor: 50kΩ approx.

■ MEMORY MAP

MB96V300B		MB96(F)3xx
Emulation ROM (FF:FFFFH – DE:0000H)		**USER ROM / External Bus**[4]
External Bus (DE:0000H – 10:0000H)		**External Bus**
Boot-ROM (0F:E000H)		**Boot-ROM**
Reserved (0E:0000H)		**Reserved**
External RAM (02:0000H)		
		Reserved
Internal RAM bank 1 (01:0000H)	RAMEND1[2] RAMSTART1[2]	**Internal RAM bank 1** — RAM availability depending on the device
		Reserved
ROM/RAM MIRROR (00:8000H)		**ROM/RAM MIRROR**
Internal RAM bank 0		**Internal RAM bank 0**
	RAMSTART0[2]	**Reserved**
RAMSTART0[3]		**External Bus** — External Bus end address[2]
External Bus (00:0C00H)		
Peripherals (00:0380H)		**Peripherals**
GPR[1] (00:0180H)		**GPR**[1]
DMA (00:0100H)		**DMA**
External Bus (00:00F0H)		**External Bus**
Peripheral (00:0000H)		**Peripheral**

*1: Unused GPR banks can be used as RAM area

*2: For External Bus end address and RAMSTART/END addresses, please refer to the table on the next page.

*3: For EVA device, RAMSTART0 depends on the configuration of the emulated device.

*4: For details about USER ROM area, see the USER ROM MEMORY MAP on the following pages.

The External Bus area and DMA area are only available if the device contains the corresponding resource.

The available RAM and ROM area depends on the device.

■ RAMSTART/END AND EXTERNAL BUS END ADDRESSES

Devices	Bank 0 RAM size	Bank 1 RAM size	External Bus end address	RAMSTART0	RAMSTART1	RAMEND1
MB96384	6kB	-	00:61FF$_H$	00:6A40$_H$	-	-
MB96385/F385	8kB	-	00:61FF$_H$	00:6240$_H$	-	-
MB96F386, MB96F387	16kB	-	00:41FF$_H$	00:4240$_H$	-	-
MB96F388	28kB	-	00:11FF$_H$	00:1240$_H$	-	-
MB96F389	28kB	4kB	00:11FF$_H$	00:1240$_H$	01:8000$_H$	01:8FFF$_H$

■ USER ROM MEMORY MAP FOR FLASH DEVICES
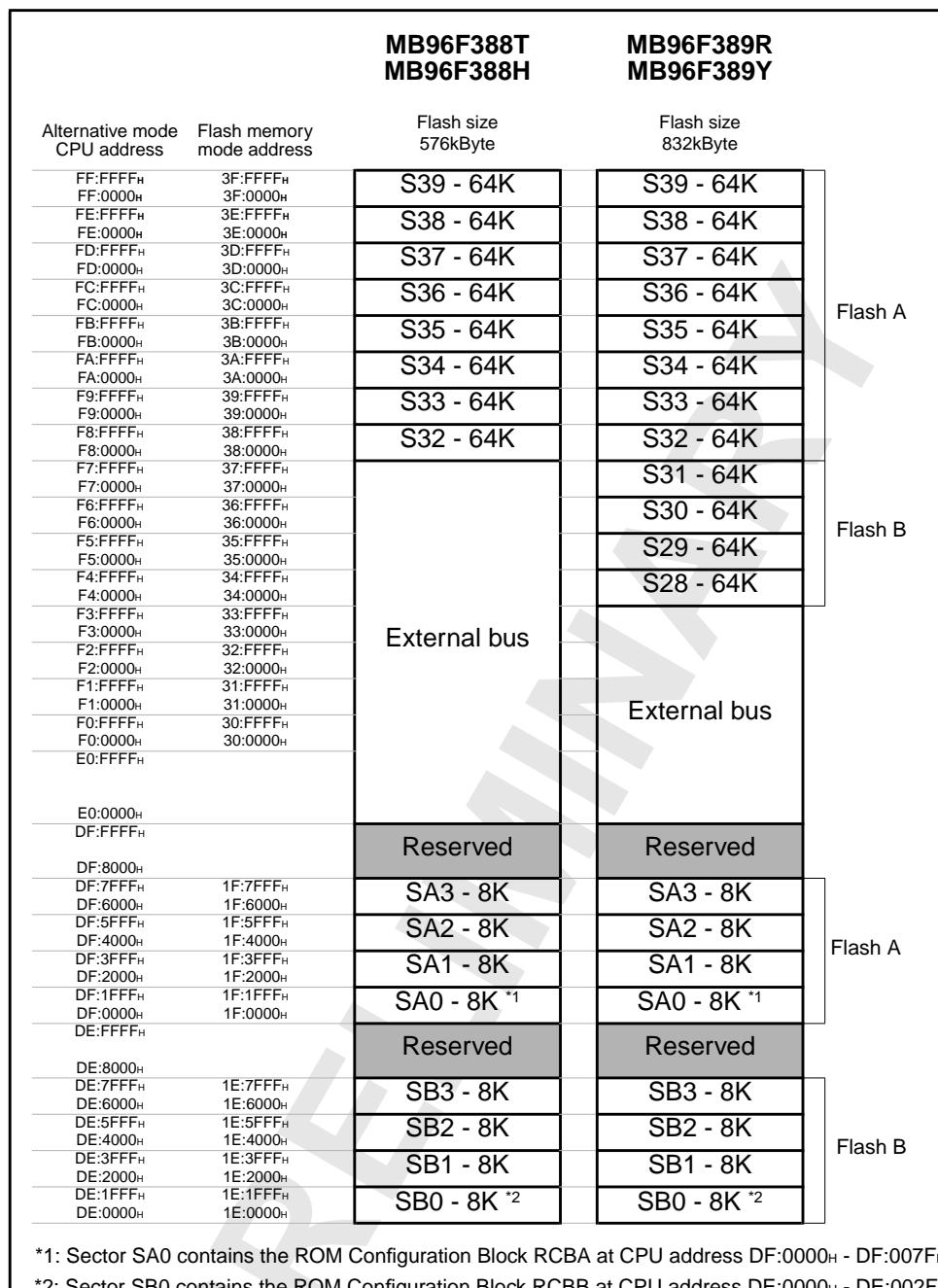
Alternative mode CPU address	Flash memory mode address	MB96F385R MB96F385Y Flash size 160kByte	MB96F386R MB96F386Y Flash size 288kByte	MB96F387R MB96F387Y Flash size 416kByte	
FF:FFFFH FF:0000H	3F:FFFFH 3F:0000H	S39 - 64K	S39 - 64K	S39 - 64K	Flash A
FE:FFFFH FE:0000H	3E:FFFFH 3E:0000H	S38 - 64K	S38 - 64K	S38 - 64K	
FD:FFFFH FD:0000H	3D:FFFFH 3D:0000H		S37 - 64K	S37 - 64K	
FC:FFFFH FC:0000H	3C:FFFFH 3C:0000H		S36 - 64K	S36 - 64K	
FB:FFFFH FB:0000H	3B:FFFFH 3B:0000H			S35 - 64K	
FA:FFFFH FA:0000H	3A:FFFFH 3A:0000H			S34 - 64K	
F9:FFFFH F9:0000H	39:FFFFH 39:0000H				
F8:FFFFH F8:0000H	38:FFFFH 38:0000H				
F7:FFFFH F7:0000H	37:FFFFH 37:0000H				
F6:FFFFH F6:0000H	36:FFFFH 36:0000H	External bus			
F5:FFFFH F5:0000H	35:FFFFH 35:0000H				
F4:FFFFH F4:0000H	34:FFFFH 34:0000H		External bus		
F3:FFFFH F3:0000H	33:FFFFH 33:0000H			External bus	
F2:FFFFH F2:0000H	32:FFFFH 32:0000H				
F1:FFFFH F1:0000H	31:FFFFH 31:0000H				
F0:FFFFH F0:0000H	30:FFFFH 30:0000H				
E0:FFFFH E0:0000H					
DF:FFFFH DF:8000H		Reserved	Reserved	Reserved	
DF:7FFFH DF:6000H	1F:7FFFH 1F:6000H	SA3 - 8K	SA3 - 8K	SA3 - 8K	Flash A
DF:5FFFH DF:4000H	1F:5FFFH 1F:4000H	SA2 - 8K	SA2 - 8K	SA2 - 8K	
DF:3FFFH DF:2000H	1F:3FFFH 1F:2000H	SA1 - 8K	SA1 - 8K	SA1 - 8K	
DF:1FFFH DF:0000H	1F:1FFFH 1F:0000H	SA0 - 8K [1]	SA0 - 8K [1]	SA0 - 8K [1]	
DE:FFFFH DE:0000H		Reserved	Reserved	Reserved	

[1]: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000H - DF:007FH

Alternative mode CPU address	Flash memory mode address	MB96F388T MB96F388H Flash size 576kByte	MB96F389R MB96F389Y Flash size 832kByte	
FF:FFFF$_H$ FF:0000$_H$	3F:FFFF$_H$ 3F:0000$_H$	S39 - 64K	S39 - 64K	
FE:FFFF$_H$ FE:0000$_H$	3E:FFFF$_H$ 3E:0000$_H$	S38 - 64K	S38 - 64K	
FD:FFFF$_H$ FD:0000$_H$	3D:FFFF$_H$ 3D:0000$_H$	S37 - 64K	S37 - 64K	
FC:FFFF$_H$ FC:0000$_H$	3C:FFFF$_H$ 3C:0000$_H$	S36 - 64K	S36 - 64K	Flash A
FB:FFFF$_H$ FB:0000$_H$	3B:FFFF$_H$ 3B:0000$_H$	S35 - 64K	S35 - 64K	
FA:FFFF$_H$ FA:0000$_H$	3A:FFFF$_H$ 3A:0000$_H$	S34 - 64K	S34 - 64K	
F9:FFFF$_H$ F9:0000$_H$	39:FFFF$_H$ 39:0000$_H$	S33 - 64K	S33 - 64K	
F8:FFFF$_H$ F8:0000$_H$	38:FFFF$_H$ 38:0000$_H$	S32 - 64K	S32 - 64K	
F7:FFFF$_H$ F7:0000$_H$	37:FFFF$_H$ 37:0000$_H$		S31 - 64K	
F6:FFFF$_H$ F6:0000$_H$	36:FFFF$_H$ 36:0000$_H$		S30 - 64K	Flash B
F5:FFFF$_H$ F5:0000$_H$	35:FFFF$_H$ 35:0000$_H$		S29 - 64K	
F4:FFFF$_H$ F4:0000$_H$	34:FFFF$_H$ 34:0000$_H$		S28 - 64K	
F3:FFFF$_H$ F3:0000$_H$	33:FFFF$_H$ 33:0000$_H$	External bus		
F2:FFFF$_H$ F2:0000$_H$	32:FFFF$_H$ 32:0000$_H$			
F1:FFFF$_H$ F1:0000$_H$	31:FFFF$_H$ 31:0000$_H$		External bus	
F0:FFFF$_H$ F0:0000$_H$	30:FFFF$_H$ 30:0000$_H$			
E0:FFFF$_H$ E0:0000$_H$				
DF:FFFF$_H$ DF:8000$_H$		Reserved	Reserved	
DF:7FFF$_H$ DF:6000$_H$	1F:7FFF$_H$ 1F:6000$_H$	SA3 - 8K	SA3 - 8K	
DF:5FFF$_H$ DF:4000$_H$	1F:5FFF$_H$ 1F:4000$_H$	SA2 - 8K	SA2 - 8K	Flash A
DF:3FFF$_H$ DF:2000$_H$	1F:3FFF$_H$ 1F:2000$_H$	SA1 - 8K	SA1 - 8K	
DF:1FFF$_H$ DF:0000$_H$	1F:1FFF$_H$ 1F:0000$_H$	SA0 - 8K [*1]	SA0 - 8K [*1]	
DE:FFFF$_H$ DE:8000$_H$		Reserved	Reserved	
DE:7FFF$_H$ DE:6000$_H$	1E:7FFF$_H$ 1E:6000$_H$	SB3 - 8K	SB3 - 8K	
DE:5FFF$_H$ DE:4000$_H$	1E:5FFF$_H$ 1E:4000$_H$	SB2 - 8K	SB2 - 8K	Flash B
DE:3FFF$_H$ DE:2000$_H$	1E:3FFF$_H$ 1E:2000$_H$	SB1 - 8K	SB1 - 8K	
DE:1FFF$_H$ DE:0000$_H$	1E:1FFF$_H$ 1E:0000$_H$	SB0 - 8K [*2]	SB0 - 8K [*2]	

*1: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000$_H$ - DF:007F$_H$

*2: Sector SB0 contains the ROM Configuration Block RCBB at CPU address DE:0000$_H$ - DE:002F$_H$

■ **USER ROM MEMORY MAP FOR MASK ROM DEVICES**

	MB96384	MB96385
CPU address	ROM size 128kByte	ROM size 160kByte
FF:FFFFH		
FF:0000H	128K ROM	128K ROM
FE:FFFFH		
FE:0000H		
FD:FFFFH	External bus	External bus
E0:0000H		
DF:FFFFH		Reserved
DF:8000H	Reserved	
DF:7FFFH		32K ROM
DF:0080H		
DF:007FH	ROM configuration block RCB	ROM configuration block RCB
DF:0000H		
DE:FFFFH	Reserved	Reserved
DE:0000H		

■ **SERIAL PROGRAMMING COMMUNICATION INTERFACE**

USART pins for Flash serial programming (MD[2:0] = 010, Serial Communication mode)

MB96F38x		
Pin number	USART Number	Normal function
LQFP-120		
8	USART0	SIN0
9		SOT0
10		SCK0
3	USART1	SIN1
4		SOT1
5		SCK1
56	USART2	SIN2
57		SOT2
58		SCK2

Note: For handshaking pin, please use for these devices the default port P00_1 on pin 88. If any other pin is required, please contact the Flash programmer device vendor.

■ I/O MAP

I/O map MB96(F)38x (1 / 31)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000000H	I/O Port P00 - Port Data Register	PDR00		RW
000001H	I/O Port P01 - Port Data Register	PDR01		RW
000002H	I/O Port P02 - Port Data Register	PDR02		RW
000003H	I/O Port P03 - Port Data Register	PDR03		RW
000004H	I/O Port P04 - Port Data Register	PDR04		RW
000005H	I/O Port P05 - Port Data Register	PDR05		RW
000006H	I/O Port P06 - Port Data Register	PDR06		RW
000007H	Reserved			-
000008H	I/O Port P08 - Port Data Register	PDR08		RW
000009H	I/O Port P09 - Port Data Register	PDR09		RW
00000AH	I/O Port P10 - Port Data Register	PDR10		RW
00000BH	I/O Port P11 - Port Data Register	PDR11		RW
00000CH	I/O Port P12 - Port Data Register	PDR12		RW
00000DH	I/O Port P13 - Port Data Register	PDR13		RW
00000EH-000017H	Reserved			-
000018H	ADC0 - Control Status register Low	ADCSL	ADCS	RW
000019H	ADC0 - Control Status register High	ADCSH		RW
00001AH	ADC0 - Data Register Low	ADCRL	ADCR	R
00001BH	ADC0 - Data Register High	ADCRH		R
00001CH	ADC0 - Setting Register		ADSR	RW
00001DH	ADC0 - Setting Register			RW
00001EH	ADC0 - Extended Configuration Register	ADECR		RW
00001FH	Reserved			-
000020H	FRT0 - Data register of free-running timer		TCDT0	RW
000021H	FRT0 - Data register of free-running timer			RW
000022H	FRT0 - Control status register of free-running timer Low	TCCSL0	TCCS0	RW
000023H	FRT0 - Control status register of free-running timer High	TCCSH0		RW

I/O map MB96(F)38x (2 / 31)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000024H	FRT1 - Data register of free-running timer		TCDT1	RW
000025H	FRT1 - Data register of free-running timer			RW
000026H	FRT1 - Control status register of free-running timer Low	TCCSL1	TCCS1	RW
000027H	FRT1 - Control status register of free-running timer High	TCCSH1		RW
000028H	OCU0 - Output Compare Control Status	OCS0		RW
000029H	OCU1 - Output Compare Control Status	OCS1		RW
00002AH	OCU0 - Compare Register		OCCP0	RW
00002BH	OCU0 - Compare Register			RW
00002CH	OCU1 - Compare Register		OCCP1	RW
00002DH	OCU1 - Compare Register			RW
00002EH	OCU2 - Output Compare Control Status	OCS2		RW
00002FH	OCU3 - Output Compare Control Status	OCS3		RW
000030H	OCU2 - Compare Register		OCCP2	RW
000031H	OCU2 - Compare Register			RW
000032H	OCU3 - Compare Register		OCCP3	RW
000033H	OCU3 - Compare Register			RW
000034H-00003FH	Reserved			-
000040H	ICU0/ICU1 - Control Status Register	ICS01		RW
000041H	ICU0/ICU1 - Edge register	ICE01		RW
000042H	ICU0 - Capture Register Low	IPCPL0	IPCP0	R
000043H	ICU0 - Capture Register High	IPCPH0		R
000044H	ICU1 - Capture Register Low	IPCPL1	IPCP1	R
000045H	ICU1 - Capture Register High	IPCPH1		R
000046H	ICU2/ICU3 - Control Status Register	ICS23		RW
000047H	ICU2/ICU3 - Edge register	ICE23		RW
000048H	ICU2 - Capture Register Low	IPCPL2	IPCP2	R
000049H	ICU2 - Capture Register High	IPCPH2		R
00004AH	ICU3 - Capture Register Low	IPCPL3	IPCP3	R

I/O map MB96(F)38x (3 / 31)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00004BH	ICU3 - Capture Register High	IPCPH3		R
00004CH	ICU4/ICU5 - Control Status Register	ICS45		RW
00004DH	ICU4/ICU5 - Edge register	ICE45		RW
00004EH	ICU4 - Capture Register Low	IPCPL4	IPCP4	R
00004FH	ICU4 - Capture Register High	IPCPH4		R
000050H	ICU5 - Capture Register Low	IPCPL5	IPCP5	R
000051H	ICU5 - Capture Register High	IPCPH5		R
000052H	ICU6/ICU7 - Control Status Register	ICS67		RW
000053H	ICU6/ICU7 - Edge register	ICE67		RW
000054H	ICU6 - Capture Register Low	IPCPL6	IPCP6	R
000055H	ICU6 - Capture Register High	IPCPH6		R
000056H	ICU7 - Capture Register Low	IPCPL7	IPCP7	R
000057H	ICU7 - Capture Register High	IPCPH7		R
000058H	EXTINT0 - External Interrupt Enable Register	ENIR0		RW
000059H	EXTINT0 - External Interrupt Interrupt request Register	EIRR0		RW
00005AH	EXTINT0 - External Interrupt Level Select Low	ELVRL0	ELVR0	RW
00005BH	EXTINT0 - External Interrupt Level Select High	ELVRH0		RW
00005CH-00005FH	Reserved			-
000060H	RLT0 - Timer Control Status Register Low	TMCSRL0	TMCSR0	RW
000061H	RLT0 - Timer Control Status Register High	TMCSRH0		RW
000062H	RLT0 - Reload Register - for writing		TMRLR0	W
000062H	RLT0 - Reload Register - for reading		TMR0	R
000063H	RLT0 - Reload Register - for writing			W
000063H	RLT0 - Reload Register - for reading			R
000064H	RLT1 - Timer Control Status Register Low	TMCSRL1	TMCSR1	RW
000065H	RLT1 - Timer Control Status Register High	TMCSRH1		RW
000066H	RLT1 - Reload Register - for writing		TMRLR1	W
000066H	RLT1 - Reload Register - for reading		TMR1	R
000067H	RLT1 - Reload Register - for writing			W

I/O map MB96(F)38x (4 / 31)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000067H	RLT1 - Reload Register - for reading			R
000068H	RLT2 - Timer Control Status Register Low	TMCSRL2	TMCSR2	RW
000069H	RLT2 - Timer Control Status Register High	TMCSRH2		RW
00006AH	RLT2 - Reload Register - for writing		TMRLR2	W
00006AH	RLT2 - Reload Register - for reading		TMR2	R
00006BH	RLT2 - Reload Register - for writing			W
00006BH	RLT2 - Reload Register - for reading			R
00006CH	RLT3 - Timer Control Status Register Low	TMCSRL3	TMCSR3	RW
00006DH	RLT3 - Timer Control Status Register High	TMCSRH3		RW
00006EH	RLT3 - Reload Register - for writing		TMRLR3	W
00006EH	RLT3 - Reload Register - for reading		TMR3	R
00006FH	RLT3 - Reload Register - for writing			W
00006FH	RLT3 - Reload Register - for reading			R
000070H	RLT6 - Timer Control Status Register Low (dedic. RLT for PPG)	TMCSRL6	TMCSR6	RW
000071H	RLT6 - Timer Control Status Register High (dedic. RLT for PPG)	TMCSRH6		RW
000072H	RLT6 - Reload Register (dedic. RLT for PPG) - for writing		TMRLR6	W
000072H	RLT6 - Reload Register (dedic. RLT for PPG) - for reading		TMR6	R
000073H	RLT6 - Reload Register (dedic. RLT for PPG) - for writing			W
000073H	RLT6 - Reload Register (dedic. RLT for PPG) - for reading			R
000074H	PPG3-PPG0 - General Control register 1 Low	GCN1L0	GCN10	RW
000075H	PPG3-PPG0 - General Control register 1 High	GCN1H0		RW
000076H	PPG3-PPG0 - General Control register 2 Low	GCN2L0	GCN20	RW
000077H	PPG3-PPG0 - General Control register 2 High	GCN2H0		RW
000078H	PPG0 - Timer register		PTMR0	R
000079H	PPG0 - Timer register			R
00007AH	PPG0 - Period setting register		PCSR0	W

I/O map MB96(F)38x (5 / 31)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00007BH	PPG0 - Period setting register			W
00007CH	PPG0 - Duty cycle register		PDUT0	W
00007DH	PPG0 - Duty cycle register			W
00007EH	PPG0 - Control status register Low	PCNL0	PCN0	RW
00007FH	PPG0 - Control status register High	PCNH0		RW
000080H	PPG1 - Timer register		PTMR1	R
000081H	PPG1 - Timer register			R
000082H	PPG1 - Period setting register		PCSR1	W
000083H	PPG1 - Period setting register			W
000084H	PPG1 - Duty cycle register		PDUT1	W
000085H	PPG1 - Duty cycle register			W
000086H	PPG1 - Control status register Low	PCNL1	PCN1	RW
000087H	PPG1 - Control status register High	PCNH1		RW
000088H	PPG2 - Timer register		PTMR2	R
000089H	PPG2 - Timer register			R
00008AH	PPG2 - Period setting register		PCSR2	W
00008BH	PPG2 - Period setting register			W
00008CH	PPG2 - Duty cycle register		PDUT2	W
00008DH	PPG2 - Duty cycle register			W
00008EH	PPG2 - Control status register Low	PCNL2	PCN2	RW
00008FH	PPG2 - Control status register High	PCNH2		RW
000090H	PPG3 - Timer register		PTMR3	R
000091H	PPG3 - Timer register			R
000092H	PPG3 - Period setting register		PCSR3	W
000093H	PPG3 - Period setting register			W
000094H	PPG3 - Duty cycle register		PDUT3	W
000095H	PPG3 - Duty cycle register			W
000096H	PPG3 - Control status register Low	PCNL3	PCN3	RW
000097H	PPG3 - Control status register High	PCNH3		RW
000098H	PPG7-PPG4 - General Control register 1 Low	GCN1L1	GCN11	RW

I/O map MB96(F)38x (6 / 31)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000099H	PPG7-PPG4 - General Control register 1 High	GCN1H1		RW
00009AH	PPG7-PPG4 - General Control register 2 Low	GCN2L1	GCN21	RW
00009BH	PPG7-PPG4 - General Control register 2 High	GCN2H1		RW
00009CH	PPG4 - Timer register		PTMR4	R
00009DH	PPG4 - Timer register			R
00009EH	PPG4 - Period setting register		PCSR4	W
00009FH	PPG4 - Period setting register			W
0000A0H	PPG4 - Duty cycle register		PDUT4	W
0000A1H	PPG4 - Duty cycle register			W
0000A2H	PPG4 - Control status register Low	PCNL4	PCN4	RW
0000A3H	PPG4 - Control status register High	PCNH4		RW
0000A4H	PPG5 - Timer register		PTMR5	R
0000A5H	PPG5 - Timer register			R
0000A6H	PPG5 - Period setting register		PCSR5	W
0000A7H	PPG5 - Period setting register			W
0000A8H	PPG5 - Duty cycle register		PDUT5	W
0000A9H	PPG5 - Duty cycle register			W
0000AAH	PPG5 - Control status register Low	PCNL5	PCN5	RW
0000ABH	PPG5 - Control status register High	PCNH5		RW
0000ACH	I2C0 - Bus Status Register	IBSR0		R
0000ADH	I2C0 - Bus Control Register	IBCR0		RW
0000AEH	I2C0 - Ten bit Slave address Register Low	ITBAL0	ITBA0	RW
0000AFH	I2C0 - Ten bit Slave address Register High	ITBAH0		RW
0000B0H	I2C0 - Ten bit Address mask Register Low	ITMKL0	ITMK0	RW
0000B1H	I2C0 - Ten bit Address mask Register High	ITMKH0		RW
0000B2H	I2C0 - Seven bit Slave address Register	ISBA0		RW
0000B3H	I2C0 - Seven bit Address mask Register	ISMK0		RW
0000B4H	I2C0 - Data Register	IDAR0		RW
0000B5H	I2C0 - Clock Control Register	ICCR0		RW

I/O map MB96(F)38x (7 / 31)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0000B6H-0000BFH	Reserved			-
0000C0H	USART0 - Serial Mode Register	SMR0		RW
0000C1H	USART0 - Serial Control Register	SCR0		RW
0000C2H	USART0 - TX Register	TDR0		W
0000C2H	USART0 - RX Register	RDR0		R
0000C3H	USART0 - Serial Status	SSR0		RW
0000C4H	USART0 - Control/Com. Register	ECCR0		RW
0000C5H	USART0 - Ext. Status Register	ESCR0		RW
0000C6H	USART0 - Baud Rate Generator Register Low	BGRL0	BGR0	RW
0000C7H	USART0 - Baud Rate Generator Register High	BGRH0		RW
0000C8H	USART0 - Extended Serial Interrupt Register	ESIR0		RW
0000C9H	Reserved			-
0000CAH	USART1 - Serial Mode Register	SMR1		RW
0000CBH	USART1 - Serial Control Register	SCR1		RW
0000CCH	USART1 - TX Register	TDR1		W
0000CCH	USART1 - RX Register	RDR1		R
0000CDH	USART1 - Serial Status	SSR1		RW
0000CEH	USART1 - Control/Com. Register	ECCR1		RW
0000CFH	USART1 - Ext. Status Register	ESCR1		RW
0000D0H	USART1 - Baud Rate Generator Register Low	BGRL1	BGR1	RW
0000D1H	USART1 - Baud Rate Generator Register High	BGRH1		RW
0000D2H	USART1 - Extended Serial Interrupt Register	ESIR1		RW
0000D3H	Reserved			-
0000D4H	USART2 - Serial Mode Register	SMR2		RW
0000D5H	USART2 - Serial Control Register	SCR2		RW
0000D6H	USART2 - TX Register	TDR2		W
0000D6H	USART2 - RX Register	RDR2		R
0000D7H	USART2 - Serial Status	SSR2		RW
0000D8H	USART2 - Control/Com. Register	ECCR2		RW

I/O map MB96(F)38x (8 / 31)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0000D9H	USART2 - Ext. Status Register	ESCR2		RW
0000DAH	USART2 - Baud Rate Generator Register Low	BGRL2	BGR2	RW
0000DBH	USART2 - Baud Rate Generator Register High	BGRH2		RW
0000DCH	USART2 - Extended Serial Interrupt Register	ESIR2		RW
0000DDH-0000EFH	Reserved			-
0000F0H-0000FFH	External Bus area	EXTBUS0		RW
000100H	DMA0 - Buffer address pointer low byte	BAPL0		RW
000101H	DMA0 - Buffer address pointer middle byte	BAPM0		RW
000102H	DMA0 - Buffer address pointer high byte	BAPH0		RW
000103H	DMA0 - DMA control register	DMACS0		RW
000104H	DMA0 - I/O register address pointer low byte	IOAL0	IOA0	RW
000105H	DMA0 - I/O register address pointer high byte	IOAH0		RW
000106H	DMA0 - Data counter low byte	DCTL0	DCT0	RW
000107H	DMA0 - Data counter high byte	DCTH0		RW
000108H	DMA1 - Buffer address pointer low byte	BAPL1		RW
000109H	DMA1 - Buffer address pointer middle byte	BAPM1		RW
00010AH	DMA1 - Buffer address pointer high byte	BAPH1		RW
00010BH	DMA1 - DMA control register	DMACS1		RW
00010CH	DMA1 - I/O register address pointer low byte	IOAL1	IOA1	RW
00010DH	DMA1 - I/O register address pointer high byte	IOAH1		RW
00010EH	DMA1 - Data counter low byte	DCTL1	DCT1	RW
00010FH	DMA1 - Data counter high byte	DCTH1		RW
000110H	DMA2 - Buffer address pointer low byte	BAPL2		RW
000111H	DMA2 - Buffer address pointer middle byte	BAPM2		RW
000112H	DMA2 - Buffer address pointer high byte	BAPH2		RW
000113H	DMA2 - DMA control register	DMACS2		RW
000114H	DMA2 - I/O register address pointer low byte	IOAL2	IOA2	RW
000115H	DMA2 - I/O register address pointer high byte	IOAH2		RW
000116H	DMA2 - Data counter low byte	DCTL2	DCT2	RW

I/O map MB96(F)38x (9 / 31)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000117H	DMA2 - Data counter high byte	DCTH2		RW
000118H	DMA3 - Buffer address pointer low byte	BAPL3		RW
000119H	DMA3 - Buffer address pointer middle byte	BAPM3		RW
00011AH	DMA3 - Buffer address pointer high byte	BAPH3		RW
00011BH	DMA3 - DMA control register	DMACS3		RW
00011CH	DMA3 - I/O register address pointer low byte	IOAL3	IOA3	RW
00011DH	DMA3 - I/O register address pointer high byte	IOAH3		RW
00011EH	DMA3 - Data counter low byte	DCTL3	DCT3	RW
00011FH	DMA3 - Data counter high byte	DCTH3		RW
000120H	DMA4 - Buffer address pointer low byte	BAPL4		RW
000121H	DMA4 - Buffer address pointer middle byte	BAPM4		RW
000122H	DMA4 - Buffer address pointer high byte	BAPH4		RW
000123H	DMA4 - DMA control register	DMACS4		RW
000124H	DMA4 - I/O register address pointer low byte	IOAL4	IOA4	RW
000125H	DMA4 - I/O register address pointer high byte	IOAH4		RW
000126H	DMA4 - Data counter low byte	DCTL4	DCT4	RW
000127H	DMA4 - Data counter high byte	DCTH4		RW
000128H	DMA5 - Buffer address pointer low byte	BAPL5		RW
000129H	DMA5 - Buffer address pointer middle byte	BAPM5		RW
00012AH	DMA5 - Buffer address pointer high byte	BAPH5		RW
00012BH	DMA5 - DMA control register	DMACS5		RW
00012CH	DMA5 - I/O register address pointer low byte	IOAL5	IOA5	RW
00012DH	DMA5 - I/O register address pointer high byte	IOAH5		RW
00012EH	DMA5 - Data counter low byte	DCTL5	DCT5	RW
00012FH	DMA5 - Data counter high byte	DCTH5		RW
000130H	DMA6 - Buffer address pointer low byte	BAPL6		RW
000131H	DMA6 - Buffer address pointer middle byte	BAPM6		RW
000132H	DMA6 - Buffer address pointer high byte	BAPH6		RW
000133H	DMA6 - DMA control register	DMACS6		RW
000134H	DMA6 - I/O register address pointer low byte	IOAL6	IOA6	RW

I/O map MB96(F)38x (10 / 31)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000135H	DMA6 - I/O register address pointer high byte	IOAH6		RW
000136H	DMA6 - Data counter low byte	DCTL6	DCT6	RW
000137H	DMA6 - Data counter high byte	DCTH6		RW
000138H-00017FH	Reserved			-
000180H-00037FH	CPU - General Purpose registers (RAM access)	GPR_RAM		RW
000380H	DMA0 - Interrupt select	DISEL0		RW
000381H	DMA1 - Interrupt select	DISEL1		RW
000382H	DMA2 - Interrupt select	DISEL2		RW
000383H	DMA3 - Interrupt select	DISEL3		RW
000384H	DMA4 - Interrupt select	DISEL4		RW
000385H	DMA5 - Interrupt select	DISEL5		RW
000386H	DMA6 - Interrupt select	DISEL6		RW
000387H-00038FH	Reserved			-
000390H	DMA7-DMA0 - status register Low	DSRL	DSR	RW
000391H	DMA15-DMA8 - status register High	DSRH		RW
000392H	DMA7-DMA0 - stop status register Low	DSSRL	DSSR	RW
000393H	DMA15-DMA8 - stop status register High	DSSRH		RW
000394H	DMA7-DMA0 - enable register Low	DERL	DER	RW
000395H	DMA15-DMA8 enable register High	DERH		RW
000396H-00039FH	Reserved			-
0003A0H	Interrupt level register	ILR	ICR	RW
0003A1H	Interrupt index register	IDX		RW
0003A2H	Interrupt vector table base register Low	TBRL	TBR	RW
0003A3H	Interrupt vector table base register High	TBRH		RW
0003A4H	Delayed Interrupt register	DIRR		RW
0003A5H	Non Maskable Interrupt register	NMI		RW
0003A6H-0003ABH	Reserved			-

I/O map MB96(F)38x (11 / 31)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0003ACH	EDSU communication interrupt selection Low	EDSU2L	EDSU2	RW
0003ADH	EDSU communication interrupt selection High	EDSU2H		RW
0003AEH	ROM mirror control register	ROMM		RW
0003AFH	EDSU configuration register	EDSU		RW
0003B0H	Memory patch control/status register ch 0/1		PFCS0	RW
0003B1H	Memory patch control/status register ch 0/1			RW
0003B2H	Memory patch control/status register ch 2/3		PFCS1	RW
0003B3H	Memory patch control/status register ch 2/3			RW
0003B4H	Memory patch control/status register ch 4/5		PFCS2	RW
0003B5H	Memory patch control/status register ch 4/5			RW
0003B6H	Memory patch control/status register ch 6/7		PFCS3	RW
0003B7H	Memory patch control/status register ch 6/7			RW
0003B8H	Memory Patch function - Patch address 0 low	PFAL0		RW
0003B9H	Memory Patch function - Patch address 0 middle	PFAM0		RW
0003BAH	Memory Patch function - Patch address 0 high	PFAH0		RW
0003BBH	Memory Patch function - Patch address 1 low	PFAL1		RW
0003BCH	Memory Patch function - Patch address 1 middle	PFAM1		RW
0003BDH	Memory Patch function - Patch address 1 high	PFAH1		RW
0003BEH	Memory Patch function - Patch address 2 low	PFAL2		RW
0003BFH	Memory Patch function - Patch address 2 middle	PFAM2		RW
0003C0H	Memory Patch function - Patch address 2 high	PFAH2		RW
0003C1H	Memory Patch function - Patch address 3 low	PFAL3		RW
0003C2H	Memory Patch function - Patch address 3 middle	PFAM3		RW
0003C3H	Memory Patch function - Patch address 3 high	PFAH3		RW
0003C4H	Memory Patch function - Patch address 4 low	PFAL4		RW
0003C5H	Memory Patch function - Patch address 4 middle	PFAM4		RW
0003C6H	Memory Patch function - Patch address 4 high	PFAH4		RW
0003C7H	Memory Patch function - Patch address 5 low	PFAL5		RW
0003C8H	Memory Patch function - Patch address 5 middle	PFAM5		RW
0003C9H	Memory Patch function - Patch address 5 high	PFAH5		RW

I/O map MB96(F)38x (12 / 31)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0003CAH	Memory Patch function - Patch address 6 low	PFAL6		RW
0003CBH	Memory Patch function - Patch address 6 middle	PFAM6		RW
0003CCH	Memory Patch function - Patch address 6 high	PFAH6		RW
0003CDH	Memory Patch function - Patch address 7 low	PFAL7		RW
0003CEH	Memory Patch function - Patch address 7 middle	PFAM7		RW
0003CFH	Memory Patch function - Patch address 7 high	PFAH7		RW
0003D0H	Memory Patch function - Patch data 0 Low	PFDL0	PFD0	RW
0003D1H	Memory Patch function - Patch data 0 High	PFDH0		RW
0003D2H	Memory Patch function - Patch data 1 Low	PFDL1	PFD1	RW
0003D3H	Memory Patch function - Patch data 1 High	PFDH1		RW
0003D4H	Memory Patch function - Patch data 2 Low	PFDL2	PFD2	RW
0003D5H	Memory Patch function - Patch data 2 High	PFDH2		RW
0003D6H	Memory Patch function - Patch data 3 Low	PFDL3	PFD3	RW
0003D7H	Memory Patch function - Patch data 3 High	PFDH3		RW
0003D8H	Memory Patch function - Patch data 4 Low	PFDL4	PFD4	RW
0003D9H	Memory Patch function - Patch data 4 High	PFDH4		RW
0003DAH	Memory Patch function - Patch data 5 Low	PFDL5	PFD5	RW
0003DBH	Memory Patch function - Patch data 5 High	PFDH5		RW
0003DCH	Memory Patch function - Patch data 6 Low	PFDL6	PFD6	RW
0003DDH	Memory Patch function - Patch data 6 High	PFDH6		RW
0003DEH	Memory Patch function - Patch data 7 Low	PFDL7	PFD7	RW
0003DFH	Memory Patch function - Patch data 7 High	PFDH7		RW
0003E0H-0003F0H	Reserved			-
0003F1H	Memory Control Status Register A	MCSRA		RW
0003F2H	Memory Timing Configuration Register A Low	MTCRAL	MTCRA	RW
0003F3H	Memory Timing Configuration Register A High	MTCRAH		RW
0003F4H	Reserved			-
0003F5H	Memory Control Status Register B	MCSRB		RW
0003F6H	Memory Timing Configuration Register B Low	MTCRBL	MTCRB	RW

I/O map MB96(F)38x (13 / 31)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0003F7H	Memory Timing Configuration Register B High	MTCRBH		RW
0003F8H	Flash Memory Write Control register 0	FMWC0		RW
0003F9H	Flash Memory Write Control register 1	FMWC1		RW
0003FAH	Flash Memory Write Control register 2	FMWC2		RW
0003FBH	Flash Memory Write Control register 3	FMWC3		RW
0003FCH	Flash Memory Write Control register 4	FMWC4		RW
0003FDH	Flash Memory Write Control register 5	FMWC5		RW
0003FEH-0003FFH	Reserved			-
000400H	Standby Mode control register	SMCR		RW
000401H	Clock select register	CKSR		RW
000402H	Clock Stabilisation select register	CKSSR		RW
000403H	Clock monitor register	CKMR		R
000404H	Clock Frequency control register Low	CKFCRL	CKFCR	RW
000405H	Clock Frequency control register High	CKFCRH		RW
000406H	PLL Control register Low	PLLCRL	PLLCR	RW
000407H	PLL Control register High	PLLCRH		RW
000408H	RC clock timer control register	RCTCR		RW
000409H	Main clock timer control register	MCTCR		RW
00040AH	Sub clock timer control register	SCTCR		RW
00040BH	Reset cause and clock status register with clear function	RCCSRC		R
00040CH	Reset configuration register	RCR		RW
00040DH	Reset cause and clock status register	RCCSR		R
00040EH	Watch dog timer configuration register	WDTC		RW
00040FH	Watch dog timer clear pattern register	WDTCP		W
000410H-000414H	Reserved			-
000415H	Clock output activation register	COAR		RW
000416H	Clock output configuration register 0	COCR0		RW
000417H	Clock output configuration register 1	COCR1		RW

I/O map MB96(F)38x (14 / 31)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000418H	Clock Modulator control register	CMCR		RW
000419H	Reserved			-
00041AH	Clock Modulator Parameter register Low	CMPRL	CMPR	RW
00041BH	Clock Modulator Parameter register High	CMPRH		RW
00041CH-00042BH	Reserved			-
00042CH	Voltage Regulator Control register	VRCR		RW
00042DH	Clock Input and LVD Control Register	CILCR		RW
00042EH-00042FH	Reserved			-
000430H	I/O Port P00 - Data Direction Register	DDR00		RW
000431H	I/O Port P01 - Data Direction Register	DDR01		RW
000432H	I/O Port P02 - Data Direction Register	DDR02		RW
000433H	I/O Port P03 - Data Direction Register	DDR03		RW
000434H	I/O Port P04 - Data Direction Register	DDR04		RW
000435H	I/O Port P05 - Data Direction Register	DDR05		RW
000436H	I/O Port P06 - Data Direction Register	DDR06		RW
000437H	Reserved			-
000438H	I/O Port P08 - Data Direction Register	DDR08		RW
000439H	I/O Port P09 - Data Direction Register	DDR09		RW
00043AH	I/O Port P10 - Data Direction Register	DDR10		RW
00043BH	I/O Port P11 - Data Direction Register	DDR11		RW
00043CH	I/O Port P12 - Data Direction Register	DDR12		RW
00043DH	I/O Port P13 - Data Direction Register	DDR13		RW
00043EH-000443H	Reserved			-
000444H	I/O Port P00 - Port Input Enable Register	PIER00		RW
000445H	I/O Port P01 - Port Input Enable Register	PIER01		RW
000446H	I/O Port P02 - Port Input Enable Register	PIER02		RW
000447H	I/O Port P03 - Port Input Enable Register	PIER03		RW
000448H	I/O Port P04 - Port Input Enable Register	PIER04		RW

I/O map MB96(F)38x (15 / 31)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000449H	I/O Port P05 - Port Input Enable Register	PIER05		RW
00044AH	I/O Port P06 - Port Input Enable Register	PIER06		RW
00044BH	Reserved			-
00044CH	I/O Port P08 - Port Input Enable Register	PIER08		RW
00044DH	I/O Port P09 - Port Input Enable Register	PIER09		RW
00044EH	I/O Port P10 - Port Input Enable Register	PIER10		RW
00044FH	I/O Port P11 - Port Input Enable Register	PIER11		RW
000450H	I/O Port P12 - Port Input Enable Register	PIER12		RW
000451H	I/O Port P13 - Port Input Enable Register	PIER13		RW
000452H-000457H	Reserved			-
000458H	I/O Port P00 - Port Input Level Register	PILR00		RW
000459H	I/O Port P01 - Port Input Level Register	PILR01		RW
00045AH	I/O Port P02 - Port Input Level Register	PILR02		RW
00045BH	I/O Port P03 - Port Input Level Register	PILR03		RW
00045CH	I/O Port P04 - Port Input Level Register	PILR04		RW
00045DH	I/O Port P05 - Port Input Level Register	PILR05		RW
00045EH	I/O Port P06 - Port Input Level Register	PILR06		RW
00045FH	Reserved			-
000460H	I/O Port P08 - Port Input Level Register	PILR08		RW
000461H	I/O Port P09 - Port Input Level Register	PILR09		RW
000462H	I/O Port P10 - Port Input Level Register	PILR10		RW
000463H	I/O Port P11 - Port Input Level Register	PILR11		RW
000464H	I/O Port P12 - Port Input Level Register	PILR12		RW
000465H	I/O Port P13 - Port Input Level Register	PILR13		RW
000466H-00046BH	Reserved			-
00046CH	I/O Port P00 - Extended Port Input Level Register	EPILR00		RW
00046DH	I/O Port P01 - Extended Port Input Level Register	EPILR01		RW
00046EH	I/O Port P02 - Extended Port Input Level Register	EPILR02		RW
00046FH	I/O Port P03 - Extended Port Input Level Register	EPILR03		RW

I/O map MB96(F)38x (16 / 31)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000470H	I/O Port P04 - Extended Port Input Level Register	EPILR04		RW
000471H	I/O Port P05 - Extended Port Input Level Register	EPILR05		RW
000472H	I/O Port P06 - Extended Port Input Level Register	EPILR06		RW
000473H	Reserved			-
000474H	I/O Port P08 - Extended Port Input Level Register	EPILR08		RW
000475H	I/O Port P09 - Extended Port Input Level Register	EPILR09		RW
000476H	I/O Port P10 - Extended Port Input Level Register	EPILR10		RW
000477H	I/O Port P11 - Extended Port Input Level Register	EPILR11		RW
000478H	I/O Port P12 - Extended Port Input Level Register	EPILR12		RW
000479H	I/O Port P13 - Extended Port Input Level Register	EPILR13		RW
00047AH-00047FH	Reserved			-
000480H	I/O Port P00 - Port Output Drive Register	PODR00		RW
000481H	I/O Port P01 - Port Output Drive Register	PODR01		RW
000482H	I/O Port P02 - Port Output Drive Register	PODR02		RW
000483H	I/O Port P03 - Port Output Drive Register	PODR03		RW
000484H	I/O Port P04 - Port Output Drive Register	PODR04		RW
000485H	I/O Port P05 - Port Output Drive Register	PODR05		RW
000486H	I/O Port P06 - Port Output Drive Register	PODR06		RW
000487H	Reserved			-
000488H	I/O Port P08 - Port Output Drive Register	PODR08		RW
000489H	I/O Port P09 - Port Output Drive Register	PODR09		RW
00048AH	I/O Port P10 - Port Output Drive Register	PODR10		RW
00048BH	I/O Port P11 - Port Output Drive Register	PODR11		RW
00048CH	I/O Port P12 - Port Output Drive Register	PODR12		RW
00048DH	I/O Port P13 - Port Output Drive Register	PODR13		RW
00048EH-00049BH	Reserved			-
00049CH	I/O Port P08 - Port High Drive Register	PHDR08		RW
00049DH	I/O Port P09 - Port High Drive Register	PHDR09		RW
00049EH	I/O Port P10 - Port High Drive Register	PHDR10		RW

I/O map MB96(F)38x (17 / 31)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00049FH-0004A7H	Reserved			-
0004A8H	I/O Port P00 - Pull-Up resistor Control Register	PUCR00		RW
0004A9H	I/O Port P01 - Pull-Up resistor Control Register	PUCR01		RW
0004AAH	I/O Port P02 - Pull-Up resistor Control Register	PUCR02		RW
0004ABH	I/O Port P03 - Pull-Up resistor Control Register	PUCR03		RW
0004ACH	I/O Port P04 - Pull-Up resistor Control Register	PUCR04		RW
0004ADH	I/O Port P05 - Pull-Up resistor Control Register	PUCR05		RW
0004AEH	I/O Port P06 - Pull-Up resistor Control Register	PUCR06		RW
0004AFH	Reserved			-
0004B0H	I/O Port P08 - Pull-Up resistor Control Register	PUCR08		RW
0004B1H	I/O Port P09 - Pull-Up resistor Control Register	PUCR09		RW
0004B2H	I/O Port P10 - Pull-Up resistor Control Register	PUCR10		RW
0004B3H	I/O Port P11 - Pull-Up resistor Control Register	PUCR11		RW
0004B4H	I/O Port P12 - Pull-Up resistor Control Register	PUCR12		RW
0004B5H	I/O Port P13 - Pull-Up resistor Control Register	PUCR13		RW
0004B6H-0004BBH	Reserved			-
0004BCH	I/O Port P00 - External Pin State Register	EPSR00		R
0004BDH	I/O Port P01 - External Pin State Register	EPSR01		R
0004BEH	I/O Port P02 - External Pin State Register	EPSR02		R
0004BFH	I/O Port P03 - External Pin State Register	EPSR03		R
0004C0H	I/O Port P04 - External Pin State Register	EPSR04		R
0004C1H	I/O Port P05 - External Pin State Register	EPSR05		R
0004C2H	I/O Port P06 - External Pin State Register	EPSR06		R
0004C3H	Reserved			-
0004C4H	I/O Port P08 - External Pin State Register	EPSR08		R
0004C5H	I/O Port P09 - External Pin State Register	EPSR09		R
0004C6H	I/O Port P10 - External Pin State Register	EPSR10		R
0004C7H	I/O Port P11 - External Pin State Register	EPSR11		R
0004C8H	I/O Port P12 - External Pin State Register	EPSR12		R

I/O map MB96(F)38x (18 / 31)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0004C9H	I/O Port P13 - External Pin State Register	EPSR13		R
0004CAH-0004CFH	Reserved			-
0004D0H	ADC analog input enable register 0	ADER0		RW
0004D1H	ADC analog input enable register 1	ADER1		RW
0004D2H	ADC analog input enable register 2	ADER2		RW
0004D3H	ADC analog input enable register 3	ADER3		RW
0004D4H	ADC analog input enable register 4	ADER4		RW
0004D5H	Reserved			-
0004D6H	Peripheral Resource Relocation Register 0	PRRR0		RW
0004D7H	Peripheral Resource Relocation Register 1	PRRR1		RW
0004D8H	Peripheral Resource Relocation Register 2	PRRR2		RW
0004D9H	Peripheral Resource Relocation Register 3	PRRR3		RW
0004DAH	Peripheral Resource Relocation Register 4	PRRR4		RW
0004DBH	Peripheral Resource Relocation Register 5	PRRR5		RW
0004DCH	Peripheral Resource Relocation Register 6	PRRR6		RW
0004DDH	Peripheral Resource Relocation Register 7	PRRR7		RW
0004DEH	Peripheral Resource Relocation Register 8	PRRR8		RW
0004DFH	Peripheral Resource Relocation Register 9	PRRR9		RW
0004E0H	RTC - Sub Second Register L	WTBRL0	WTBR0	RW
0004E1H	RTC - Sub Second Register M	WTBRH0		RW
0004E2H	RTC - Sub-Second Register H	WTBR1		RW
0004E3H	RTC - Second Register	WTSR		RW
0004E4H	RTC - Minutes	WTMR		RW
0004E5H	RTC - Hour	WTHR		RW
0004E6H	RTC - Timer Control Extended Register	WTCER		RW
0004E7H	RTC - Clock select register	WTCKSR		RW
0004E8H	RTC - Timer Control Register Low	WTCRL	WTCR	RW
0004E9H	RTC - Timer Control Register High	WTCRH		RW
0004EAH	CAL - Calibration unit Control register	CUCR		RW

I/O map MB96(F)38x (19 / 31)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0004EBH	Reserved			-
0004ECH	CAL - Duration Timer Data Register Low	CUTDL	CUTD	RW
0004EDH	CAL - Duration Timer Data Register High	CUTDH		RW
0004EEH	CAL - Calibration Timer Register 2 Low	CUTR2L	CUTR2	R
0004EFH	CAL - Calibration Timer Register 2 High	CUTR2H		R
0004F0H	CAL - Calibration Timer Register 1 Low	CUTR1L	CUTR1	R
0004F1H	CAL - Calibration Timer Register 1 High	CUTR1H		R
0004F2H-0004F9H	Reserved			-
0004FAH	RLT - Timer input select (for Cascading)	TMISR		RW
0004FBH-00051FH	Reserved			-
000520H	USART4 - Serial Mode Register	SMR4		RW
000521H	USART4 - Serial Control Register	SCR4		RW
000522H	USART4 - TX Register	TDR4		W
000522H	USART4 - RX Register	RDR4		R
000523H	USART4 - Serial Status	SSR4		RW
000524H	USART4 - Control/Com. Register (internal)	ECCR4		RW
000525H	USART4 - Ext. Status Register	ESCR4		RW
000526H	USART4 - Baud Rate Generator Register Low	BGRL4	BGR4	RW
000527H	USART4 - Baud Rate Generator Register High	BGRH4		RW
000528H	USART4 - Extended Serial Interrupt Register	ESIR4		RW
000529H	Reserved			-
00052AH	USART5 - Serial Mode Register	SMR5		RW
00052BH	USART5 - Serial Control Register	SCR5		RW
00052CH	USART5 - RX Register	TDR5		W
00052CH	USART5 - TX Register	RDR5		R
00052DH	USART5 - Serial Status	SSR5		RW
00052EH	USART5 - Control/Com. Register	ECCR5		RW
00052FH	USART5 - Ext. Status Register	ESCR5		RW
000530H	USART5 - Baud Rate Generator Register Low	BGRL5	BGR5	RW

I/O map MB96(F)38x (20 / 31)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000531H	USART5 - Baud Rate Generator Register High	BGRH5		RW
000532H	USART5 - Extended Serial Interrupt Register	ESIR5		RW
000533H-00055FH	Reserved			-
000560H	ALARM0 - Control Status Register	ACSR0		RW
000561H	ALARM0 - Extended Control Status Register	AECSR0		RW
000562H	ALARM1 - Control Status Register	ACSR1		RW
000563H	ALARM1 - Extended Control Status Register	AECSR1		RW
000564H	PPG6 - Timer register		PTMR6	R
000565H	PPG6 - Timer register			R
000566H	PPG6 - Period setting register		PCSR6	W
000567H	PPG6 - Period setting register			W
000568H	PPG6 - Duty cycle register		PDUT6	W
000569H	PPG6 - Duty cycle register			W
00056AH	PPG6 - Control status register Low	PCNL6	PCN6	RW
00056BH	PPG6 - Control status register High	PCNH6		RW
00056CH	PPG7 - Timer register		PTMR7	R
00056DH	PPG7 - Timer register			R
00056EH	PPG7 - Period setting register		PCSR7	W
00056FH	PPG7 - Period setting register			W
000570H	PPG7 - Duty cycle register		PDUT7	W
000571H	PPG7 - Duty cycle register			W
000572H	PPG7 - Control status register Low	PCNL7	PCN7	RW
000573H	PPG7 - Control status register High	PCNH7		RW
000574H-0005DFH	Reserved			-
0005E0H	SMC0 - PWM control register	PWC0		RW
0005E1H	SMC0 - Extended control register (Output enable)	PWEC0		RW
0005E2H	SMC0 - PWM compare register PWM 1		PWC10	RW
0005E3H	SMC0 - PWM compare register PWM 1			RW
0005E4H	SMC0 - PWM compare register PWM 2		PWC20	RW

I/O map MB96(F)38x (21 / 31)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0005E5H	SMC0 - PWM compare register PWM 2			RW
0005E6H	SMC0 - PWM Select register	PWS10		RW
0005E7H	SMC0 - PWM Select register	PWS20		RW
0005E8H-0005E9H	Reserved			-
0005EAH	SMC1 - PWM control register	PWC1		RW
0005EBH	SMC1 - Extended control register (Output enable)	PWEC1		RW
0005ECH	SMC1 - PWM compare register PWM 1		PWC11	RW
0005EDH	SMC1 - PWM compare register PWM 1			RW
0005EEH	SMC1 - PWM compare register PWM 2		PWC21	RW
0005EFH	SMC1 - PWM compare register PWM 2			RW
0005F0H	SMC1 - PWM Select register	PWS11		RW
0005F1H	SMC1 - PWM Select register	PWS21		RW
0005F2H-0005F3H	Reserved			-
0005F4H	SMC2 - PWM control register	PWC2		RW
0005F5H	SMC2 - Extended control register (Output enable)	PWEC2		RW
0005F6H	SMC2 - PWM compare register PWM 1		PWC12	RW
0005F7H	SMC2 - PWM compare register PWM 1			RW
0005F8H	SMC2 - PWM compare register PWM 2		PWC22	RW
0005F9H	SMC2 - PWM compare register PWM 2			RW
0005FAH	SMC2 - PWM Select register	PWS12		RW
0005FBH	SMC2 - PWM Select register	PWS22		RW
0005FCH-0005FDH	Reserved			-
0005FEH	SMC3 - PWM control register	PWC3		RW
0005FFH	SMC3 - Extended control register (Output enable)	PWEC3		RW
000600H	SMC3 - PWM compare register PWM 1		PWC13	RW
000601H	SMC3 - PWM compare register PWM 1			RW
000602H	SMC3 - PWM compare register PWM 2		PWC23	RW
000603H	SMC3 - PWM compare register PWM 2			RW

I/O map MB96(F)38x (22 / 31)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000604H	SMC3 - PWM Select register	PWS13		RW
000605H	SMC3 - PWM Select register	PWS23		RW
000606H-000607H	Reserved			-
000608H	SMC4 - PWM control register	PWC4		RW
000609H	SMC4 - Extended control register (Output enable)	PWEC4		RW
00060AH	SMC4 - PWM compare register PWM 1		PWC14	RW
00060BH	SMC4 - PWM compare register PWM 1			RW
00060CH	SMC4 - PWM compare register PWM 2		PWC24	RW
00060DH	SMC4 - PWM compare register PWM 2			RW
00060EH	SMC4 - PWM Select register	PWS14		RW
00060FH	SMC4 - PWM Select register	PWS24		RW
000610H-00061BH	Reserved			-
00061CH	LCD - Output Enable Register 0 (Seg 7-0)	LCDER0		RW
00061DH	LCD - Output Enable Register 1 (Seg 15-8)	LCDER1		RW
00061EH	LCD - Output Enable Register 2 (Seg 23-16)	LCDER2		RW
00061FH	LCD - Output Enable Register 3 (Seg 31-24)	LCDER3		RW
000620H	LCD - Output Enable Register 4 (Seg 39-32)	LCDER4		RW
000621H	LCD - Output Enable Register 5 (Seg 47-40)	LCDER5		RW
000622H	LCD - Output Enable Register 6 (Seg 55-48)	LCDER6		RW
000623H	LCD - Output Enable Register 7 (Seg 63-56)	LCDER7		RW
000624H	LCD - Output Enable Register 8 (Seg 71-64)	LCDER8		RW
000625H	Reserved			-
000626H	LCD - Output Enable Register V (Vx)	LCDVER		RW
000627H	LCD - Extended Control Register	LECR		RW
000628H	LCD - Common pin switching register	LCDCMR		RW
000629H	LCD - Control Register	LCR		RW
00062AH	LCD - Data register for Segment 1-0	VRAM0		RW
00062BH	LCD - Data register for Segment 3-2	VRAM1		RW
00062CH	LCD - Data register for Segment 5-4	VRAM2		RW

I/O map MB96(F)38x (23 / 31)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00062DH	LCD - Data register for Segment 7-6	VRAM3		RW
00062EH	LCD - Data register for Segment 9-8	VRAM4		RW
00062FH	LCD - Data register for Segment 11-10	VRAM5		RW
000630H	LCD - Data register for Segment 13-12	VRAM6		RW
000631H	LCD - Data register for Segment 15-14	VRAM7		RW
000632H	LCD - Data register for Segment 17-16	VRAM8		RW
000633H	LCD - Data register for Segment 19-18	VRAM9		RW
000634H	LCD - Data register for Segment 21-20	VRAM10		RW
000635H	LCD - Data register for Segment 23-22	VRAM11		RW
000636H	LCD - Data register for Segment 25-24	VRAM12		RW
000637H	LCD - Data register for Segment 27-26	VRAM13		RW
000638H	LCD - Data register for Segment 29-28	VRAM14		RW
000639H	LCD - Data register for Segment 31-30	VRAM15		RW
00063AH	LCD - Data register for Segment 33-32	VRAM16		RW
00063BH	LCD - Data register for Segment 35-34	VRAM17		RW
00063CH	LCD - Data register for Segment 37-36	VRAM18		RW
00063DH	LCD - Data register for Segment 39-38	VRAM19		RW
00063EH	LCD - Data register for Segment 41-40	VRAM20		RW
00063FH	LCD - Data register for Segment 43-42	VRAM21		RW
000640H	LCD - Data register for Segment 45-44	VRAM22		RW
000641H	LCD - Data register for Segment 47-46	VRAM23		RW
000642H	LCD - Data register for Segment 49-48	VRAM24		RW
000643H	LCD - Data register for Segment 51-50	VRAM25		RW
000644H	LCD - Data register for Segment 53-52	VRAM26		RW
000645H	LCD - Data register for Segment 55-54	VRAM27		RW
000646H	LCD - Data register for Segment 57-56	VRAM28		RW
000647H	LCD - Data register for Segment 59-58	VRAM29		RW
000648H	LCD - Data register for Segment 61-60	VRAM30		RW
000649H	LCD - Data register for Segment 63-62	VRAM31		RW
00064AH	LCD - Data register for Segment 65-64	VRAM32		RW

I/O map MB96(F)38x (24 / 31)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00064BH-00065FH	Reserved			-
000660H	Peripheral Resource Relocation Register 10	PRRR10		RW
000661H	Peripheral Resource Relocation Register 11	PRRR11		RW
000662H	Peripheral Resource Relocation Register 12	PRRR12		RW
000663H	Peripheral Resource Relocation Register 13	PRRR13		W
000664H-0006DFH	Reserved			-
0006E0H	External Bus - Area configuration register 0 Low	EACL0	EAC0	RW
0006E1H	External Bus - Area configuration register 0 High	EACH0		RW
0006E2H	External Bus - Area configuration register 1 Low	EACL1	EAC1	RW
0006E3H	External Bus - Area configuration register 1 High	EACH1		RW
0006E4H	External Bus - Area configuration register 2 Low	EACL2	EAC2	RW
0006E5H	External Bus - Area configuration register 2 High	EACH2		RW
0006E6H	External Bus - Area configuration register 3 Low	EACL3	EAC3	RW
0006E7H	External Bus - Area configuration register 3 High	EACH3		RW
0006E8H	External Bus - Area configuration register 4 Low	EACL4	EAC4	RW
0006E9H	External Bus - Area configuration register 4 High	EACH4		RW
0006EAH	External Bus - Area configuration register 5 Low	EACL5	EAC5	RW
0006EBH	External Bus - Area configuration register 5 High	EACH5		RW
0006ECH	External Bus - Area select register 2	EAS2		RW
0006EDH	External Bus - Area select register 3	EAS3		RW
0006EEH	External Bus - Area select register 4	EAS4		RW
0006EFH	External Bus - Area select register 5	EAS5		RW
0006F0H	External Bus - Mode register	EBM		RW
0006F1H	External Bus - Clock and Function register	EBCF		RW
0006F2H	External Bus - Address output enable register 0	EBAE0		RW
0006F3H	External Bus - Address output enable register 1	EBAE1		RW
0006F4H	External Bus - Address output enable register 2	EBAE2		RW
0006F5H	External Bus - Control signal register	EBCS		RW

I/O map MB96(F)38x (25 / 31)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0006F6H-0006FFH	Reserved			-
000700H	CAN0 - Control register Low	CTRLRL0	CTRLR0	RW
000701H	CAN0 - Control register High (reserved)	CTRLRH0		R
000702H	CAN0 - Status register Low	STATRL0	STATR0	RW
000703H	CAN0 - Status register High (reserved)	STATRH0		R
000704H	CAN0 - Error Counter Low (Transmit)	ERRCNTL0	ERRCNT0	R
000705H	CAN0 - Error Counter High (Receive)	ERRCNTH0		R
000706H	CAN0 - Bit Timing Register Low	BTRL0	BTR0	RW
000707H	CAN0 - Bit Timing Register High	BTRH0		RW
000708H	CAN0 - Interrupt Register Low	INTRL0	INTR0	R
000709H	CAN0 - Interrupt Register High	INTRH0		R
00070AH	CAN0 - Test Register Low	TESTRL0	TESTR0	RW
00070BH	CAN0 - Test Register High (reserved)	TESTRH0		R
00070CH	CAN0 - BRP Extension register Low	BRPERL0	BRPER0	RW
00070DH	CAN0 - BRP Extension register High (reserved)	BRPERH0		R
00070EH-00070FH	Reserved			-
000710H	CAN0 - IF1 Command request register Low	IF1CREQL0	IF1CREQ0	RW
000711H	CAN0 - IF1 Command request register High	IF1CREQH0		RW
000712H	CAN0 - IF1 Command Mask register Low	IF1CMSKL0	IF1CMSK0	RW
000713H	CAN0 - IF1 Command Mask register High (reserved)	IF1CMSKH0		R
000714H	CAN0 - IF1 Mask 1 Register Low	IF1MSK1L0	IF1MSK10	RW
000715H	CAN0 - IF1 Mask 1 Register High	IF1MSK1H0		RW
000716H	CAN0 - IF1 Mask 2 Register Low	IF1MSK2L0	IF1MSK20	RW
000717H	CAN0 - IF1 Mask 2 Register High	IF1MSK2H0		RW
000718H	CAN0 - IF1 Arbitration 1 Register Low	IF1ARB1L0	IF1ARB10	RW
000719H	CAN0 - IF1 Arbitration 1 Register High	IF1ARB1H0		RW
00071AH	CAN0 - IF1 Arbitration 2 Register Low	IF1ARB2L0	IF1ARB20	RW
00071BH	CAN0 - IF1 Arbitration 2 Register High	IF1ARB2H0		RW

I/O map MB96(F)38x (26 / 31)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00071CH	CAN0 - IF1 Message Control Register Low	IF1MCTRL0	IF1MCTR0	RW
00071DH	CAN0 - IF1 Message Control Register High	IF1MCTRH0		RW
00071EH	CAN0 - IF1 Data A1 Low	IF1DTA1L0	IF1DTA10	RW
00071FH	CAN0 - IF1 Data A1 High	IF1DTA1H0		RW
000720H	CAN0 - IF1 Data A2 Low	IF1DTA2L0	IF1DTA20	RW
000721H	CAN0 - IF1 Data A2 High	IF1DTA2H0		RW
000722H	CAN0 - IF1 Data B1 Low	IF1DTB1L0	IF1DTB10	RW
000723H	CAN0 - IF1 Data B1 High	IF1DTB1H0		RW
000724H	CAN0 - IF1 Data B2 Low	IF1DTB2L0	IF1DTB20	RW
000725H	CAN0 - IF1 Data B2 High	IF1DTB2H0		RW
000726H-00073FH	Reserved			-
000740H	CAN0 - IF2 Command request register Low	IF2CREQL0	IF2CREQ0	RW
000741H	CAN0 - IF2 Command request register High	IF2CREQH0		RW
000742H	CAN0 - IF2 Command Mask register Low	IF2CMSKL0	IF2CMSK0	RW
000743H	CAN0 - IF2 Command Mask register High (reserved)	IF2CMSKH0		R
000744H	CAN0 - IF2 Mask 1 Register Low	IF2MSK1L0	IF2MSK10	RW
000745H	CAN0 - IF2 Mask 1 Register High	IF2MSK1H0		RW
000746H	CAN0 - IF2 Mask 2 Register Low	IF2MSK2L0	IF2MSK20	RW
000747H	CAN0 - IF2 Mask 2 Register High	IF2MSK2H0		RW
000748H	CAN0 - IF2 Arbitration 1 Register Low	IF2ARB1L0	IF2ARB10	RW
000749H	CAN0 - IF2 Arbitration 1 Register High	IF2ARB1H0		RW
00074AH	CAN0 - IF2 Arbitration 2 Register Low	IF2ARB2L0	IF2ARB20	RW
00074BH	CAN0 - IF2 Arbitration 2 Register High	IF2ARB2H0		RW
00074CH	CAN0 - IF2 Message Control Register Low	IF2MCTRL0	IF2MCTR0	RW
00074DH	CAN0 - IF2 Message Control Register High	IF2MCTRH0		RW
00074EH	CAN0 - IF2 Data A1 Low	IF2DTA1L0	IF2DTA10	RW
00074FH	CAN0 - IF2 Data A1 High	IF2DTA1H0		RW
000750H	CAN0 - IF2 Data A2 Low	IF2DTA2L0	IF2DTA20	RW
000751H	CAN0 - IF2 Data A2 High	IF2DTA2H0		RW

I/O map MB96(F)38x (27 / 31)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000752H	CAN0 - IF2 Data B1 Low	IF2DTB1L0	IF2DTB10	RW
000753H	CAN0 - IF2 Data B1 High	IF2DTB1H0		RW
000754H	CAN0 - IF2 Data B2 Low	IF2DTB2L0	IF2DTB20	RW
000755H	CAN0 - IF2 Data B2 High	IF2DTB2H0		RW
000756H-00077FH	Reserved			-
000780H	CAN0 - Transmission Request 1 Register Low	TREQR1L0	TREQR10	R
000781H	CAN0 - Transmission Request 1 Register High	TREQR1H0		R
000782H	CAN0 - Transmission Request 2 Register Low	TREQR2L0	TREQR20	R
000783H	CAN0 - Transmission Request 2 Register High	TREQR2H0		R
000784H-00078FH	Reserved			-
000790H	CAN0 - New Data 1 Register Low	NEWDT1L0	NEWDT10	R
000791H	CAN0 - New Data 1 Register High	NEWDT1H0		R
000792H	CAN0 - New Data 2 Register Low	NEWDT2L0	NEWDT20	R
000793H	CAN0 - New Data 2 Register High	NEWDT2H0		R
000794H-00079FH	Reserved			-
0007A0H	CAN0 - Interrupt Pending 1 Register Low	INTPND1L0	INTPND10	R
0007A1H	CAN0 - Interrupt Pending 1 Register High	INTPND1H0		R
0007A2H	CAN0 - Interrupt Pending 2 Register Low	INTPND2L0	INTPND20	R
0007A3H	CAN0 - Interrupt Pending 2 Register High	INTPND2H0		R
0007A4H-0007AFH	Reserved			-
0007B0H	CAN0 - Message Valid 1 Register Low	MSGVAL1L0	MSGVAL10	R
0007B1H	CAN0 - Message Valid 1 Register High	MSGVAL1H0		R
0007B2H	CAN0 - Message Valid 2 Register Low	MSGVAL2L0	MSGVAL20	R
0007B3H	CAN0 - Message Valid 2 Register High	MSGVAL2H0		R
0007B4H-0007CDH	Reserved			-
0007CEH	CAN0 - Output enable register	COER0		RW
0007CFH	Reserved			-

I/O map MB96(F)38x (28 / 31)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0007D0H	SG0 - Sound Generator Control Register Low	SGCRL0	SGCR0	RW
0007D1H	SG0 - Sound Generator Control Register High	SGCRH0		RW
0007D2H	SG0 - Sound Generator Frequency Register	SGFR0		RW
0007D3H	SG0 - Sound Generator Amplitude Register	SGAR0		RW
0007D4H	SG0 - Sound Generator Decrement Register	SGDR0		RW
0007D5H	SG0 - Sound Generator Tone Register	SGTR0		RW
0007D6H	SG1 - Sound Generator Control Register Low	SGCRL1	SGCR1	RW
0007D7H	SG1 - Sound Generator Control Register High	SGCRH1		RW
0007D8H	SG1 - Sound Generator Frequency Register	SGFR1		RW
0007D9H	SG1 - Sound Generator Amplitude Register	SGAR1		RW
0007DAH	SG1 - Sound Generator Decrement Register	SGDR1		RW
0007DBH	SG1 - Sound Generator Tone Register	SGTR1		RW
0007DCH-0007FFH	Reserved			-
000800H	CAN1 - Control register Low	CTRLRL1	CTRLR1	RW
000801H	CAN1 - Control register High (reserved)	CTRLRH1		R
000802H	CAN1 - Status register Low	STATRL1	STATR1	RW
000803H	CAN1 - Status register High (reserved)	STATRH1		R
000804H	CAN1 - Error Counter Low (Transmit)	ERRCNTL1	ERRCNT1	R
000805H	CAN1 - Error Counter High (Receive)	ERRCNTH1		R
000806H	CAN1 - Bit Timing Register Low	BTRL1	BTR1	RW
000807H	CAN1 - Bit Timing Register High	BTRH1		RW
000808H	CAN1 - Interrupt Register Low	INTRL1	INTR1	R
000809H	CAN1 - Interrupt Register High	INTRH1		R
00080AH	CAN1 - Test Register Low	TESTRL1	TESTR1	RW
00080BH	CAN1 - Test Register High (reserved)	TESTRH1		R
00080CH	CAN1 - BRP Extension register Low	BRPERL1	BRPER1	RW
00080DH	CAN1 - BRP Extension register High (reserved)	BRPERH1		R
00080EH-00080FH	Reserved			-
000810H	CAN1 - IF1 Command request register Low	IF1CREQL1	IF1CREQ1	RW

I/O map MB96(F)38x (29 / 31)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000811H	CAN1 - IF1 Command request register High	IF1CREQH1		RW
000812H	CAN1 - IF1 Command Mask register Low	IF1CMSKL1	IF1CMSK1	RW
000813H	CAN1 - IF1 Command Mask register High (reserved)	IF1CMSKH1		R
000814H	CAN1 - IF1 Mask 1 Register Low	IF1MSK1L1	IF1MSK11	RW
000815H	CAN1 - IF1 Mask 1 Register High	IF1MSK1H1		RW
000816H	CAN1 - IF1 Mask 2 Register Low	IF1MSK2L1	IF1MSK21	RW
000817H	CAN1 - IF1 Mask 2 Register High	IF1MSK2H1		RW
000818H	CAN1 - IF1 Arbitration 1 Register Low	IF1ARB1L1	IF1ARB11	RW
000819H	CAN1 - IF1 Arbitration 1 Register High	IF1ARB1H1		RW
00081AH	CAN1 - IF1 Arbitration 2 Register Low	IF1ARB2L1	IF1ARB21	RW
00081BH	CAN1 - IF1 Arbitration 2 Register High	IF1ARB2H1		RW
00081CH	CAN1 - IF1 Message Control Register Low	IF1MCTRL1	IF1MCTR1	RW
00081DH	CAN1 - IF1 Message Control Register High	IF1MCTRH1		RW
00081EH	CAN1 - IF1 Data A1 Low	IF1DTA1L1	IF1DTA11	RW
00081FH	CAN1 - IF1 Data A1 High	IF1DTA1H1		RW
000820H	CAN1 - IF1 Data A2 Low	IF1DTA2L1	IF1DTA21	RW
000821H	CAN1 - IF1 Data A2 High	IF1DTA2H1		RW
000822H	CAN1 - IF1 Data B1 Low	IF1DTB1L1	IF1DTB11	RW
000823H	CAN1 - IF1 Data B1 High	IF1DTB1H1		RW
000824H	CAN1 - IF1 Data B2 Low	IF1DTB2L1	IF1DTB21	RW
000825H	CAN1 - IF1 Data B2 High	IF1DTB2H1		RW
000826H-00083FH	Reserved			-
000840H	CAN1 - IF2 Command request register Low	IF2CREQL1	IF2CREQ1	RW
000841H	CAN1 - IF2 Command request register High	IF2CREQH1		RW
000842H	CAN1 - IF2 Command Mask register Low	IF2CMSKL1	IF2CMSK1	RW
000843H	CAN1 - IF2 Command Mask register High (reserved)	IF2CMSKH1		R
000844H	CAN1 - IF2 Mask 1 Register Low	IF2MSK1L1	IF2MSK11	RW
000845H	CAN1 - IF2 Mask 1 Register High	IF2MSK1H1		RW

I/O map MB96(F)38x (30 / 31)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000846H	CAN1 - IF2 Mask 2 Register Low	IF2MSK2L1	IF2MSK21	RW
000847H	CAN1 - IF2 Mask 2 Register High	IF2MSK2H1		RW
000848H	CAN1 - IF2 Arbitration 1 Register Low	IF2ARB1L1	IF2ARB11	RW
000849H	CAN1 - IF2 Arbitration 1 Register High	IF2ARB1H1		RW
00084AH	CAN1 - IF2 Arbitration 2 Register Low	IF2ARB2L1	IF2ARB21	RW
00084BH	CAN1 - IF2 Arbitration 2 Register High	IF2ARB2H1		RW
00084CH	CAN1 - IF2 Message Control Register Low	IF2MCTRL1	IF2MCTR1	RW
00084DH	CAN1 - IF2 Message Control Register High	IF2MCTRH1		RW
00084EH	CAN1 - IF2 Data A1 Low	IF2DTA1L1	IF2DTA11	RW
00084FH	CAN1 - IF2 Data A1 High	IF2DTA1H1		RW
000850H	CAN1 - IF2 Data A2 Low	IF2DTA2L1	IF2DTA21	RW
000851H	CAN1 - IF2 Data A2 High	IF2DTA2H1		RW
000852H	CAN1 - IF2 Data B1 Low	IF2DTB1L1	IF2DTB11	RW
000853H	CAN1 - IF2 Data B1 High	IF2DTB1H1		RW
000854H	CAN1 - IF2 Data B2 Low	IF2DTB2L1	IF2DTB21	RW
000855H	CAN1 - IF2 Data B2 High	IF2DTB2H1		RW
000856H-00087FH	Reserved			-
000880H	CAN1 - Transmission Request 1 Register Low	TREQR1L1	TREQR11	R
000881H	CAN1 - Transmission Request 1 Register High	TREQR1H1		R
000882H	CAN1 - Transmission Request 2 Register Low	TREQR2L1	TREQR21	R
000883H	CAN1 - Transmission Request 2 Register High	TREQR2H1		R
000884H-00088FH	Reserved			-
000890H	CAN1 - New Data 1 Register Low	NEWDT1L1	NEWDT11	R
000891H	CAN1 - New Data 1 Register High	NEWDT1H1		R
000892H	CAN1 - New Data 2 Register Low	NEWDT2L1	NEWDT21	R
000893H	CAN1 - New Data 2 Register High	NEWDT2H1		R
000894H-00089FH	Reserved			-
0008A0H	CAN1 - Interrupt Pending 1 Register Low	INTPND1L1	INTPND11	R

I/O map MB96(F)38x (31 / 31)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0008A1H	CAN1 - Interrupt Pending 1 Register High	INTPND1H1		R
0008A2H	CAN1 - Interrupt Pending 2 Register Low	INTPND2L1	INTPND21	R
0008A3H	CAN1 - Interrupt Pending 2 Register High	INTPND2H1		R
0008A4H-0008AFH	Reserved			-
0008B0H	CAN1 - Message Valid 1 Register Low	MSGVAL1L1	MSGVAL11	R
0008B1H	CAN1 - Message Valid 1 Register High	MSGVAL1H1		R
0008B2H	CAN1 - Message Valid 2 Register Low	MSGVAL2L1	MSGVAL21	R
0008B3H	CAN1 - Message Valid 2 Register High	MSGVAL2H1		R
0008B4H-0008CDH	Reserved			-
0008CEH	CAN1 - Output enable register	COER1		RW
0008CFH-000BFFH	Reserved			-

■ INTERRUPT VECTOR TABLE

Interrupt vector table MB96(F)38x (1 / 3)

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
0	3FC	CALLV0	No	-	
1	3F8	CALLV1	No	-	
2	3F4	CALLV2	No	-	
3	3F0	CALLV3	No	-	
4	3EC	CALLV4	No	-	
5	3E8	CALLV5	No	-	
6	3E4	CALLV6	No	-	
7	3E0	CALLV7	No	-	
8	3DC	RESET	No	-	
9	3D8	INT9	No	-	
10	3D4	EXCEPTION	No	-	
11	3D0	NMI	No	-	Non-Maskable Interrupt
12	3CC	DLY	No	12	Delayed Interrupt
13	3C8	RC_TIMER	No	13	RC Timer
14	3C4	MC_TIMER	No	14	Main Clock Timer
15	3C0	SC_TIMER	No	15	Sub Clock Timer
16	3BC	RESERVED	No	16	Reserved
17	3B8	EXTINT0	Yes	17	External Interrupt 0
18	3B4	EXTINT1	Yes	18	External Interrupt 1
19	3B0	EXTINT2	Yes	19	External Interrupt 2
20	3AC	EXTINT3	Yes	20	External Interrupt 3
21	3A8	EXTINT4	Yes	21	External Interrupt 4
22	3A4	EXTINT5	Yes	22	External Interrupt 5
23	3A0	EXTINT6	Yes	23	External Interrupt 6
24	39C	EXTINT7	Yes	24	External Interrupt 7
25	398	CAN0	No	25	CAN Controller 0
26	394	CAN1*	No	26	CAN Controller 1
27	390	PPG0	Yes	27	Programmable Pulse Generator 0
28	38C	PPG1	Yes	28	Programmable Pulse Generator 1
29	388	PPG2	Yes	29	Programmable Pulse Generator 2
30	384	PPG3	Yes	30	Programmable Pulse Generator 3
31	380	PPG4	Yes	31	Programmable Pulse Generator 4
32	37C	PPG5	Yes	32	Programmable Pulse Generator 5

Interrupt vector table MB96(F)38x (2 / 3)

Vector number	Offset in vector ta-ble	Vector name	Cleared by DMA	Index in ICR to pro-gram	Description
33	378	PPG6	Yes	33	Programmable Pulse Generator 6
34	374	PPG7	Yes	34	Programmable Pulse Generator 7
35	370	RLT0	Yes	35	Reload Timer 0
36	36C	RLT1	Yes	36	Reload Timer 1
37	368	RLT2	Yes	37	Reload Timer 2
38	364	RLT3	Yes	38	Reload Timer 3
39	360	PPGRLT	Yes	39	Reload Timer 6 - dedicated for PPG
40	35C	ICU0	Yes	40	Input Capture Unit 0
41	358	ICU1	Yes	41	Input Capture Unit 1
42	354	ICU2	Yes	42	Input Capture Unit 2
43	350	ICU3	Yes	43	Input Capture Unit 3
44	34C	ICU4	Yes	44	Input Capture Unit 4
45	348	ICU5	Yes	45	Input Capture Unit 5
46	344	ICU6	Yes	46	Input Capture Unit 6
47	340	ICU7	Yes	47	Input Capture Unit 7
48	33C	OCU0	Yes	48	Output Compare Unit 0
49	338	OCU1	Yes	49	Output Compare Unit 1
50	334	OCU2	Yes	50	Output Compare Unit 2
51	330	OCU3	Yes	51	Output Compare Unit 3
52	32C	FRT0	Yes	52	Free Running Timer 0
53	328	FRT1	Yes	53	Free Running Timer 1
54	324	RTC0	No	54	Real Timer Clock
55	320	CAL0	No	55	Clock Calibration Unit
56	31C	SG0	No	56	Sound Generator 0
57	318	SG1	No	57	Sound Generator 1
58	314	IIC0	Yes	58	I2C interface
59	310	ADC0	Yes	59	A/D Converter
60	30C	ALARM0	No	60	Alarm Comparator 0
61	308	ALARM1*	No	61	Alarm Comparator 1
62	304	LINR0	Yes	62	LIN USART 0 RX
63	300	LINT0	Yes	63	LIN USART 0 TX
64	2FC	LINR1	Yes	64	LIN USART 1 RX
65	2F8	LINT1	Yes	65	LIN USART 1 TX
66	2F4	LINR2	Yes	66	LIN USART 2 RX
67	2F0	LINT2	Yes	67	LIN USART 2 TX

Interrupt vector table MB96(F)38x (3 / 3)

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
68	2EC	LINR4	Yes	68	LIN USART 4 RX
69	2E8	LINT4	Yes	69	LIN USART 4 TX
70	2E4	LINR5	Yes	70	LIN USART 5 RX
71	2E0	LINT5	Yes	71	LIN USART 5 TX
72	2DC	FLASH_A	No	72	Flash memory A (only Flash devices)
73	2D8	FLASH_B	No	73	Flash memory B (only MB96F388/F389)

*:   ALARM1 and CAN1 are not included on MB96384 and MB96(F)385 devices

■ HANDLING DEVICES

Special care is required for the following when handling the device:

- Latch-up prevention
- Unused pins handling
- External clock usage
- Unused sub clock signal
- Notes on PLL clock mode operation
- Power supply pins (Vcc/Vss)
- Crystal oscillator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on energization
- Stabilization of power supply voltage
- SMC power supply pins

1. Latch-up prevention

- CMOS IC chips may suffer latch-up under the following conditions:

  - A voltage higher than Vcc or lower than Vss is applied to an input or output pin.
  - A voltage higher than the rated voltage is applied between Vcc and Vss.
  - The AVcc power supply is applied before the Vcc voltage.

- Latch-up may increase the power supply current dramatically, causing thermal damages to the device.

- For the same reason, extra care is required to not let the analog power-supply voltage (AVcc, AVRH) exceed the digital power-supply voltage.

2. Unused pins handling
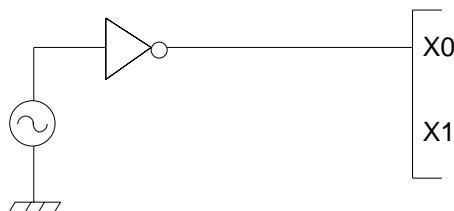
- Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register PIER = 0).

- Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. They must therefore be pulled up or pulled down through resistors. To prevent latch-up, those resistors should be more than 2 kΩ.

- Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

3. External clock usage

- The permitted frequency range of an external clock depends on the oscillator type and configuration. See AC Characteristics for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:
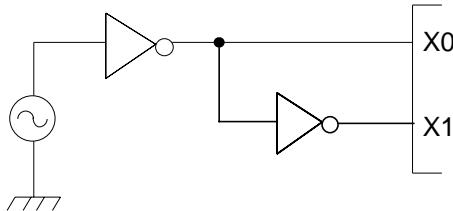
  #### 1. Single phase external clock

- When using a single phase external clock, X0 pin must be driven and X1 pin left open.

  #### 2. Opposite phase external clock

- When using an opposite phase external clock, X1 (X1A) must be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins.

4. Unused sub clock signal

- If the pins X0A and X1A are not connected to an oscillator, a pull-down resistor must be connected on the X0A pin and the X1A pin must be left open.

5. Notes on PLL clock mode operation

- If the PLL clock mode is selected and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

6. Power supply pins (V$_{CC}$/V$_{SS}$)

- It is required that all V$_{CC}$-level as well as all V$_{SS}$-level power supply pins are at the same potential. If there is more than one V$_{CC}$ or V$_{SS}$ level, the device may operate incorrectly or be damaged even within the guaranteed operating range.
- V$_{CC}$ and V$_{SS}$ must be connected to the device from the power supply with lowest possible impedance.
- As a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1 μF between V$_{CC}$ and V$_{SS}$ as close as possible to V$_{CC}$ and V$_{SS}$ pins.

7. Crystal oscillator circuit

- Noise at X0 or X1 pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.
- It is highly recommended to provide a printed circuit board art work surrounding X0 and X1 pins with a ground area for stabilizing the operation.
- It is highly recommended to evaluate the quartz/MCU system at the quartz manufacturer.

8. Turn on sequence of power supply to A/D converter and analog inputs

- It is required to turn the A/D converter power supply (AV$_{CC}$, AVRH, AVRL) and analog inputs (ANn) on after turning the digital power supply (V$_{CC}$) on.
- It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, the voltage must not exceed AVRH or AV$_{CC}$ (turning the analog and digital power supplies simultaneously on or off is acceptable).

9. Pin handling when not using the A/D converter

- It is required to connect the unused pins of the A/D converter as AV$_{CC}$ = V$_{CC}$, AV$_{SS}$ = AVRH = AVRL = V$_{SS}$.

10. Notes on energization

- To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50μs from 0.2 V to 2.7 V.

11. Stabilization of power supply voltage

- If the power supply voltage varies acutely even within the operation safety range of the Vcc power supply voltage, a malfunction may occur. The Vcc power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that Vcc ripple fluctuations (peak to peak value) in the commercial frequencies (50 to 60 Hz) fall within 10% of the standard Vcc power supply voltage and the transient fluctuation rate becomes 0.1V/µs or less in instantaneous fluctuation for power supply switching.

12. SMC power supply pins

- All DVss pins must be set to the same level as the Vss pins.

- The DVcc power supply level can be set independently of the Vcc power supply level. However note that the SMC I/O pin state is undefined if DVcc is powered on and Vcc is below 3V. To avoid this, we recommend to always power Vcc before DVcc.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

Parameter	Symbol	Rating		Unit	Remarks
		Min	**Max**		
Power supply voltage	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	
	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_{CC} = AV_{CC}$ [*1]
AD Converter voltage references	AVRH, AVRL	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$AV_{CC} \geq AVRH$, $AV_{CC} \geq AVRL$, $AVRH > AVRL$, $AVRL \geq AV_{SS}$
SMC Power supply	DV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	See [*7]
LCD power supply voltage	V0 to V3	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	V0 to V3 must not exceed V_{CC}
Input voltage	V_I	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_I \leq (D)V_{CC} + 0.3V$ [*2]
Output voltage	V_O	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_O \leq (D)V_{CC} + 0.3V$ [*2]
Maximum Clamp Current	I_{CLAMP}	-4.0	+4.0	mA	Applicable to general purpose I/O pins [*3]
Total Maximum Clamp Current	$\Sigma\|I_{CLAMP}\|$	-	40	mA	Applicable to general purpose I/O pins [*3]
"L" level maximum output current	I_{OL1}	-	15	mA	Normal outputs with driving strength set to 5mA
	I_{OLSMC}	-	40	mA	High current outputs with driving strength set to 30mA
"L" level average output current	I_{OLAV1}	-	5	mA	Normal outputs with driving strength set to 5mA
	$I_{OLAVSMC}$	-	30	mA	High current outputs with driving strength set to 30mA
"L" level maximum overall output current	ΣI_{OL1}	-	100	mA	Normal outputs
	ΣI_{OLSMC}	-	330	mA	High current outputs
"L" level average overall output current	ΣI_{OLAV1}	-	50	mA	Normal outputs
	$\Sigma I_{OLAVSMC}$	-	250	mA	High current outputs
"H" level maximum output current	I_{OH1}	-	-15	mA	Normal outputs with driving strength set to 5mA
	I_{OHSMC}	-	-40	mA	High current outputs with driving strength set to 30mA
"H" level average output current	I_{OHAV1}	-	-5	mA	Normal outputs with driving strength set to 5mA
	$I_{OHAVSMC}$	-	-30	mA	High current outputs with driving strength set to 30mA

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
"H" level maximum overall output current	ΣI_{OH1}	-	-100	mA	Normal outputs
	ΣI_{OHSMC}	-	-330	mA	High current outputs
"H" level average overall output current	ΣI_{OHAV1}	-	-50	mA	Normal outputs
	ΣI_{OHASMC}	-	-250	mA	High current outputs
Permitted Power dissipation (Flash devices) [4]	P_D	-	370[5]	mW	$T_A=105^oC$
		-	740[5]	mW	$T_A=85^oC$
		-	1000[5]	mW	$T_A=70^oC$
		-	460[5]	mW	$T_A=125^oC$, no Flash program/erase [6]
		-	800[5]	mW	$T_A=105^oC$, no Flash program/erase [6]
Permitted Power dissipation (Mask ROM devices) [4]	P_D	-	310[5]	mW	$T_A=105^oC$
		-	625[5]	mW	$T_A=85^oC$
		-	800[5]	mW	$T_A=70^oC$
		-	390[5]	mW	$T_A=125^oC$ [6]
		-	700[5]	mW	$T_A=105^oC$ [6]
Operating ambient temperature	T_A	0	+70	^oC	MB96V300B
		-40	+105		
		-40	+125		[6]
Storage temperature	T_{STG}	-55	+150	^oC	

*1: AV_{CC} and V_{CC} must be set to the same voltage. It is required that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} neither when the power is switched on.
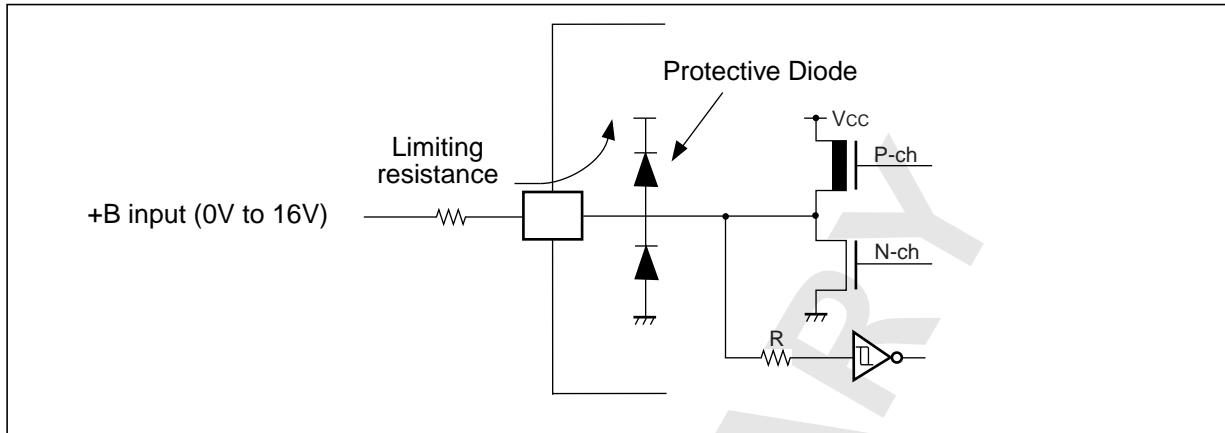
*2: V_I and V_O should not exceed $(D)V_{CC}$ + 0.3 V. V_I should also not exceed the specified ratings. However if the maximum current to/from a input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating. Input/output voltages of high current ports depend on DV_{CC}. Input/output voltages of standard ports depend on V_{CC}.

*3: • Applicable to all general purpose I/O pins (Pnn_m) except I/O pins with SEG or COM functionality.
• Use within recommended operating conditions.
• Use at DC voltage (current)
• The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
• The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
• Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the VCC pin, and this may affect other devices.
• Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
• Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset (except devices with persistent low voltage

reset in internal vector mode).
- No +B signal must be applied to any LCD I/O pin (including unused SEG/COM pins).

- Sample recommended circuits:

*4: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.
The actual power dissipation depends on the customer application and can be calculated as follows:
$P_D = P_{IO} + P_{INT}$
$P_{IO} = \sum (V_{OL} * I_{OL} + V_{OH} * I_{OH})$ (IO load power dissipation, sum is performed on all IO ports)
$P_{INT} = V_{CC} * (I_{CC} + I_A)$ (internal power dissipation)
I_{CC} is the total core current consumption into V_{CC} as described in the "DC characteristics" and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming or the clock modulator.
I_A is the analog current consumption into AV_{CC}.

*5: Worst case value for a package mounted on single layer PCB at specified T_A without air flow.

*6: Please contact Fujitsu for reliability limitations when using under these conditions.

*7: If DV_{CC} is powered before V_{CC}, then SMC I/O pins state is undefined. To avoid this, we recommend to always power V_{CC} before DV_{CC}. It is not necessary to set V_{CC} and DV_{CC} to the same value.

2. Recommended Conditions

Parameter	Symbol	Value			Unit	Remarks
		Min	**Typ**	**Max**		
Power supply voltage	V_{CC}, DV_{CC}	3.0	-	5.5	V	
Smoothing capacitor at C pin	C_S	4.7	-	10	μF	Use a low inductance capacitor (for example X7R ceramic capacitor)

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the devices electrical characteristics are guaranteed when the device is operated within these ranges.

Semiconductor devices must always be operated within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC characteristics

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, DV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input "H" voltage	V_{IH}	Port inputs Pnn_m	CMOS Hysteresis 0.8/0.2 input selected	0.8 V_{CC}	-	(D)V_{CC} + 0.3	V	
			CMOS Hysteresis 0.7/0.3 input selected	0.7 V_{CC}	-	(D)V_{CC} + 0.3	V	(D)$V_{CC} \geq 4.5$V
				0.74 V_{CC}	-	(D)V_{CC} + 0.3	V	(D)$V_{CC} < 4.5$V
			AUTOMOTIVE Hysteresis input selected	0.8 V_{CC}	-	(D)V_{CC} + 0.3	V	
			TTL input selected	2.0	-	(D)V_{CC} + 0.3	V	
	V_{IHX0F}	X0	External clock in "Fast Clock Input mode"	0.8 V_{CC}	-	V_{CC} + 0.3	V	Not available in MB96F386xxA/ F387xxA
	V_{IHX0S}	X0,X1, X0A,X1A	External clock in "oscillation mode"	2.5	-	V_{CC} + 0.3	V	
	V_{IHR}	RSTX	-	0.8 V_{CC}	-	V_{CC} + 0.3	V	CMOS Hysteresis input
	V_{IHM}	MD2-MD0	-	V_{CC} - 0.3	-	V_{CC} + 0.3	V	
Input "L" voltage	V_{IL}	Port inputs Pnn_m	CMOS Hysteresis 0.8/0.2 input selected	V_{SS} - 0.3	-	0.2 (D)V_{CC}	V	
			CMOS Hysteresis 0.7/0.3 input selected	V_{SS} - 0.3	-	0.3 (D)V_{CC}	V	
			AUTOMOTIVE Hysteresis input selected	V_{SS} - 0.3	-	0.5 (D)V_{CC}	V	(D)$V_{CC} \geq 4.5$V
				V_{SS} - 0.3	-	0.46 (D)V_{CC}		(D)$V_{CC} < 4.5$V
			TTL input selected	V_{SS} - 0.3	-	0.8	V	
	V_{ILX0F}	X0	External clock in "Fast Clock Input mode"	V_{SS} - 0.3	-	0.2 V_{CC}	V	Not available in MB96F386xxA/ F387xxA
	V_{ILX0S}	X0,X1, X0A,X1A	External clock in "oscillation mode"	V_{SS} - 0.3	-	0.5	V	
	V_{ILR}	RSTX	-	V_{SS} - 0.3	-	0.2 V_{CC}	V	CMOS Hysteresis input
	V_{ILM}	MD2-MD0	-	V_{SS} - 0.3	-	V_{SS} + 0.3	V	

$(T_A = -40°C \text{ to } 125°C, V_{CC} = AV_{CC} = 3.0V \text{ to } 5.5V, DV_{CC} = 3.0V \text{ to } 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V)$

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Output "H" voltage	V_{OH2}	Normal and High Current outputs	$4.5V \leq (D)V_{CC} \leq 5.5V$ $I_{OH} = -2mA$ $3.0V \leq (D)V_{CC} < 4.5V$ $I_{OH} = -1.6mA$	$(D)V_{CC} - 0.5$	-	-	V	Driving strength set to 2mA
	V_{OH5}	Normal and High Current outputs	$4.5V \leq (D)V_{CC} \leq 5.5V$ $I_{OH} = -5mA$ $3.0V \leq (D)V_{CC} < 4.5V$ $I_{OH} = -3mA$	$(D)V_{CC} - 0.5$	-	-	V	Driving strength set to 5mA
	V_{OH30}	High current outputs	$4.5V \leq DV_{CC} \leq 5.5V$ $I_{OH} = -30mA$ $3.0V \leq DV_{CC} < 4.5V$ $I_{OH} = -20mA$	$DV_{CC} - 0.5$	-	-	V	Driving strength set to 30mA
	V_{OH3}	I²C outputs	$4.5V \leq V_{CC} \leq 5.5V$ $I_{OH} = -3mA$ $3.0V \leq V_{CC} < 4.5V$ $I_{OH} = -2mA$	$V_{CC} - 0.5$	-	-	V	
Output "L" voltage	V_{OL2}	Normal and High Current outputs	$4.5V \leq (D)V_{CC} \leq 5.5V$ $I_{OL} = +2mA$ $3.0V \leq (D)V_{CC} < 4.5V$ $I_{OL} = +1.6mA$	-	-	0.4	V	Driving strength set to 2mA
	V_{OL5}	Normal and High Current outputs	$4.5V \leq (D)V_{CC} \leq 5.5V$ $I_{OL} = +5mA$ $3.0V \leq (D)V_{CC} < 4.5V$ $I_{OL} = +3mA$	-	-	0.4	V	Driving strength set to 5mA
	V_{OL30}	High current outputs	$4.5V \leq DV_{CC} \leq 5.5V$ $I_{OL} = +30mA$ $3.0V \leq DV_{CC} < 4.5V$ $I_{OL} = +20mA$	-	-	0.5	V	Driving strength set to 30mA
	V_{OL3}	I²C outputs	$4.5V \leq V_{CC} \leq 5.5V$ $I_{OL} = +3mA$ $3.0V \leq V_{CC} < 4.5V$ $I_{OL} = +2mA$	-	-	0.4	V	
Input leak current	I_{IL}	Pnn_m	$DV_{CC} = V_{CC} = 5.5V$ $V_{SS} < V_I < V_{CC}$	-1	-	+1	µA	

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, DV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Total LCD leakage current	ΣI_{ILCD}	all SEG/COM pins	V_{CC} = 5.0V	-10	0.5	10	μA	Maximum leakage current of all LCD pins
Internal LCD divide resistance	R_{LCD}	Between V3 and Vss		25	35	50	kΩ	
Pull-up resistance	R_{UP}	Pnn_m, RSTX	-	25	50	100	kΩ	

Note: Input/output voltages of high current ports depend on DV_{CC}, of other ports on V_{CC}.

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, DV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V)

Parameter	Symbol	Condition	Value			temp	Remarks
			Typ	Max	Unit		
Power supply current in Run modes*	I_{CCPLL}	PLL Run mode with CLKS1/2 = 48MHz, CLKB = CLKP1/2 = 24MHz	35	44	mA	25˚C	CLKRC and CLKSC stopped. Core voltage at 1.9V
			36	47		125˚C	0 Flash/ROM wait states
		PLL Run mode with CLKS1/2 = CLKB = CLKP1=56MHz, CLKP2 = 28MHz	44	57	mA	25˚C	CLKRC and CLKSC stopped. Core voltage at 1.9V
			45	60		125˚C	2 Flash/ROM wait states (not for MB96F385/F388/F389)
		PLL Run mode with CLKS1/2 = 96MHz, CLKB = CLKP1= 48MHz, CLKP2 = 24MHz	49	62	mA	25˚C	CLKRC and CLKSC stopped. Core voltage at 1.9V
			50	65		125˚C	1 Flash/ROM wait state MB96384/385
		PLL Run mode with CLKS1/2 = 80MHz, CLKB = CLKP1 = 40MHz, CLKP2 = 20MHz	42	55	mA	25˚C	CLKRC and CLKSC stopped. Core voltage at 1.9V
			43	58		125˚C	1 Flash/ROM wait state MB96F385/F388/F389
		PLL Run mode with CLKS1/2 = 72MHz, CLKB = CLKP1 = 36MHz, CLKP2 = 18MHz	38	50	mA	25˚C	CLKRC and CLKSC stopped. Core voltage at 1.9V
			39	53		125˚C	1 Flash/ROM wait state MB96F386/F387
	I_{CCMAIN}	Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4MHz	4.5	5.5	mA	25˚C	CLKPLL, CLKSC and CLKRC stopped
			5.1	8.5		125˚C	1 Flash/ROM wait state
	I_{CCRCH}	RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 2MHz	2.9	4	mA	25˚C	CLKMC, CLKPLL and CLKSC stopped
			3.5	6.5		125˚C	1 Flash/ROM wait state

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, DV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V)

Parameter	Symbol	Condition	Value			temp	Remarks
			Typ	Max	Unit		
Power supply current in Run modes*	I_{CCRCL}	RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 100kHz, SMCR:LPMS = 0	0.4	0.6	mA	25˚C	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode
			0.9	3.5		125˚C	1 Flash/ROM wait state
		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 100kHz, SMCR:LPMS = 1	0.15	0.25	mA	25˚C	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode, no Flash programming/erasing allowed.
			0.65	3.2		125˚C	1 Flash/ROM wait state
	I_{CCSUB}	Sub Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32kHz	0.1	0.2	mA	25˚C	CLKMC, CLKPLL and CLKRC stopped, no Flash programming/erasing allowed.
			0.6	3		125˚C	1 Flash/ROM wait state

(T$_A$ = -40˚C to 125˚C, V$_{CC}$ = AV$_{CC}$ = 3.0V to 5.5V, DV$_{CC}$ = 3.0V to 5.5V, V$_{SS}$ = AV$_{SS}$ = DV$_{SS}$ = 0V)

Parameter	Symbol	Condition	Value			temp	Remarks
			Typ	Max	Unit		
Power supply current in Sleep modes*	I$_{CCSPLL}$	PLL Sleep mode with CLKS1/2 = 48MHz, CLKP1/2 = 24MHz	9	10.5	mA	25˚C	CLKRC and CLKSC stopped. Core voltage at 1.9V
			9.7	13		125˚C	
		PLL Sleep mode with CLKS1/2 = CLKP1= 56MHz, CLKP2 = 28MHz	14	15.5	mA	25˚C	CLKRC and CLKSC stopped. Core voltage at 1.9V
			14.8	18		125˚C	(not for MB96F385/F388/F389)
		PLL Sleep mode with CLKS1/2 = 96MHz, CLKP1= 48MHz, CLKP2 = 24MHz	14	15.5	mA	25˚C	CLKRC and CLKSC stopped. Core voltage at 1.9V
			14.8	18		125˚C	MB96384/385
		PLL Sleep mode with CLKS1/2 = 80MHz, CLKP1 = 40MHz, CLKP2 = 20MHz	11.7	13.2	mA	25˚C	CLKRC and CLKSC stopped. Core voltage at 1.9V
			12.5	15.7		125˚C	MB96F385/F388/F389
		PLL Sleep mode with CLKS1/2 = 72MHz, CLKP1 = 36MHz, CLKP2 = 18MHz	10.5	12	mA	25˚C	CLKRC and CLKSC stopped. Core voltage at 1.9V
			11.3	14.5		125˚C	MB96F386/F387
	I$_{CCSMAIN}$	Main Sleep mode with CLKS1/2 = CLKP1/2 = 4MHz	1.5	1.8	mA	25˚C	CLKPLL, CLKSC and CLKRC stopped
			2	4.5		125˚C	
	I$_{CCSRCH}$	RC Sleep mode with CLKS1/2 = CLKP1/2 = 2MHz	0.8	1.3	mA	25˚C	CLKMC, CLKPLL and CLKSC stopped
			1.4	4		125˚C	

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, DV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V)

Parameter	Symbol	Condition	Value			temp	Remarks
			Typ	Max	Unit		
Power supply current in Sleep modes*	I_{CCSRCL}	RC Sleep mode with CLKS1/2 = CLKP1/2 = 100kHz, SMCR:LPMSS = 0	0.3	0.5	mA	25°C	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode
			0.8	3.4		125°C	
		RC Sleep mode with CLKS1/2 = CLKP1/2 = 100kHz, SMCR:LPMSS = 1	0.06	0.15	mA	25°C	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode
			0.56	3		125°C	
	I_{CCSSUB}	Sub Sleep mode with CLKS1/2 = CLKP1/2 = 32kHz	0.04	0.12	mA	25°C	CLKMC, CLKPLL and CLKRC stopped
			0.54	2.9		125°C	

$(T_A = -40°C \text{ to } 125°C, V_{CC} = AV_{CC} = 3.0V \text{ to } 5.5V, DV_{CC} = 3.0V \text{ to } 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V)$

Parameter	Symbol	Condition	Value			temp	Remarks
			Typ	Max	Unit		
Power supply current in Timer modes*	I_{CCTPLL}	PLL Timer mode with CLKMC = 4MHz, CLK-PLL = 48MHz	1.6	2	mA	25°C	CLKRC and CLKSC stopped. Core voltage at 1.9V
			2.1	4.8		125°C	
	$I_{CCTMAIN}$	Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 0	0.35	0.5	mA	25°C	CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in high power mode
			0.85	3.3		125°C	
		Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 1	0.1	0.15	mA	25°C	CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in low power mode
			0.6	2.9		125°C	
	I_{CCTRCH}	RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 0	0.35	0.5	mA	25°C	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode
			0.85	3.3		125°C	
		RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 1	0.1	0.15	mA	25°C	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode
			0.6	2.9		125°C	
	I_{CCTRCL}	RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 0	0.3	0.45	mA	25°C	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode
			0.8	3.2		125°C	
		RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 1	0.05	0.1	mA	25°C	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode
			0.55	2.8		125°C	

(T$_A$ = -40˚C to 125˚C, V$_{CC}$ = AV$_{CC}$ = 3.0V to 5.5V, DV$_{CC}$ = 3.0V to 5.5V, V$_{SS}$ = AV$_{SS}$ = DV$_{SS}$ = 0V)

Parameter	Symbol	Condition	Value			temp	Remarks
			Typ	Max	Unit		
Power supply current in Timer modes*	I$_{CCTSUB}$	Sub Timer mode with CLKSC = 32kHz	0.03	0.1	mA	25˚C	CLKMC, CLKPLL and CLKRC stopped
			0.53	2.8		125˚C	
Stop Mode	I$_{CCH}$	VRCR:LPMB[2:0] = "110"	0.02	0.08	mA	25˚C	Core voltage at 1.8V
			0.52	2.8		125˚C	
		VRCR:LPMB[2:0] = "000"	0.015	0.06	mA	25˚C	Core voltage at 1.2V
			0.4	2.3		125˚C	
Power supply current for active Low Voltage detector	I$_{CCLVD}$	Low voltage detector enabled (RCR:LVDE='1')	90	140	µA	25˚C	This current must be added to all Power supply currents above
			100	150		125˚C	
Clock modulator current	I$_{CCCLOMO}$	Clock modulator enabled (CMCR:PDX = '1')	3	4.5	mA	-	Must be added to all current above
Flash Write/Erase current	I$_{CCFLASH}$	Current for one Flash module	15	40	mA	-	Must be added to all current above
Input capacitance	C$_{IN}$	-	15	30	pF		High current outputs
Input capacitance	C$_{IN}$	-	5	15	pF		Other than C, AV$_{CC}$, AV$_{SS}$, AVRH, AVRL, V$_{CC}$, V$_{SS}$, DV$_{CC}$, DV$_{SS}$, High current outputs

* The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. See chapter "Standby mode and voltage regulator control circuit" of the Hardware Manual for further details about voltage regulator control.
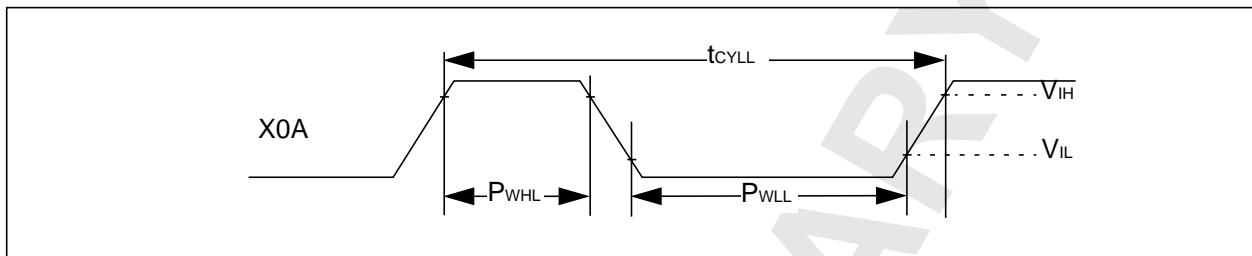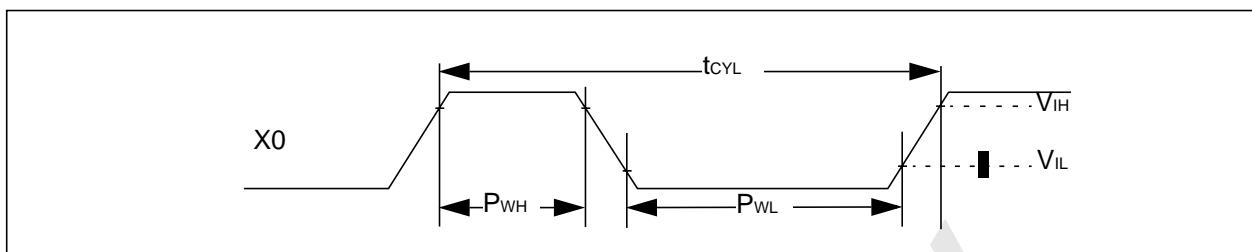
4. AC Characteristics

Source Clock timing
(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, DV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	-	16	MHz	When using an oscillation circuit, PLL off
			0	-	16	MHz	When using an opposite phase external clock, PLL off
			3.5	-	16	MHz	When using an oscillation circuit or opposite phase external clock, PLL on
Clock frequency	f_{FCI}	X0	0	-	56	MHz	When using a single phase external clock in "Fast Clock Input mode" (not available in MB96F386xxA and MB96F387xxA), PLL off
			3.5	-	56	MHz	When using a single phase external clock in "Fast Clock Input mode" (not available in MB96F386xxA and MB96F387xxA), PLL on
Clock frequency	f_{CL}	X0A, X1A	32	32.768	100	kHz	When using an oscillation circuit
			0	-	100	kHz	When using an opposite phase external clock
		X0A	0	-	50	kHz	When using a single phase external clock
Clock frequency	f_{CR}	-	50	100	200	kHz	When using slow frequency of RC oscillator
			1	2	4	MHz	When using fast frequency of RC oscillator
Clock frequency	f_{CLKVCO}	-	50	-	200	MHz	Permitted VCO output frequency of PLL (CLKVCO)
Input clock pulse width	P_{WH}, P_{WL}	X0,X1	8	-	-	ns	Duty ratio is about 30% to 70%
Input clock pulse width	P_{WHL}, P_{WLL}	X0A,X1A	5	-	-	µs	

Internal Clock timing

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, DV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V)
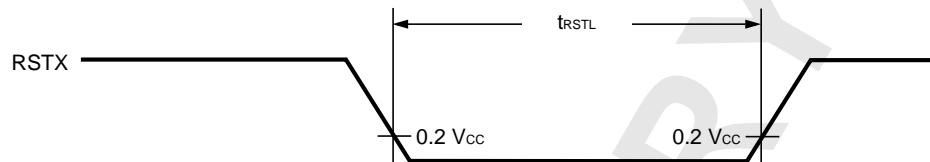
Parameter	Symbol	Core Voltage Settings				Unit	Remarks
		1.8V		1.9V			
		Min	Max	Min	Max		
Internal System clock frequency (CLKS1 and CLKS2)	f_{CLKS1}, f_{CLKS2}	0	92	0	96	MHz	Others than below
		0	72	0	80	MHz	MB96F385/F388/F389
		0	68	0	74	MHz	MB96F386/F387
Internal CPU clock frequency (CLKB), internal peripheral clock frequency (CLKP1)	f_{CLKB}, f_{CLKP1}	0	52	0	56	MHz	Others than below
		0	36	0	40	MHz	MB96F385/F388/F389
Internal peripheral clock frequency (CLKP2)	f_{CLKP2}	0	28	0	32	MHz	Others than below
		0	26	0	28	MHz	MB96F386/F387

External Reset timing

(T$_A$ = -40°C to 125°C, V$_{CC}$ = AV$_{CC}$ = 3.0V to 5.5V, DV$_{CC}$ = 3.0V to 5.5V, V$_{SS}$ = AV$_{SS}$ = DV$_{SS}$ = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Reset input time	t$_{RSTL}$	RSTX	500	-	-	ns	
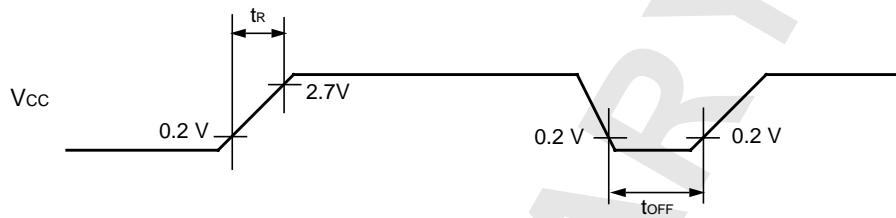
Power On Reset timing

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, DV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Power on rise time	t_R	Vcc	0.05	-	30	ms	
Power off time	t_{OFF}	Vcc	1	-	-	ms	

If the power supply is changed too rapidly, a power-on reset may occur.
We recommend a smooth startup by restraining voltages when changing the power supply voltage during operation, as shown in the figure below.
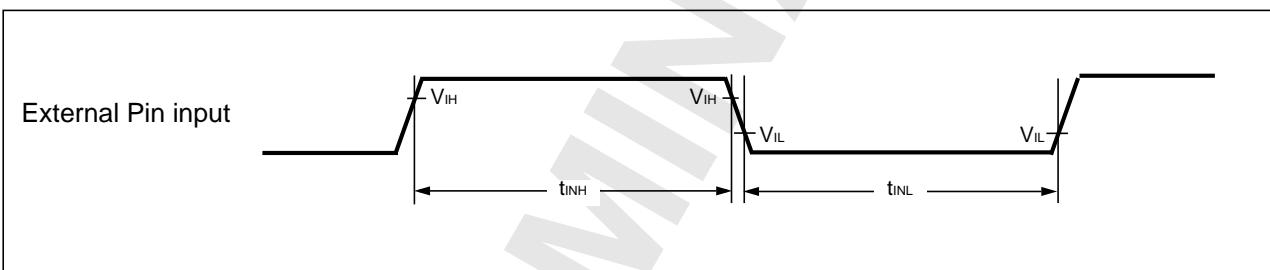
PRELIMINARY

External Input timing

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, DV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V)

Parameter	Symbol	Pin	Condition	Value		Unit	Used Pin input function
				Min	Max		
Input pulse width	t_{INH} t_{INL}	INTn	—	200	—	ns	External Interrupt
		NMI					NMI
		Pnn_m		$2*t_{CLKP1} + 200$ ($t_{CLKP1}=1/f_{CLKP1}$)	—	ns	General Purpose IO
		TINn					Reload Timer
		TTGn					PPG Trigger input
		ADTG					AD Converter Trigger
		FRCKn					Free Running Timer external clock
		INn					Input Capture

Note : Relocated Resource Inputs have same characteristics

External Pin input V_{IH} V_{IH} V_{IL} V_{IL} t_{INH} t_{INL}
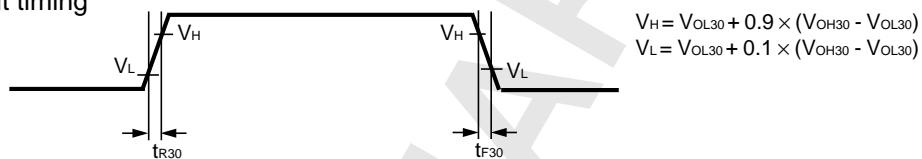
Slew Rate High Current Outputs

$(T_A = -40°C \text{ to } 125°C, V_{CC} = AV_{CC} = 3.0V \text{ to } 5.5V, DV_{CC} = 3.0V \text{ to } 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V)$

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Output rise/fall time	t_{R30} t_{F30}	I/O circuit type M	Output driving strength set to "30mA"	15	—	ns	

Note : Relocated Resource Inputs have same characteristics

- Slew rate output timing

$V_H = V_{OL30} + 0.9 \times (V_{OH30} - V_{OL30})$
$V_L = V_{OL30} + 0.1 \times (V_{OH30} - V_{OL30})$

External Bus timing

WARNING: The values given below are for an I/O driving strength IO_{drive} = 5mA. If IO_{drive} is 2mA, all the maximum output timing described in the different tables must then be increased by 10ns.

Basic Timing
$(T_A = -40\ °C\ to\ +125\ °C,\ V_{CC} = 5.0\ V \pm 10\%,\ V_{SS} = 0.0\ V,\ IO_{drive} = 5mA,\ C_L = 50pF)$
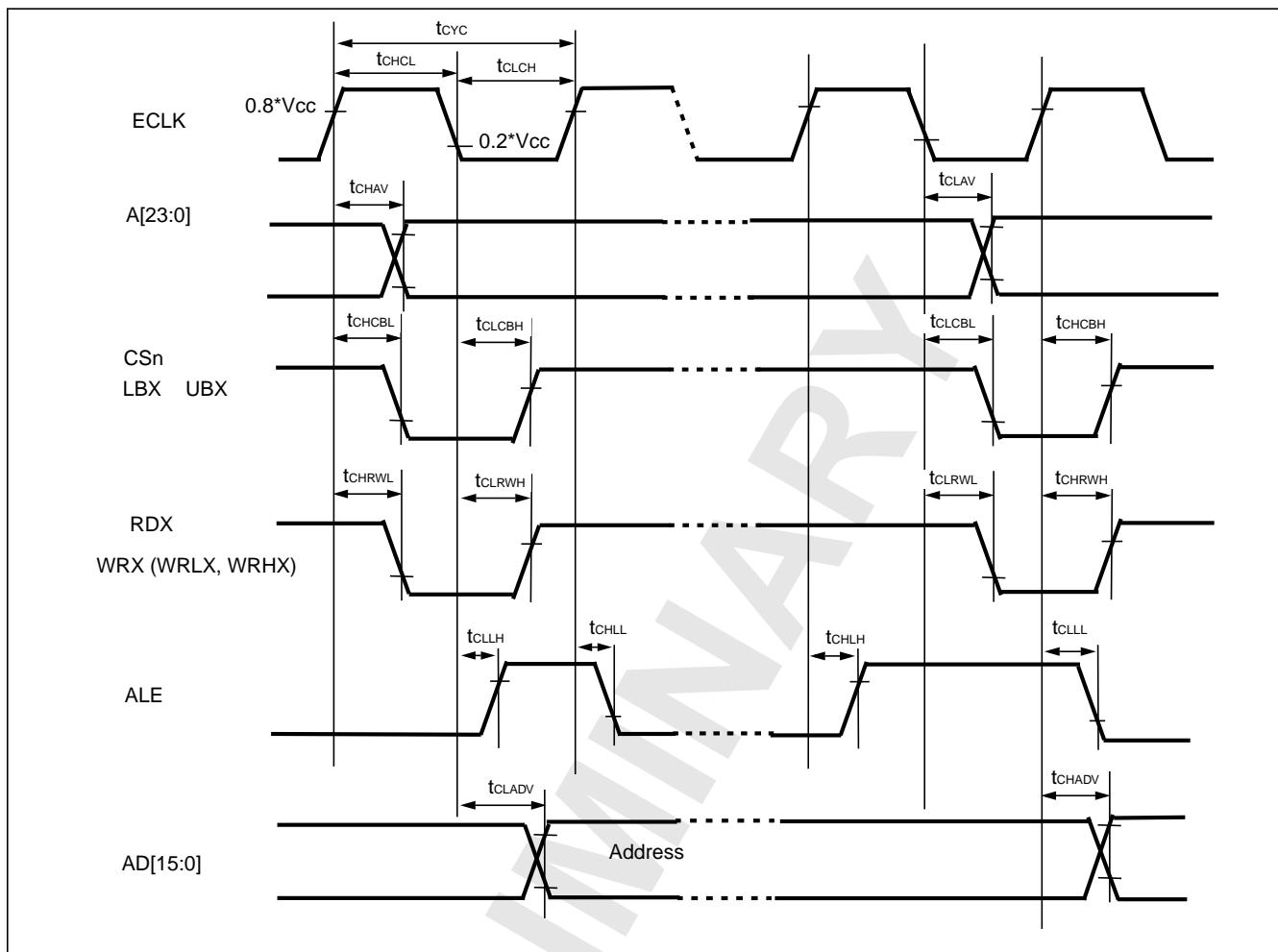
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ECLK	t_{CYC}	ECLK	—	25	—	ns	
	t_{CHCL}			t_{CYC}/2-5	t_{CYC}/2+5		
	t_{CLCH}			t_{CYC}/2-5	t_{CYC}/2+5		
ECLK → UBX/ LBX / CSn time	t_{CHCBH}	CSn, UBX, LBX, ECLK	—	-20	20	ns	
	t_{CHCBL}			-20	20		
	t_{CLCBH}			-20	20		
	t_{CLCBL}			-20	20		
ECLK → ALE time	t_{CHLH}	ALE, ECLK	—	-10	10	ns	
	t_{CHLL}			-10	10		
	t_{CLLH}			-10	10		
	t_{CLLL}			-10	10		
ECLK → address valid time (non-multiplexed)	t_{CHAV}	A[23:0], ECLK	EBM:NMS=1	-15	15	ns	
	t_{CLAV}			-15	15		
ECLK → address valid time (multiplexed)	t_{CHAV}	A[23:16], ECLK	EBM:NMS=0	-15	15	ns	
	t_{CLAV}			-15	15		
	t_{CLADV}	AD[15:0], ECLK	EBM:NMS=0	-15	15	ns	
	t_{CHADV}			-15	15		
ECLK → RDX /WRX time	t_{CHRWH}	RDX, WRX, WRLX,WRHX, ECLK	—	-10	10	ns	
	t_{CHRWL}			-10	10		
	t_{CLRWH}			-10	10		
	t_{CLRWL}			-10	10		

$(T_A = -40\ °C\ to\ +125\ °C,\ V_{CC} = 3.0\ to\ 4.5V,\ V_{SS} = 0.0\ V,\ IO_{drive} = 5mA,\ C_L = 50pF)$

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ECLK	t_{CYC}	ECLK	—	30	—	ns	
	t_{CHCL}			t_{CYC}/2-8	t_{CYC}/2+8		
	t_{CLCH}			t_{CYC}/2-8	t_{CYC}/2+8		

(T$_A$ = −40 °**C to** +125 °**C,** V$_{CC}$ = 3.0 to 4.5V, V$_{SS}$ = 0.0 V, IO$_{drive}$ = 5mA, C$_L$ = 50pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ECLK → UBX/ LBX / CSn time	t$_{CHCBH}$	CSn, UBX, LBX, ECLK	—	-25	25	ns	
	t$_{CHCBL}$			-25	25		
	t$_{CLCBH}$			-25	25		
	t$_{CLCBL}$			-25	25		
ECLK → ALE time	t$_{CHLH}$	ALE, ECLK	—	-15	15	ns	
	t$_{CHLL}$			-15	15		
	t$_{CLLH}$			-15	15		
	t$_{CLLL}$			-15	15		
ECLK → address valid time (non-multiplexed)	t$_{CHAV}$	A[23:0], ECLK	EBM:NMS=1	-20	20	ns	
	t$_{CLAV}$			-20	20		
ECLK → address valid time (multiplexed)	t$_{CHAV}$	A[23:16], ECLK	EBM:NMS=0	-20	20	ns	
	t$_{CLAV}$			-20	20		
	t$_{CLADV}$	AD[15:0], ECLK	EBM:NMS=0	-20	20	ns	
	t$_{CHADV}$			-20	20		
ECLK → RDX /WRX time	t$_{CHRWH}$	RDX, WRX, WRLX, WRHX, ECLK	—	-15	15	ns	
	t$_{CHRWL}$			-15	15		
	t$_{CLRWH}$			-15	15		
	t$_{CLRWL}$			-15	15		

Refer to the Hardware Manual for detailed Timing Charts.

Bus Timing (Read)

($T_A = -40\ °C$ **to** $+125\ °C$**,** $V_{CC} = 5.0\ V \pm 10\%$**,** $V_{SS} = 0.0\ V$, $IO_{drive} = 5mA$, $C_L = 50pF$)

Parameter	Sym-bol	Pin	Conditions	Value Min	Value Max	Unit	Remarks
ALE pulse width (multiplexed)	t_{LHLL}	ALE	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 5$	—	ns	
			EACL:STS=1	$t_{CYC} - 5$	—		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 5$	—		
Valid address $\Rightarrow$ ALE $\downarrow$ time (multiplexed)	t_{AVLL}	ALE, A[23:16],	EACL:STS=0 and EACL:ACE=0	$t_{CYC} - 15$	—	ns	EBM:NMS=0
			EACL:STS=1 and EACL:ACE=0	$3t_{CYC}/2 - 15$	—		
			EACL:STS=0 and EACL:ACE=1	$2t_{CYC} - 15$	—		
			EACL:STS=1 and EACL:ACE=1	$5t_{CYC}/2 - 15$	—		
	t_{ADVLL}	ALE,AD[15:0]	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 15$	—	ns	
			EACL:STS=1 and EACL:ACE=0	$t_{CYC} - 15$	—		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 15$	—		
			EACL:STS=1 and EACL:ACE=1	$2t_{CYC} - 15$	—		
ALE $\downarrow$ $\Rightarrow$ Address valid time (multiplexed)	t_{LLAX}	ALE, AD[15:0]	EACL:STS=0	$t_{CYC}/2 - 15$	—	ns	
			EACL:STS=1	-15	—		
Valid address $\Rightarrow$ RDX $\downarrow$ time (non-multiplexed)	t_{AVRL}	RDX, A[23:0]	EBM:NMS= 1	$t_{CYC}/2 - 15$	—	ns	
Valid address $\Rightarrow$ RDX $\downarrow$ time (multiplexed)	t_{AVRL}	RDX, A[23:16]	EACL:ACE=0 EBM:NMS=0	$3t_{CYC}/2 - 15$	—	ns	
			EACL:ACE=1 EBM:NMS=0	$5t_{CYC}/2 - 15$	—		
	t_{ADVRL}	RDX, AD[15:0]	EACL:ACE=0 EBM:NMS=0	$t_{CYC} - 15$	—	ns	
			EACL:ACE=1 EBM:NMS=0	$2t_{CYC} - 15$	—		
Valid address $\Rightarrow$ Valid data input (non-multiplexed)	t_{AVDV}	A[23:0], AD[15:0]	EBM:NMS= 1	—	$2t_{CYC} - 55$	ns	w/o cycle extension
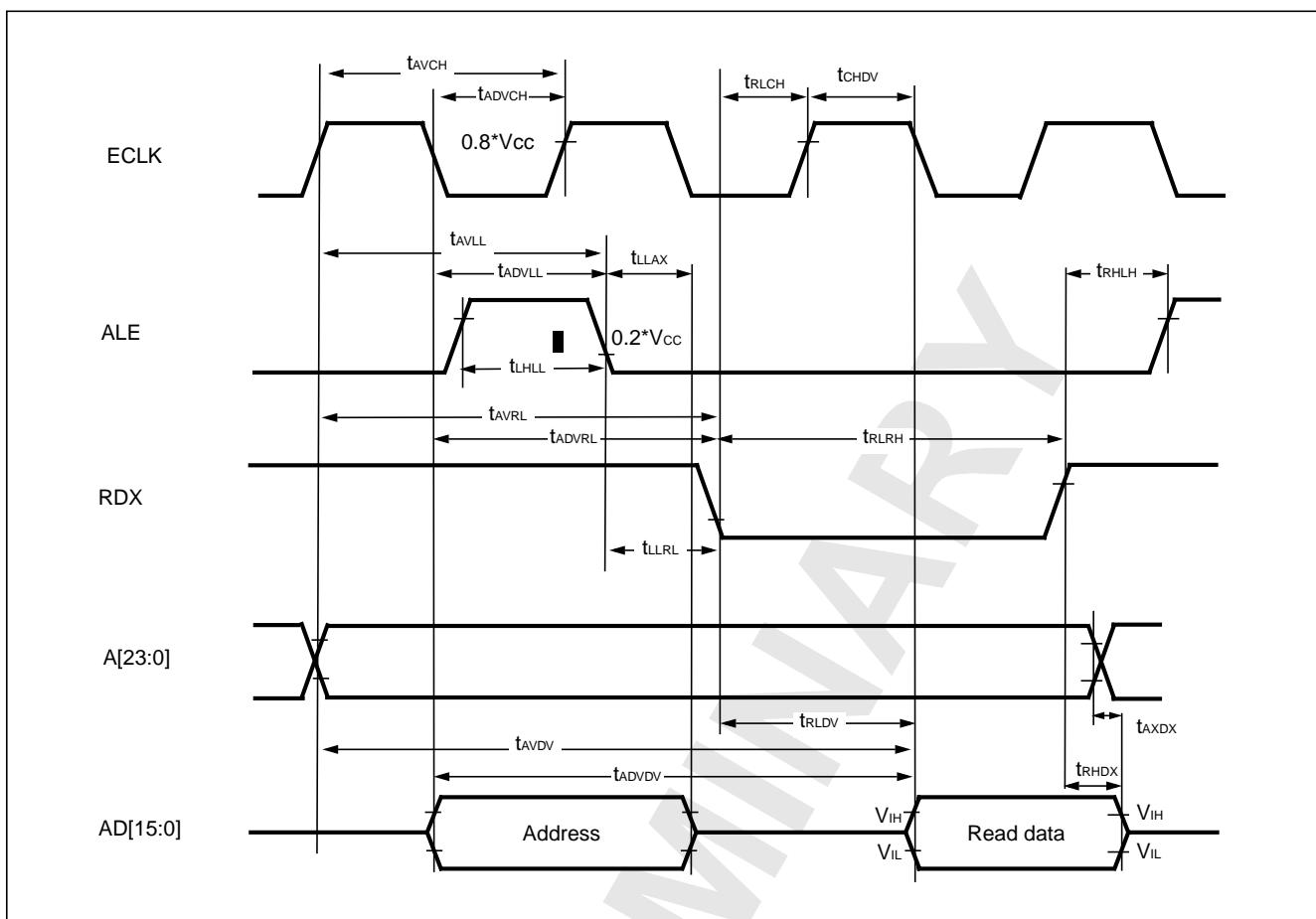
($T_A = -40\,°\mathbf{C\ to}\ +125\,°\mathbf{C,}$ $V_{CC} = 5.0$ V $\pm 10\%$, $V_{SS} = 0.0$ V, $IO_{drive} = 5$mA, $C_L = 50$pF)

Parameter	Sym-bol	Pin	Conditions	Value Min	Value Max	Unit	Remarks
Valid address ⇒ Valid data input (multiplexed)	t_{AVDV}	A[23:16], AD[15:0]	EACL:ACE=0 EBM:NMS=0	—	$3t_{CYC} - 55$	ns	w/o cycle extension
			EACL:ACE=1 EBM:NMS=0	—	$4t_{CYC} - 55$		
	t_{ADVDV}	AD[15:0]	EACL:ACE=0 EBM:NMS=0	—	$5t_{CYC}/2 - 55$	ns	w/o cycle extension
			EACL:ACE=1 EBM:NMS=0	—	$7t_{CYC}/2 - 55$		
RDX pulse width	t_{RLRH}	RDX	—	$3\ t_{CYC}/2 - 5$	—	ns	w/o cycle extension
RDX ↓ ⇒ Valid data input	t_{RLDV}	RDX, AD[15:0]	—	—	$3\ t_{CYC}/2 - 50$	ns	w/o cycle extension
RDX ↑ ⇒ Data hold time	t_{RHDX}	RDX, AD[15:0]	—	0	—	ns	
Address valid ⇒ Data hold time	t_{AXDX}	A[23:0], AD[15:0]	—	0	—	ns	
RDX ↑ ⇒ ALE ↑ time	t_{RHLH}	RDX, ALE	EACL:STS=1 and EACL:ACE=1	$3t_{CYC}/2 - 10$	—	ns	
			other ECL:STS, EACL:ACE setting	$t_{CYC}/2 - 10$	—		
Valid address ⇒ ECLK ↑ time	t_{AVCH}	A[23:0], ECLK	—	$t_{CYC} - 15$	—	ns	
	t_{ADVCH}	AD[15:0], ECLK		$t_{CYC}/2 - 15$	—		
RDX ↓ ⇒ ECLK ↑ time	t_{RLCH}	RDX, CLK	—	$t_{CYC}/2 - 10$	—	ns	
ALE ↓ ⇒ RDX ↓ time	t_{LLRL}	ALE, RDX	EACL:STS=0	$t_{CYC}/2 - 10$	—	ns	
			EACL:STS=1	-10	—		
ECLK ↑ ⇒ Valid data input	t_{CHDV}	AD[15:0], ECLK	—	—	$t_{CYC} - 50$	ns	

$(T_A = -40\ °\text{C to} +125\ °\text{C}, V_{CC} = 3.0 \text{ to } 4.5\text{V}, V_{SS} = 0.0\text{ V, IO}_{drive} = 5\text{mA}, C_L = 50\text{pF})$

Parameter	Sym-bol	Pin	Conditions	Value Min	Value Max	Unit	Remarks
ALE pulse width (multiplexed)	t_{LHLL}	ALE	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 8$	—	ns	
			EACL:STS=1	$t_{CYC} - 8$	—		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 8$	—		
Valid address $\Rightarrow$ ALE $\downarrow$ time (multiplexed)	t_{AVLL}	ALE, A[23:16],	EACL:STS=0 and EACL:ACE=0	$t_{CYC} - 20$	—	ns	EBM:NMS=0
			EACL:STS=1 and EACL:ACE=0	$3t_{CYC}/2 - 20$	—		
			EACL:STS=0 and EACL:ACE=1	$2t_{CYC} - 20$	—		
			EACL:STS=1 and EACL:ACE=1	$5t_{CYC}/2 - 20$	—		
	t_{ADVLL}	ALE, AD[15:0]	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 20$	—	ns	
			EACL:STS=1 and EACL:ACE=0	$t_{CYC} - 20$	—		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 20$	—		
			EACL:STS=1 and EACL:ACE=1	$2t_{CYC} - 20$	—		
ALE $\downarrow$ $\Rightarrow$ Address valid time (multiplexed)	t_{LLAX}	ALE, AD[15:0]	EACL:STS=0	$t_{CYC}/2 - 20$	—	ns	
			EACL:STS=1	-20	—		
Valid address $\Rightarrow$ RDX $\downarrow$ time (non-multiplexed)	t_{AVRL}	RDX, A[23:0]	EBM:NMS= 1	$t_{CYC}/2 - 20$	—	ns	
Valid address $\Rightarrow$ RDX $\downarrow$ time (multiplexed)	t_{AVRL}	RDX, A[23:16]	EACL:ACE=0 EBM:NMS=0	$3t_{CYC}/2 - 20$	—	ns	
			EACL:ACE=1 EBM:NMS=0	$5t_{CYC}/2 - 20$	—		
	t_{ADVRL}	RDX, AD[15:0]	EACL:ACE=0 EBM:NMS=0	$t_{CYC} - 20$	—	ns	
			EACL:ACE=1 EBM:NMS=0	$2t_{CYC} - 20$	—		
Valid address $\Rightarrow$ Valid data input (non-multiplexed)	t_{AVDV}	A[23:0], AD[15:0]	EBM:NMS= 1	—	$2t_{CYC} - 60$	ns	w/o cycle extension

(T_A = −40 °**C to** +125 °**C,** V_{CC} = 3.0 to 4.5V**,** V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Conditions	Value Min	Value Max	Unit	Remarks
Valid address ⇒ Valid data input (multiplexed)	t_{AVDV}	A[23:16], AD[15:0]	EACL:ACE=0 EBM:NMS=0	—	$3t_{CYC} - 60$	ns	w/o cycle extension
			EACL:ACE=1 EBM:NMS=0	—	$4t_{CYC} - 60$		
	t_{ADVDV}	AD[15:0]	EACL:ACE=0 EBM:NMS=0	—	$5t_{CYC}/2 - 60$	ns	w/o cycle extension
			EACL:ACE=1 EBM:NMS=0	—	$7t_{CYC}/2 - 60$		
RDX pulse width	t_{RLRH}	RDX	—	$3t_{CYC}/2 - 8$	—	ns	w/o cycle extension
RDX ↓ ⇒ Valid data input	t_{RLDV}	RDX, AD[15:0]	—	—	$3t_{CYC}/2 - 55$	ns	w/o cycle extension
RDX ↑ ⇒ Data hold time	t_{RHDX}	RDX, AD[15:0]	—	0	—	ns	
Address valid ⇒ Data hold time	t_{AXDX}	A[23:0]	—	0	—	ns	
RDX ↑ ⇒ ALE ↑ time	t_{RHLH}	RDX, ALE	EACL:STS=1 and EACL:ACE=1	$3t_{CYC}/2 - 15$	—	ns	
			other ECL:STS, EACL:ACE setting	$t_{CYC}/2 - 15$	—		
Valid address ⇒ ECLK ↑ time	t_{AVCH}	A[23:0], ECLK	—	$t_{CYC} - 20$	—	ns	
	t_{ADVCH}	AD[15:0], ECLK	—	$t_{CYC}/2 - 20$	—		
RDX ↓ ⇒ ECLK ↑ time	t_{RLCH}	RDX, CLK	—	$t_{CYC}/2 - 15$	—	ns	
ALE ↓ ⇒ RDX ↓ time	t_{LLRL}	ALE, RDX	EACL:STS=0	$t_{CYC}/2 - 15$	—	ns	
			EACL:STS=1	-15	—		
ECLK ↑ ⇒ Valid data input	t_{CHDV}	AD[15:0], ECLK	—	—	$t_{CYC} - 55$	ns	

Refer to the Hardware Manual for detailed Timing Charts.

Bus Timing (Write)

($T_A = -40\ °C$ to $+125\ °C$, $V_{CC} = 5.0\ V \pm 10\%$, $V_{SS} = 0.0\ V$, $IO_{drive} = 5mA$, $C_L = 50pF$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Valid address $\Rightarrow$ WRX $\downarrow$ time (non-multiplexed)	t_{AVWL}	WRX, WRLX, WRHX, A[23:0]	EACL:STS=0 EBM:NMS=1	$t_{CYC}/2 - 15$	—	ns	
			EACL:STS=1 EBM:NMS=1	$t_{CYC} - 15$	—		
Valid address $\Rightarrow$ WRX $\downarrow$ time (multiplexed)	t_{AVWL}	WRX, WRLX, WRHX, A[23:16]	EACL:ACE=0 EBM:NMS=0	$3t_{CYC}/2 - 15$	—	ns	
			EACL:ACE=1 EBM:NMS=0	$5t_{CYC}/2 - 15$	—		
	t_{ADVWL}	WRX, WRLX, WRHX, AD[15:0]	EACL:ACE=0 EBM:NMS=0	$t_{CYC} - 15$		ns	
			EACL:ACE=1 EBM:NMS=0	$2t_{CYC} - 15$			
WRX pulse width	t_{WLWH}	WRX, WRLX, WRHX	—	$t_{CYC} - 5$	—	ns	w/o cycle extension
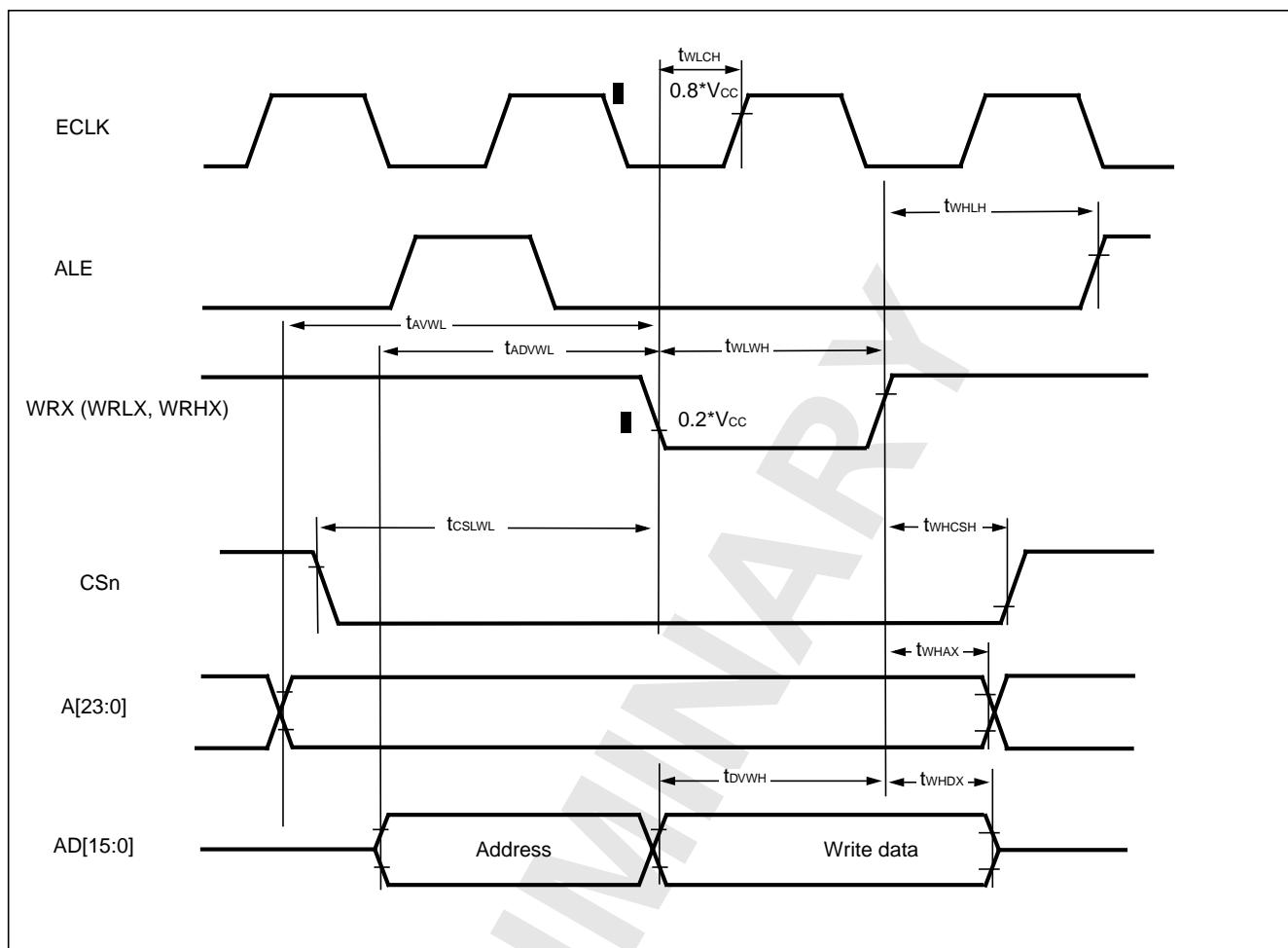
(T$_A$ = −40 °C to +125 °C, V$_{CC}$ = 5.0 V ± 10%, V$_{SS}$ = 0.0 V, IO$_{drive}$ = 5mA, C$_L$ = 50pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Valid data output ⇒ WRX ↑ time	t$_{DVWH}$	WRX, WRLX, WRHX, AD[15:0]	—	t$_{CYC}$ − 20	—	ns	w/o cycle extension
WRX ↑ ⇒ Data hold time	t$_{WHDX}$	WRX, WRLX, WRHX, AD[15:0]	—	t$_{CYC}$/2 − 15	—	ns	
WRX ↑ ⇒ Address valid time (non-multiplexed)	t$_{WHAX}$	WRX, WRLX, WRHX, A[23:0]	EACL:STS=1 EBM:NMS=1	− 15	—	ns	
			EACL:STS=0 EBM:NMS=1	t$_{CYC}$/2 − 15	—	ns	
WRX ↑ ⇒ Address valid time (multiplexed)	t$_{WHAX}$	WRX, WRLX, WRHX, A[23:16]	EBM:NMS=0	t$_{CYC}$/2 − 15	—	ns	
WRX ↑ ⇒ ALE ↑ time (multiplexed)	t$_{WHLH}$	WRX, WRLX, WRHX, ALE	EBM:ACE=1 and EACL:STS=1	2t$_{CYC}$ − 10	—	ns	EBM:NMS=0
			other EBM:ACE and EACL:STS setting	t$_{CYC}$ − 10	—		
WRX ↓ ⇒ ECLK ↑ time	t$_{WLCH}$	WRX, WRLX, WRHX, ECLK	—	t$_{CYC}$/2 − 10	—	ns	
CSn ⇒ WRX time (non-multiplexed)	t$_{CSLWL}$	WRX, WRLX, WRHX, CSn	EACL:STS=0 EBM:NMS=1	—	t$_{CYC}$/2 − 15	ns	
			EACL:STS=1 EBM:NMS=1	—	t$_{CYC}$ − 15		
CSn ⇒ WRX time (multiplexed)	t$_{CSLWL}$	WRX, WRLX, WRHX, CSn	EACL:ACE=0 EBM:NMS=0	—	3t$_{CYC}$/2 − 15	ns	
			EACL:ACE=1 EBM:NMS=0	—	5t$_{CYC}$/2 − 15		
WRX ⇒ CSn time (non-multiplexed)	t$_{WHCSH}$	WRX, WRLX, WRHX, CSn	EACL:STS=1 EBM:NMS=1	− 15	—	ns	
			EACL:STS=0 EBM:NMS=1	t$_{CYC}$/2 − 15	—	ns	
WRX ⇒ CSn time (multiplexed)	t$_{WHCSH}$	WRX, WRLX, WRHX, CSn	EBM:NMS=0	t$_{CYC}$/2 − 15	—	ns	

(T$_A$ = −40 °C to +125 °C, V$_{CC}$ = 3.0 to 4.5V, V$_{SS}$ = 0.0 V, IO$_{drive}$ = 5mA, C$_L$ = 50pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Valid address ⇒ WRX ↓ time (non-multiplexed)	t$_{AVWL}$	WRX, WRLX, WRHX, A[23:0]	EACL:STS=0 EBM:NMS=1	t$_{CYC}$/2 − 20	—	ns	
			EACL:STS=1 EBM:NMS=1	t$_{CYC}$ − 20	—		

Parameter	Symbol	Pin	Condition	Value Min	Value Max	Unit	Remarks
Valid address ⇒ WRX ↓ time (multiplexed)	t_{AVWL}	WRX, WRLX, WRHX, A[23:16]	EACL:ACE=0 EBM:NMS=0	$3t_{CYC}/2 - 20$	—	ns	
			EACL:ACE=1 EBM:NMS=0	$5t_{CYC}/2 - 20$	—	ns	
	t_{ADVWL}	WRX, WRLX, WRHX, AD[15:0]	EACL:ACE=0 EBM:NMS=0	$t_{CYC} - 20$	—	ns	
			EACL:ACE=1 EBM:NMS=0	$2t_{CYC} - 20$	—	ns	
WRX pulse width	t_{WLWH}	WRX, WRXL, WRHX	—	$t_{CYC} - 8$	—	ns	w/o cycle extension
Valid data output ⇒ WRX ↑ time	t_{DVWH}	WRX, WRLX, WRHX, AD[15:0]	—	$t_{CYC} - 25$	—	ns	w/o cycle extension
WRX ↑ ⇒ Data hold time	t_{WHDX}	WRX, WRLX, WRHX, AD[15:0]	—	$t_{CYC}/2 - 20$	—	ns	
WRX ↑ ⇒ Address valid time (non-multiplexed)	t_{WHAX}	WRX, WRLX, WRHX, A[23:0]	EACL:STS=1 EBM:NMS=1	$- 20$	—	ns	
			EACL:STS=0 EBM:NMS=1	$t_{CYC}/2 - 20$	—	ns	
WRX ↑ ⇒ Address valid time (multiplexed)	t_{WHAX}	WRX, WRLX, WRHX, A[23:16]	EBM:NMS=0	$t_{CYC}/2 - 20$	—	ns	
WRX ↑ ⇒ ALE ↑ time (multiplexed)	t_{WHLH}	WRX, WRLX, WRHX, ALE	EBM:ACE=1 and EACL:STS=1	$2t_{CYC} - 15$	—	ns	EBM:NMS=0
			other EBM:ACE and EACL:STS setting	$t_{CYC} - 15$	—	ns	
WRX ↓ ⇒ ECLK ↑ time	t_{WLCH}	WRX, WRLX, WRHX, ECLK	—	$t_{CYC}/2 - 15$	—	ns	
CSn ⇒ WRX time (non-multiplexed)	t_{CSLWL}	WRX, WRLX, WRHX, CSn	EACL:STS=0 EBM:NMS=1	—	$t_{CYC}/2 - 20$	ns	
			EACL:STS=1 EBM:NMS=1	—	$t_{CYC} - 20$	ns	
CSn ⇒ WRX time (multiplexed)	t_{CSLWL}	WRX, WRLX, WRHX, CSn	EACL:ACE=0 EBM:NMS=0	—	$3t_{CYC}/2 - 20$	ns	
			EACL:ACE=1 EBM:NMS=0	—	$5t_{CYC}/2 - 20$	ns	
WRX ⇒ CSn time (non-multiplexed)	t_{WHCSH}	WRX, WRLX, WRHX, CSn	EACL:STS=1 EBM:NMS=1	$- 20$	—	ns	
			EACL:STS=0 EBM:NMS=1	$t_{CYC}/2 - 20$	—	ns	
WRX ⇒ CSn time (multiplexed)	t_{WHCSH}	WRX, WRLX, WRHX, CSn	EBM:NMS=0	$t_{CYC}/2 - 20$	—	ns	

Refer to the Hardware Manual for detailed Timing Charts.

Ready Input Timing
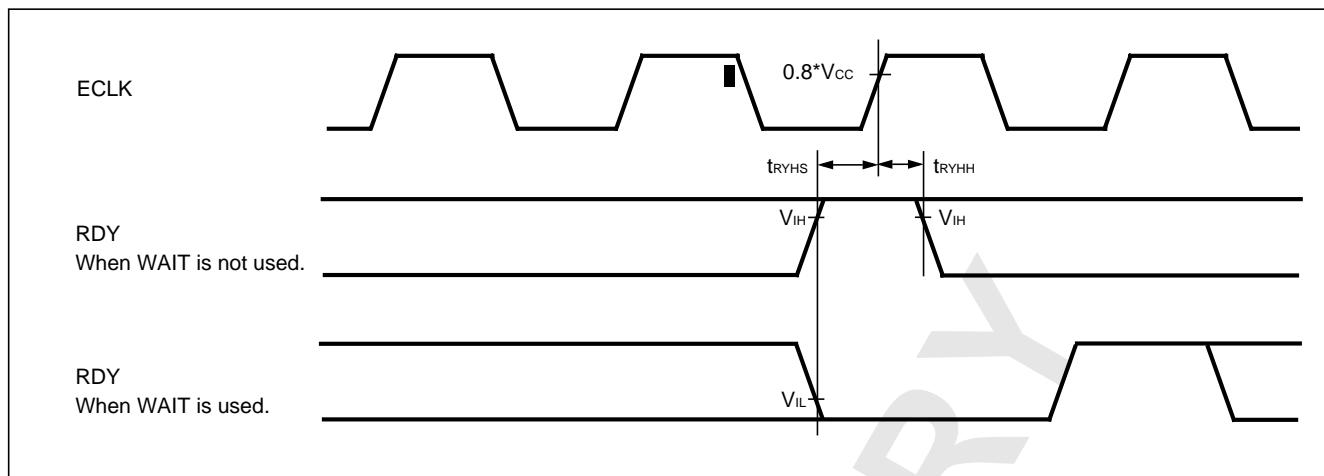
$(T_A = -40\ °C\ to\ +125\ °C,\ V_{CC} = 5.0\ V \pm 10\%,\ V_{SS} = 0.0\ V,\ IO_{drive} = 5mA,\ C_L = 50pF)$

Parameter	Symbol	Pin	Test Condition	Rated Value		Units	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	—	35	—	ns	
RDY hold time	t_{RYHH}	RDY		0	—	ns	

$(T_A = -40\ °C\ to\ +125\ °C,\ V_{CC} = 3.0\ to\ 4.5V,\ V_{SS} = 0.0\ V,\ IO_{drive} = 5mA,\ C_L = 50pF)$

Parameter	Symbol	Pin	Test Condition	Rated Value		Units	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	—	45	—	ns	
RDY hold time	t_{RYHH}	RDY		0	—	ns	

Note : If the RDY setup time is insufficient, use the auto-ready function.

Refer to the Hardware Manual for detailed Timing Charts.
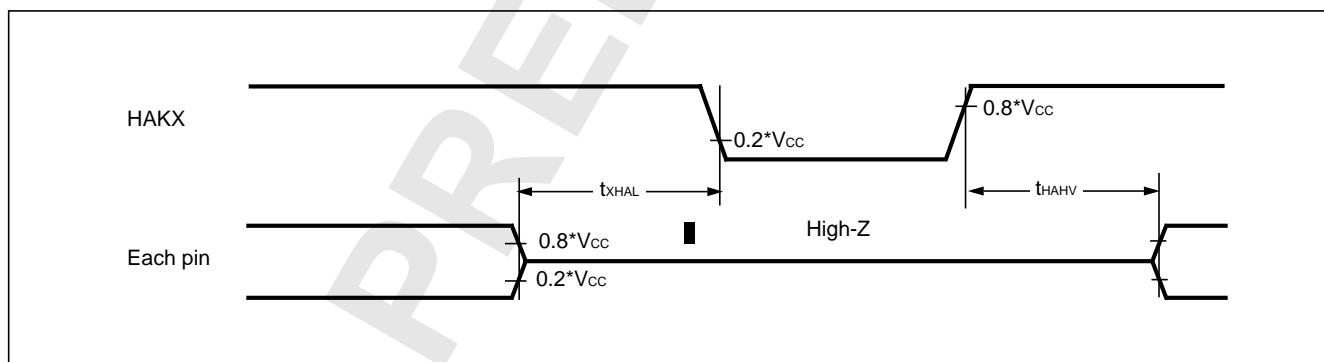
Hold Timing

$(T_A = -40\ °C\ to\ +125\ °C,\ V_{CC} = 5.0\ V \pm 10\%,\ V_{SS} = 0.0\ V,\ IO_{drive} = 5mA,\ C_I = 50pF)$

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	**Max**		
Pin floating $\Rightarrow$ HAKX $\downarrow$ time	t_{XHAL}	HAKX	—	$t_{CYC} - 20$	$t_{CYC} + 20$	ns	
HAKX $\uparrow$ time $\Rightarrow$ Pin valid time	t_{HAHV}	HAKX		$t_{CYC} - 20$	$t_{CYC} + 20$	ns	

$(T_A = -40\ °C\ to\ +125\ °C,\ V_{CC} = 3.0\ to\ 4.5V,\ V_{SS} = 0.0\ V,\ IO_{drive} = 5mA,\ C_I = 50pF)$

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	**Max**		
Pin floating $\Rightarrow$ HAKX $\downarrow$ time	t_{XHAL}	HAKX	—	$t_{CYC} - 25$	$t_{CYC} + 25$	ns	
HAKX $\uparrow$ time $\Rightarrow$ Pin valid time	t_{HAHV}	HAKX		$t_{CYC} - 25$	$t_{CYC} + 25$	ns	

Refer to the Hardware Manual for detailed Timing Charts.

USART timing

WARNING: The values given below are for an I/O driving strength IO_{drive} = 5mA. If IO_{drive} is 2mA, all the maximum output timing described in the different tables must then be increased by 10ns.

(T_A = -40˚C to 125˚C, V_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	V_{CC} = AV_{CC}= 4.5V to 5.5V		V_{CC} = AV_{CC}= 3.0V to 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYCI}	SCKn	Internal Shift Clock Mode	4 t_{CLKP1}	—	4 t_{CLKP1}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKn, SOTn		-20	+20	-30	+30	ns
SOT → SCK ↑ delay time	t_{OVSHI}	SCKn, SOTn		N*t_{CLKP1} - 20 [*1]	—	N*t_{CLKP1} - 30 [*1]	—	
Valid SIN → SCK ↑	t_{IVSHI}	SCKn, SINn		t_{CLKP1} + 45	—	t_{CLKP1} + 55	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCKn, SINn		0	—	0	—	ns
Serial clock "L" pulse width	t_{SLSHE}	SCKn	External Shift Clock Mode	t_{CLKP1} + 10	—	t_{CLKP1} + 10	—	ns
Serial clock "H" pulse width	t_{SHSLE}	SCKn		t_{CLKP1} + 10	—	t_{CLKP1} + 10	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKn, SOTn		—	2 t_{CLKP1} + 45	—	2 t_{CLKP1} + 55	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCKn, SINn		t_{CLKP1}/2 + 10	—	t_{CLKP1}/2 + 10	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXE}	SCKn, SINn		t_{CLKP1} + 10	—	t_{CLKP1} + 10	—	ns
SCK fall time	t_{FE}	SCKn		—	20	—	20	ns
SCK rise time	t_{RE}	SCKn		—	20	—	20	ns

Notes:
- AC characteristic in CLK synchronized mode.
- C_L is the load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in "MB96300 Super series HARDWARE MANUAL"
- t_{CLKP1} is the cycle time of the peripheral clock 1 (CLKP1), Unit : ns
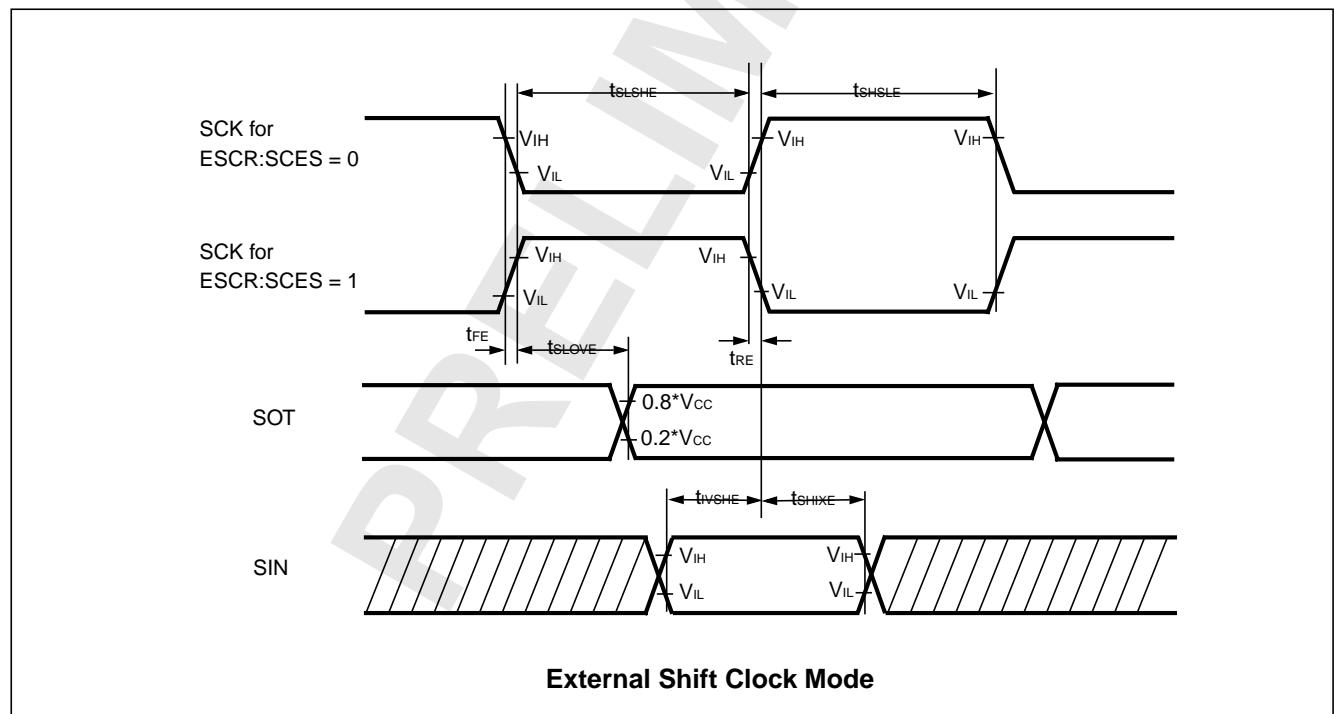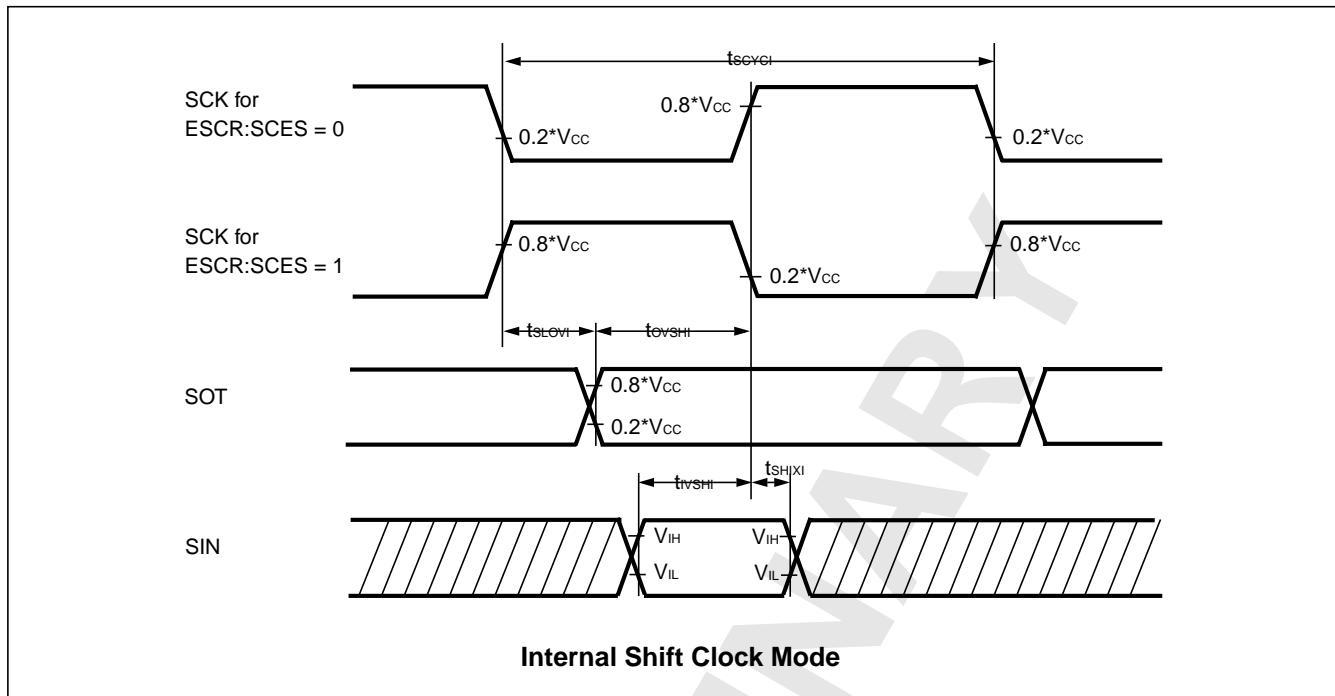
*1: Parameter N depends on t_{SCYCI} and can be calculated as follows:
- if t_{SCYCI} = 2*k*t_{CLKP1}, then N = k, where k is an integer > 2
- if t_{SCYCI} = (2*k+1)*t_{CLKP1}, then N = k+1, where k is an integer > 1
  Examples:

t_{SCYCI}	N
4*t_{CLKP1}	2
5*t_{CLKP1}, 6*t_{CLKP1}	3
7*t_{CLKP1}, 8*t_{CLKP1}	4
...	...

Internal Shift Clock Mode

External Shift Clock Mode

I²C Timing

(T$_A$ = -40˚C to 125˚C, V$_{CC}$ = AV$_{CC}$ = 3.0V to 5.5V, V$_{SS}$ = AV$_{SS}$ = 0V)
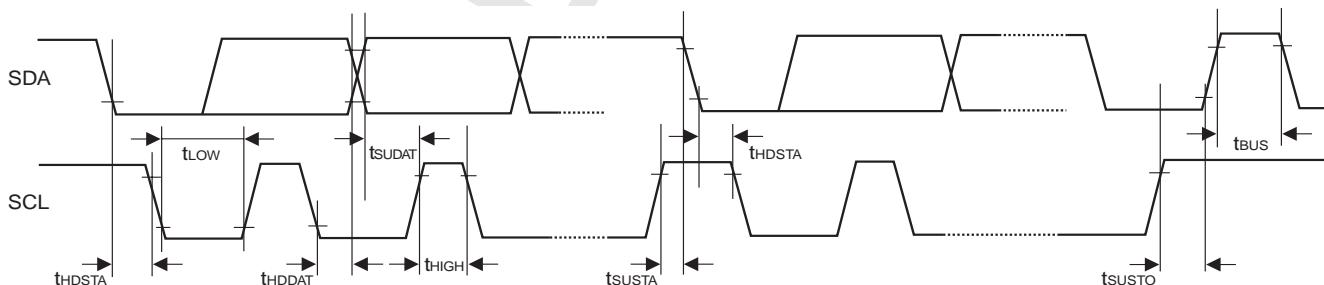
Parameter	Symbol	Condition	Standard-mode		Fast-mode[4]		Unit
			Min	Max	Min	Max	
SCL clock frequency	f$_{SCL}$		0	100	0	400	kHz
Hold time (repeated) START condition SDA↓→SCL↓	t$_{HDSTA}$		4.0	—	0.6	—	μs
"L" width of the SCL clock	t$_{LOW}$		4.7	—	1.3	—	μs
"H" width of the SCL clock	t$_{HIGH}$		4.0	—	0.6	—	μs
Set-up time for a repeated START condition SCL↑→SDA↓	t$_{SUSTA}$	R = 1.7 kΩ, C = 50 pF[1]	4.7	—	0.6	—	μs
Data hold time SCL↓→SDA↓↑	t$_{HDDAT}$		0	3.45[2]	0	0.9[3]	μs
Data set-up time SDA↓↑→SCL↑	t$_{SUDAT}$		250	—	100	—	ns
Set-up time for STOP condition SCL↑→SDA↑	t$_{SUSTO}$		4.0	—	0.6	—	μs
Bus free time between a STOP and START condition	t$_{BUS}$		4.7	—	1.3	—	μs

*1 : R,C : Pull-up resistor and load capacitor of the SCL and SDA lines.

*2 : The maximum t$_{HDDAT}$ have only to be met if the device does not stretch the "L" width (t$_{LOW}$) of the SCL signal.

*3 : A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement t$_{SUDAT}$ ≥ 250 ns must then be met.

*4 : For use at over 100 kHz, set the peripheral clock 1 to at least 6 MHz.

5. Analog Digital Converter

(T_A = -40 ˚C to +125 ˚C, 3.0 V $\leq$ AVRH - AVRL, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Total error	-	-	-3	-	+3	LSB	
Nonlinearity error	-	-	-2.5	-	+2.5	LSB	
Differential nonlinearity error	-	-	-1.9	-	+1.9	LSB	
Zero reading voltage	V_{OT}	ANn	AVRL - 1.5	AVRL+ 0.5	AVRL + 2.5	LSB	
Full scale reading voltage	V_{FST}	ANn	AVRH - 3.5	AVRH - 1.5	AVRH + 0.5	LSB	
Compare time	-	-	1.0	-	16,500	µs	4.5V $\leq$ AV_{CC} $\leq$ 5.5V
			2.0	-	-	µs	3.0V $\leq$ AV_{CC} < 4.5V
Sampling time	-	-	0.5	-	-	µs	4.5V $\leq$ AV_{CC} $\leq$ 5.5V
			1.2	-	-	µs	3.0V $\leq$ AV_{CC} < 4.5V
Analog port input current	I_{AIN}	ANn	-1	-	+1	µA	T_A = 25 ˚C
			-3	-	+3	µA	T_A = 125 ˚C
Analog input voltage range	V_{AIN}	ANn	AVRL	-	AVRH	V	
Reference voltage range	AVRH	AVRHAVRH2	0.75 AVcc	-	AVcc	V	
	AVRL	AVRL	AV_{SS}	-	0.25 AV_{CC}	V	
Power supply current	I_A	AVcc	-	2.5	5	mA	AD Converter active
	I_{AH}	AVcc	-	-	5	µA	AD Converter not operated
Reference voltage current	I_R	AVRH/ AVRL	-	0.7	1	mA	AD Converter active
	I_{RH}	AVRH/ AVRL	-	-	5	µA	AD Converter not operated
Offset between input channels	-	ANn	-	-	TBD	LSB	

Note: The accuracy gets worse as |AVRH - AVRL| becomes smaller.

Definition of A/D Converter Terms

Resolution: Analog variation that is recognized by an A/D converter.
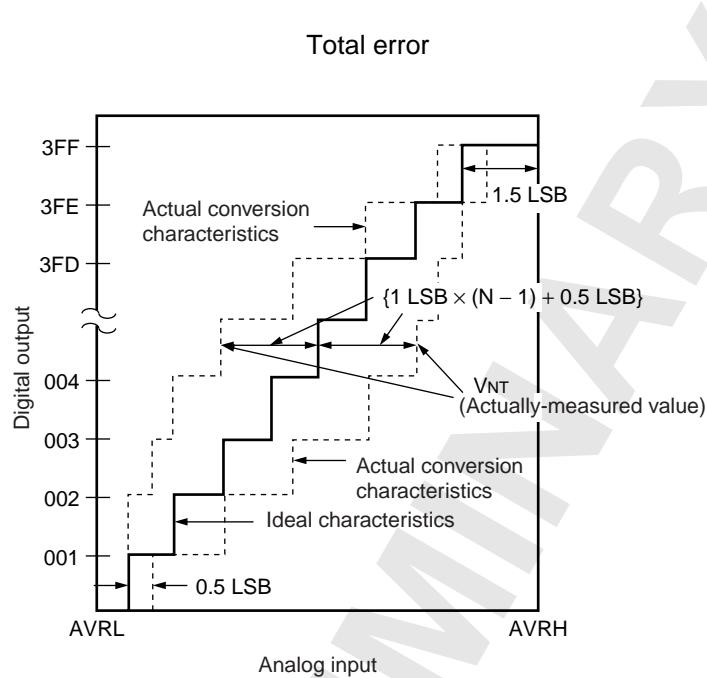
Total error: Difference between the actual value and the ideal value. The total error includes zero transition error, full-scale transition error and linear error.

Nonlinearity error: Deviation between a line across zero-transition line ("00 0000 0000" <--> "00 0000 0001") and full-scale transition line ("11 1111 1110" <--> "11 1111 1111") and actual conversion characteristics.

Differential linearity error: Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.

Zero reading voltage: Input voltage which results in the minimum conversion value.

Full scale reading voltage: Input voltage which results in the maximum conversion value.

Total error

$$\text{Total error of digital output "N"} = \frac{V_{NT} - \{1\ LSB \times (N-1) + 0.5\ LSB\}}{1\ LSB}\ [LSB]$$
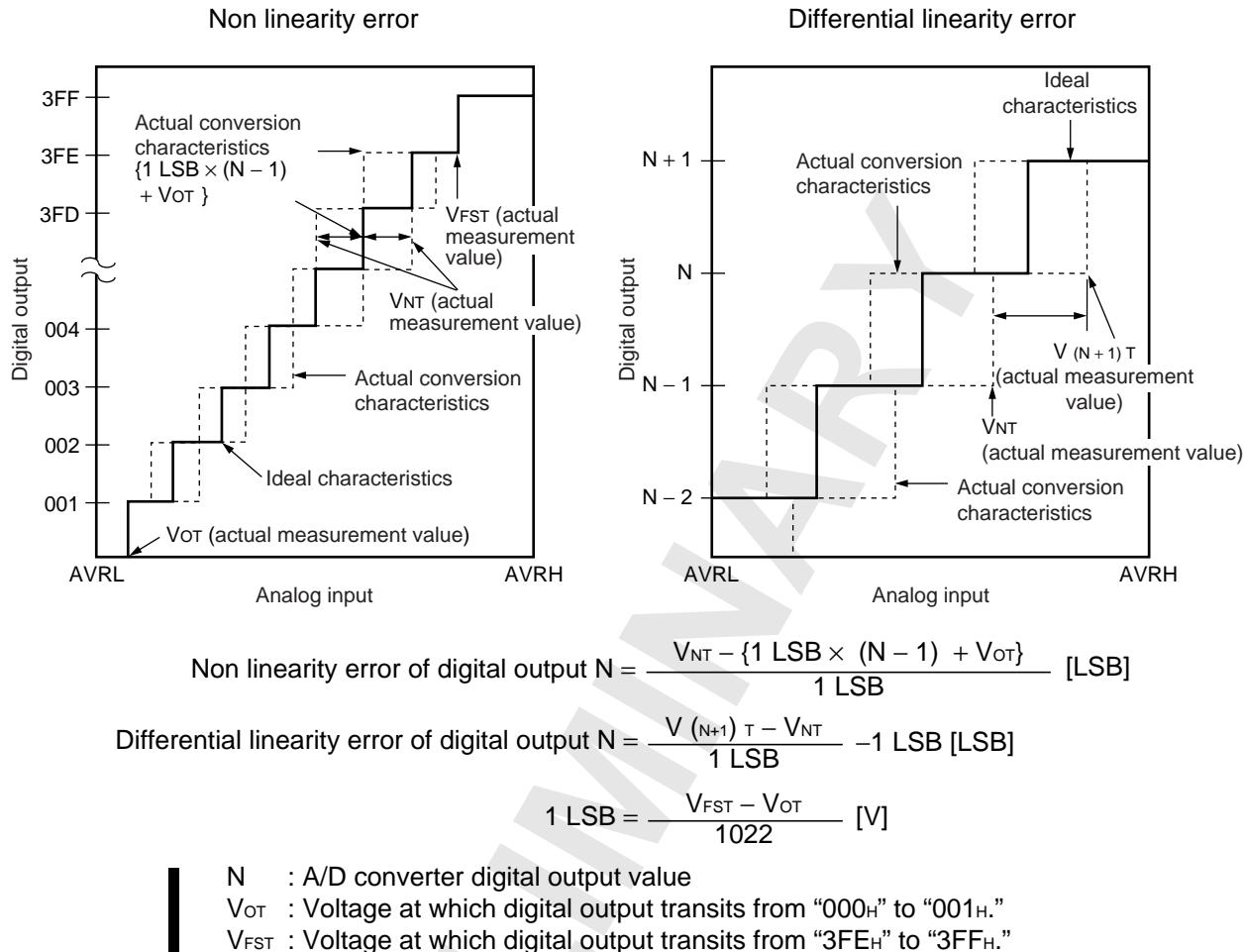
$$1\ LSB = \text{(Ideal value)}\ \frac{AVRH - AVRL}{1024}\ [V]$$

N: A/D converter digital output value

V_{OT} (Ideal value) $= AVRL + 0.5\ LSB\ [V]$

V_{FST} (Ideal value) $= AVRH - 1.5\ LSB\ [V]$
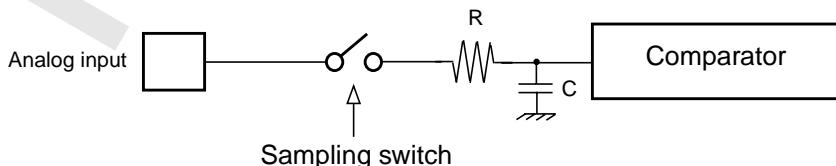
V_{NT} : A voltage at which digital output transitions from $(N-1)$ to N.

Non linearity error

Differential linearity error

$$\text{Non linearity error of digital output } N = \frac{V_{NT} - \{1\ LSB \times (N - 1) + V_{OT}\}}{1\ LSB}\ [LSB]$$

$$\text{Differential linearity error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1\ LSB} - 1\ LSB\ [LSB]$$

$$1\ LSB = \frac{V_{FST} - V_{OT}}{1022}\ [V]$$

N : A/D converter digital output value
V_{OT} : Voltage at which digital output transits from "000$_H$" to "001$_H$."
V_{FST} : Voltage at which digital output transits from "3FE$_H$" to "3FF$_H$."

Notes on A/D Converter Section
• About the external impedance of the analog input and the sampling time of the A/D converter (with sample and hold circuit):

If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

• analog input circuit model:

Reference value:
• C = 8.5 pF (Max)

To satisfy the A/D conversion precision standard, the relationship between the external impedance and minimum sampling time must be considered and then either the resistor value and operating frequency must be adjusted or the external impedance must be decreased so that the sampling time (T_{samp}) is longer than the minimum value. Usually, this value is set to 7τ, where $\tau = RC$. If the external input resistance (R_{ext}) connected to the analog input is included, the sampling time is expressed as follows:

T_{samp} [min] $= 7 \times (R_{ext} + 2.6k\Omega) \times C$ for $4.5 \le AV_{cc} \le 5.5$

T_{samp} [min] $= 7 \times (R_{ext} + 12.1k\Omega) \times C$ for $3.0 \le AV_{cc} \le 4.5$

If the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.
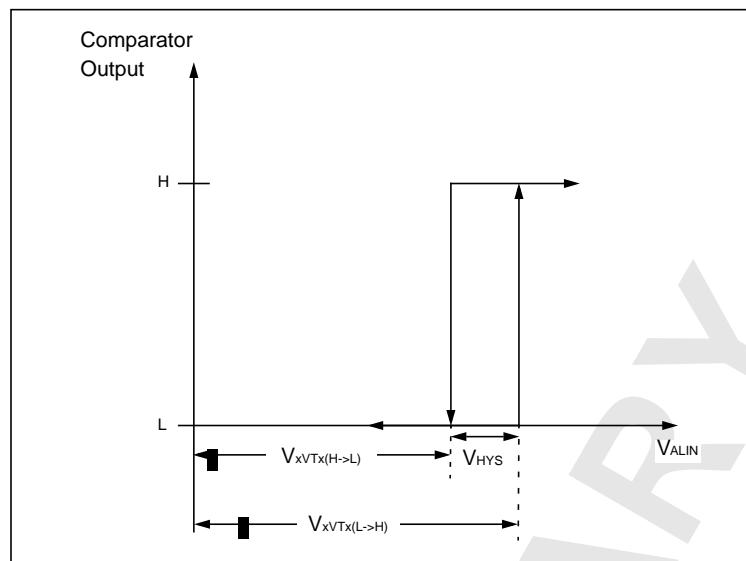
- About the error

The accuracy gets worse as |AVRH - AVRL| becomes smaller.

6. Alarm Comparator

(T$_A$ = -40 ˚C to +125 ˚C, V$_{CC}$ = AV$_{CC}$ = 3.0V - 5.5V, V$_{SS}$ = AV$_{SS}$ = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Power supply current	I$_{A5ALMF}$	AV$_{CC}$	-	25	40	µA	Alarm comparator enabled in fast mode (one channel)
	I$_{A5ALMS}$		-	7	10	µA	Alarm comparator enabled in slow mode (one channel)
	I$_{A5ALMH}$		-	-	5	µA	Alarm comparator disabled
ALARM pin input current	I$_{ALIN}$	ALARM0, ALARM1	-1	-	+1	µA	T$_A$ = 25 ˚C
			-3	-	+3	µA	T$_A$ = 125 ˚C
ALARM pin input voltage range	V$_{ALIN}$		0	-	AV$_{CC}$	V	
External low threshold high->low transition	V$_{EVTL(H->L)}$		0.36 * AV$_{CC}$ -0.25	0.36 * AV$_{CC}$ -0.1		V	INTREF = 0
External low threshold low->high transition	V$_{EVTL(L->H)}$			0.36 * AV$_{CC}$ +0.1	0.36 * AV$_{CC}$ +0.25	V	
External high threshold high->low transition	V$_{EVTH(H->L)}$		0.78 * AV$_{CC}$ -0.25	0.78 * AV$_{CC}$ -0.1		V	
External high threshold low->high transition	V$_{EVTH(L->H)}$			0.78 * AV$_{CC}$ +0.1	0.78 * AV$_{CC}$ +0.25	V	
Internal low threshold high->low transition	V$_{IVTL(H->L)}$		0.9	1.1	-	V	INTREF = 1
Internal low threshold low->high transition	V$_{IVTL(L->H)}$		-	1.3	1.55	V	
Internal high threshold high->low transition	V$_{IVTH(H->L)}$		2.2	2.4	-	V	
Internal high threshold low->high transition	V$_{IVTH(L->H)}$		-	2.6	2.85	V	
Switching hysteresis	V$_{HYS}$		50	-	300	mV	
Comparison time	t$_{COMPF}$		-	0.3	2	µs	CMD = 1 (fast)
	t$_{COMPS}$		-	2	100	µs	CMD = 0 (slow)

7. Low Voltage Detector characteristics

(T_A = -40 ˚C to +125 ˚C, V_{cc} = AV_{cc} = 3.0V - 5.5V, V_{ss} = AV_{ss} = 0V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Stabilization time	$T_{LVDSTAB}$	60	75	µs	
Level 0	V_{DL0}	2.7	2.9	V	CILCR:LVL[3:0]="0000"
Level 1	V_{DL1}	2.9	3.1	V	CILCR:LVL[3:0]="0001"
Level 2	V_{DL2}	3.1	3.3	V	CILCR:LVL[3:0]="0010"
Level 3	V_{DL3}	3.5	3.75	V	CILCR:LVL[3:0]="0011"
Level 4	V_{DL4}	3.6	3.85	V	CILCR:LVL[3:0]="0100"
Level 5	V_{DL5}	3.7	3.95	V	CILCR:LVL[3:0]="0101"
Level 6	V_{DL6}	3.8	4.05	V	CILCR:LVL[3:0]="0110"
Level 7	V_{DL7}	3.9	4.15	V	CILCR:LVL[3:0]="0111"
Level 8	V_{DL8}	4.0	4.25	V	CILCR:LVL[3:0]="1000"
Level 9	V_{DL9}	4.1	4.35	V	CILCR:LVL[3:0]="1001"
Level 10	V_{DL10}	not used			
Level 11	V_{DL11}	not used			
Level 12	V_{DL12}	not used			
Level 13	V_{DL13}	not used			
Level 14	V_{DL14}	not used			
Level 15	V_{DL15}	not used			

Levels 10 to 15 are not used in this device.
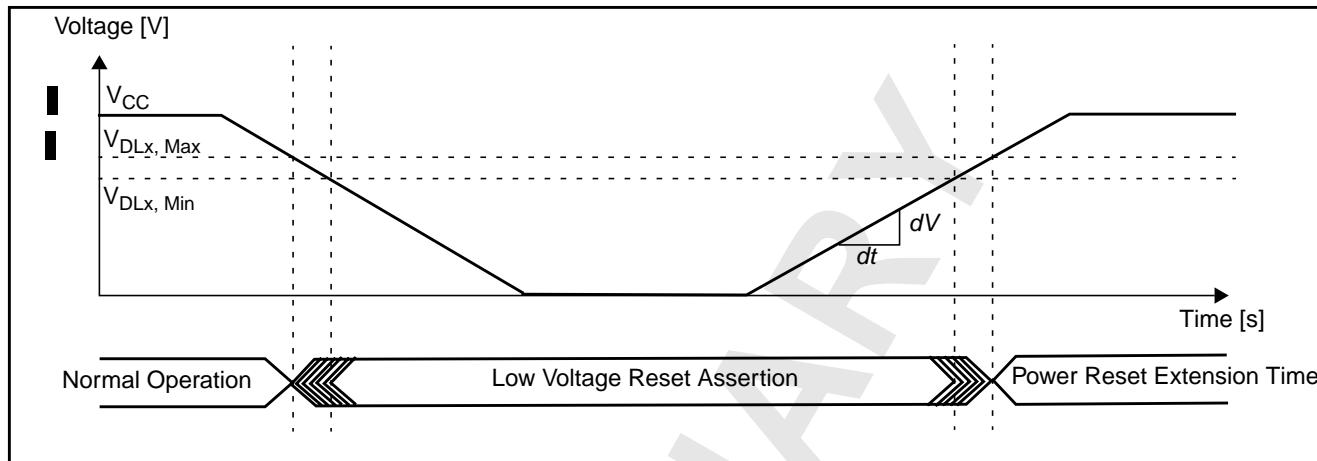
For correct detection, the slope of the voltage level must satisfy $\left|\dfrac{dV}{dt}\right| \leq 0.004 \dfrac{V}{\mu s}$.
Faster variations are regarded as noise and may not be detected.

The functional operation of the MCU is guaranteed down to the minimum low voltage detection level of
Vcc = 2.7V. The electrical characteristics however are only valid in the specified range (usually down to 3.0V).

Low Voltage Detector Operation

In the following figure, the occurrence of a low voltage condition is illustrated. For a detailed description of the reset and startup behavior, please refer to the corresponding hardware manual chapter.

8. FLASH memory program/erase characteristics

(T_A = 25°C, V_{cc} = 5.0V)
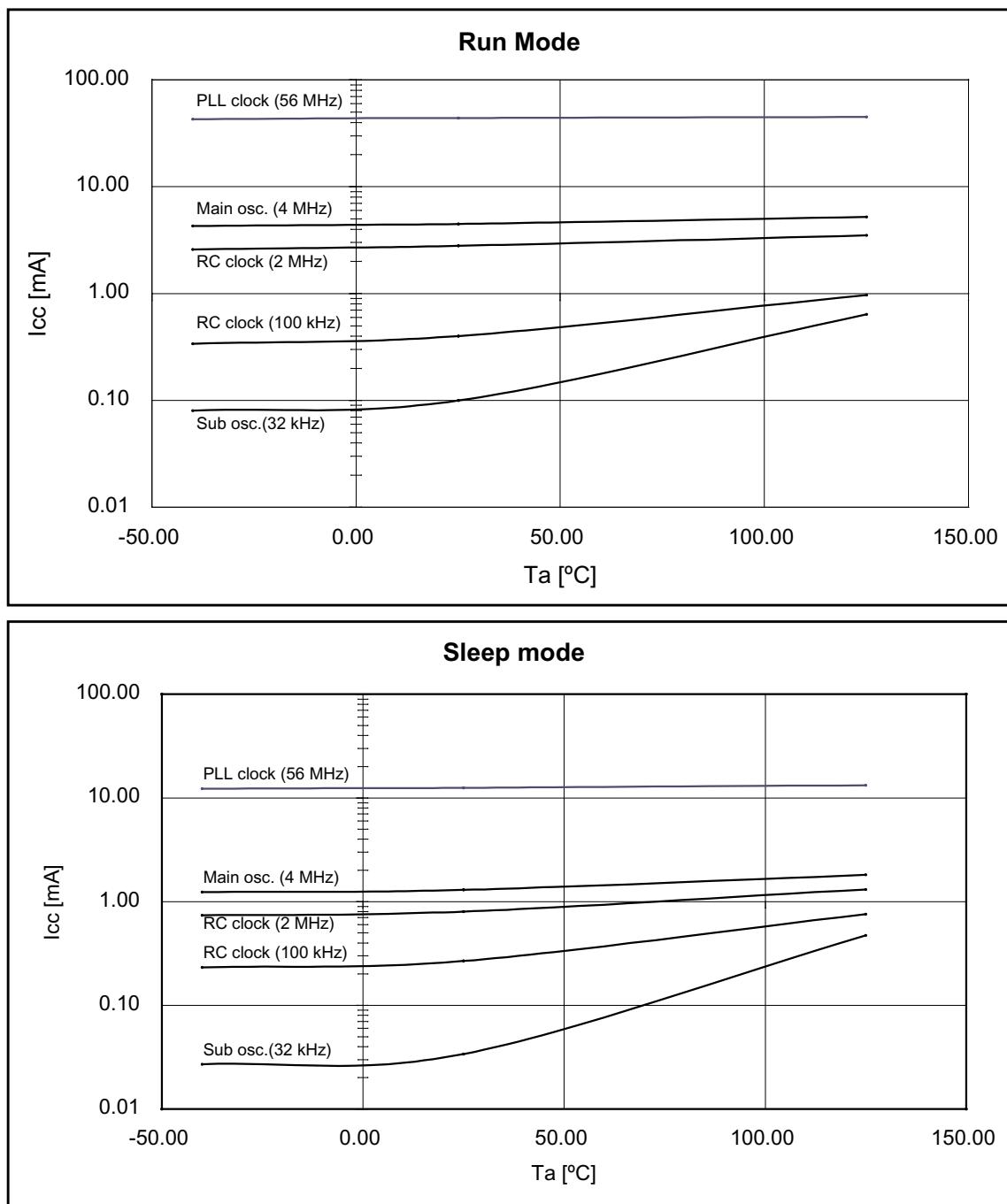
Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	0.9	3.6	s	Erasure programming time not included
Chip erase time	-	n*0.9	n*3.6	s	n is the number of Flash sector of the device
Word (16-bit width) programming time	-	23	370	us	System overhead time not included
Programme/Erase cycle	10 000			cycle	
Flash data retention time	20			year	*1
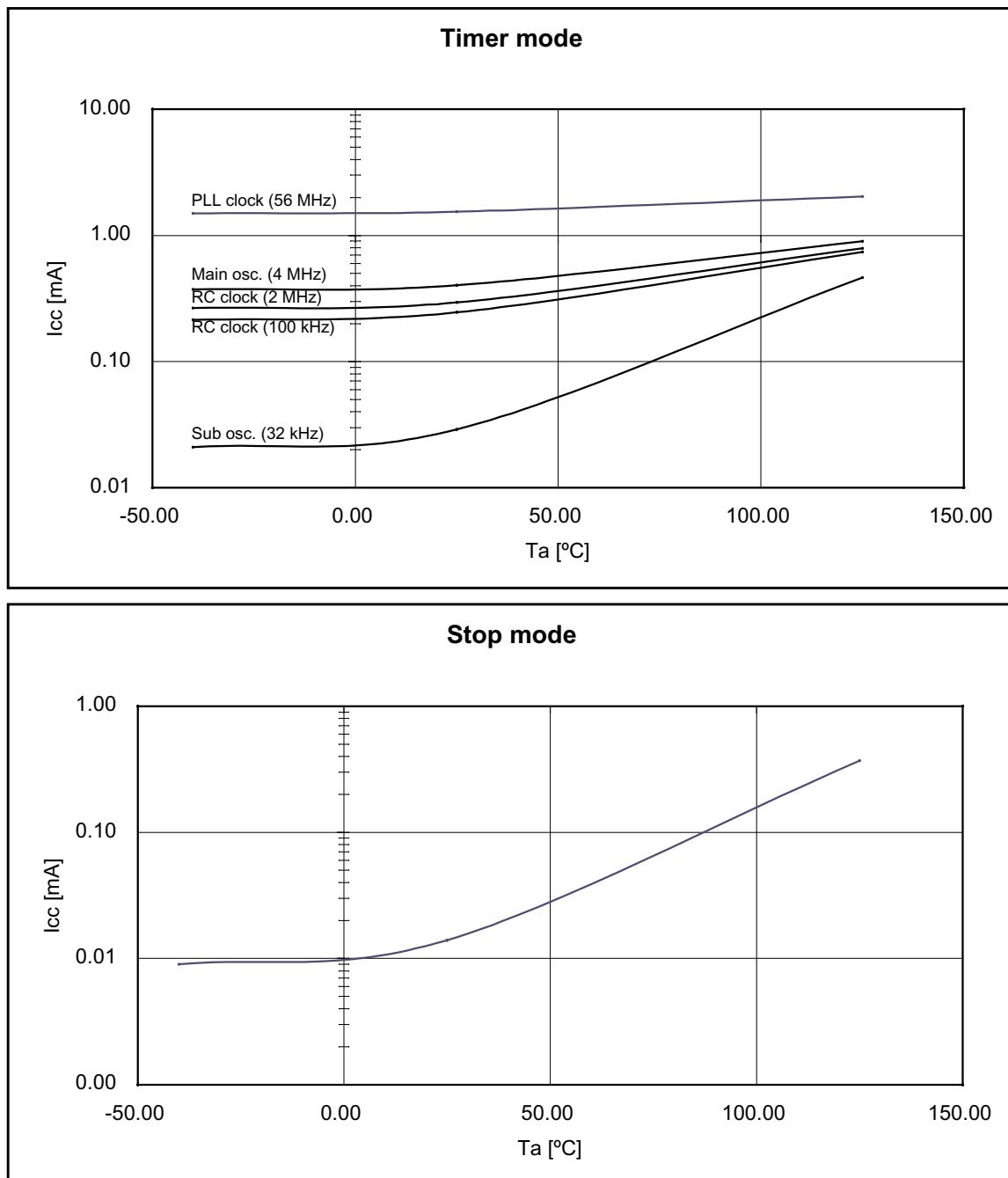
*1: This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85°C)

■ EXAMPLE CHARACTERISTICS

The diagrams below show the characteristics of one measured sample with typical process parameters.

Run Mode

Sleep mode

Timer mode

Stop mode
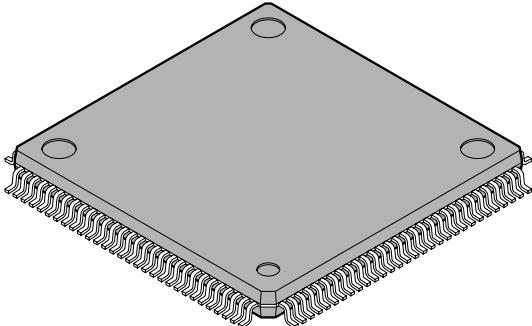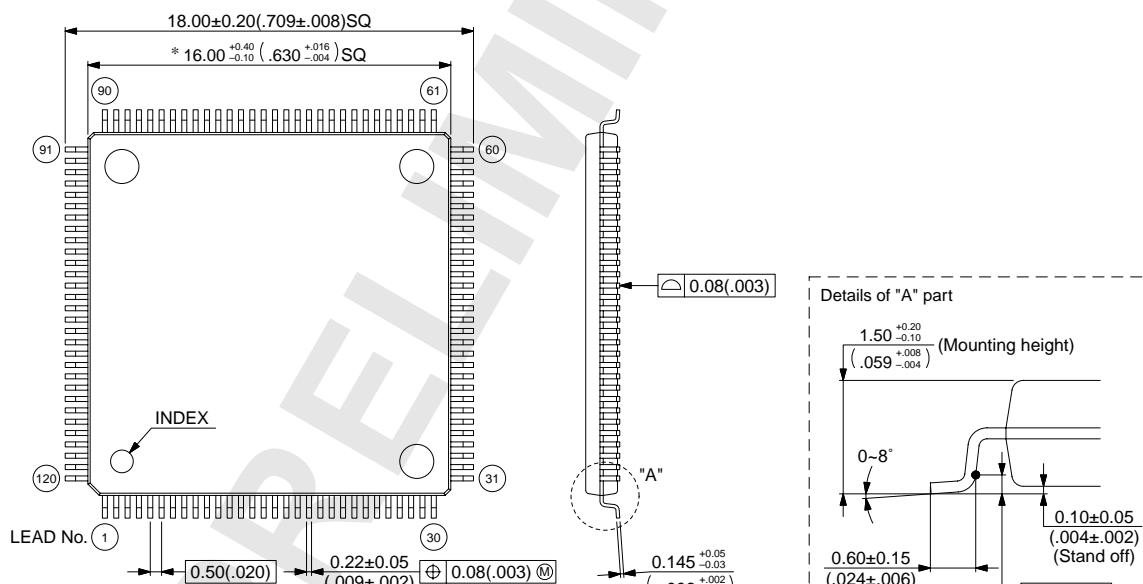
Used settings

Mode	Selected Source Clock	Clock/Regulator Settings
Run mode	PLL	CLKS1 = CLKS2 = CLKB = CLKP1 = 56 MHz CLKP2 = 28 MHz Regulator in High Power Mode Core Voltage = 1.9 V
	Main osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 4 MHz Regulator in High Power Mode Core Voltage = 1.8 V
	RC clock fast	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 2 MHz Regulator in High Power Mode Core Voltage = 1.8 V
	RC clock slow	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 100 kHz Regulator in High Power Mode Core Voltage = 1.8 V
	Sub osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32 kHz Regulator in Low Power Mode A Core Voltage = 1.8 V
Sleep mode	PLL	CLKS1 = CLKS2 = CLKP1 = 56 MHz CLKP2 = 28 MHz (CLKB is stopped in this mode) Regulator in High Power Mode Core Voltage = 1.9 V
	Main osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 4 MHz (CLKB is stopped in this mode) Regulator in High Power Mode Core Voltage = 1.8 V
	RC clock fast	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 2 MHz (CLKB is stopped in this mode) Regulator in High Power Mode Core Voltage = 1.8 V
	RC clock slow	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 100 kHz (CLKB is stopped in this mode) Regulator in High Power Mode Core Voltage = 1.8 V
	Sub osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32 kHz (CLKB is stopped in this mode) Regulator in Low Power Mode A Core Voltage = 1.8 V

Used settings

Mode	Selected Source Clock	Clock/Regulator Settings
Timer mode	PLL	CLKMC = 4 MHz, CLKPLL = 56 MHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.9 V
	Main osc.	CLKMC = 4 MHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.8 V
	RC clock fast	CLKRC = 2 MHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.8 V
	RC clock slow	CLKRC = 100 kHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.8 V
	Sub osc.	CLKSC = 100 kHz (System clocks are stopped in this mode) Regulator in Low Power Mode A, Core Voltage = 1.8 V
Stop mode	stopped	(All clocks are stopped in this mode) Regulator in Low Power Mode B, Core Voltage = 1.8 V

■ PACKAGE DIMENSION MB96(F)38x LQFP 120P

120-pin plastic LQFP	Lead pitch	0.50 mm
	Package width × package length	16.0 × 16.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.88 g
(FPT-120P-M21)	Code (Reference)	P-LFQFP120-16×16-0.50

120-pin plastic LQFP
(FPT-120P-M21)

18.00±0.20(.709±.008)SQ

* $16.00^{+0.40}_{-0.10}\left(.630^{+.016}_{-.004}\right)$SQ

90   61

91   60

INDEX

120   31

LEAD No. 1   30

0.50(.020)

$\underset{(.009\pm.002)}{0.22\pm0.05}$ $\boxed{\oplus\ 0.08(.003)\ \textcircled{M}}$

$\boxed{\bigtriangleup\ 0.08(.003)}$

"A"

$0.145^{+0.05}_{-0.03}$
$\left(.006^{+.002}_{-.001}\right)$

Details of "A" part

$1.50^{+0.20}_{-0.10}$ (Mounting height)
$\left(.059^{+.008}_{-.004}\right)$

0~8°

$\underset{(.024\pm.006)}{0.60\pm0.15}$

0.25(.010)

$\underset{(.004\pm.002)}{0.10\pm0.05}$
(Stand off)

Dimensions in mm (inches).
Note: The values in parentheses are reference values.

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■ ORDERING INFORMATION

Part number	Independent 32kB Data Flash	Subclock	Persistent Low Voltage Reset	Package	Remarks
MB96384YSA PMC-GSE2 [1]	No	No	Yes	120 pin Plastic LQFP (FPT-120P-M21)	
MB96384RSA PMC-GSE2 [1]		No	No		
MB96384YWA PMC-GSE2 [1]		Yes	Yes		
MB96384RWA PMC-GSE2 [1]		Yes	No		
MB96385YSA PMC-GSE2 [1]		No	Yes		
MB96385RSA PMC-GSE2 [1]		No	No		
MB96385YWA PMC-GSE2 [1]		Yes	Yes		
MB96385RWA PMC-GSE2 [1]		Yes	No		
MB96F385YSA PMC-GSE2 [1]	No	No	Yes	120 pin Plastic LQFP (FPT-120P-M21)	
MB96F385RSA PMC-GSE2 [1]		No	No		
MB96F385YWA PMC-GSE2 [1]		Yes	Yes		
MB96F385RWA PMC-GSE2 [1]		Yes	No		
MB96F386YSB PMC-GSE2		No	Yes		
MB96F386RSB PMC-GSE2		No	No		
MB96F386YWB PMC-GSE2		Yes	Yes		
MB96F386RWB PMC-GSE2		Yes	No		
MB96F387YSB PMC-GSE2		No	Yes		
MB96F387RSB PMC-GSE2		No	No		
MB96F387YWB PMC-GSE2		Yes	Yes		
MB96F387RWB PMC-GSE2		Yes	No		
MB96F388TSA PMC-GSE2 [1]	Yes	No	Yes		
MB96F388HSA PMC-GSE2 [1]		No	No		
MB96F388TWA PMC-GSE2 [1]		Yes	Yes		
MB96F388HWA PMC-GSE2 [1]		Yes	No		
MB96F389YSA PMC-GSE2 [1]	No (Flash B size 288kB)	No	Yes		
MB96F389RSA PMC-GSE2 [1]		No	No		
MB96F389YWA PMC-GSE2 [1]		Yes	Yes		
MB96F389RWA PMC-GSE2 [1]		Yes	No		
MB96V300BRB-ES	Emulated by ext. RAM	Yes	No	416 pin Plastic BGA (BGA416-M02)	For evaluation

*1: These devices are under development. All information in this datasheet is preliminary for the devices under development.

This datasheet is also valid for the following outdated devices:

MB96F386YSA, MB96F386RSA, MB96F386YWA, MB96F386RWA,
MB96F387YSA, MB96F387RSA, MB96F387YWA, MB96F387RWA

■ **REVISION HISTORY**

Revision	Date	Modification
Prelim 1	2007-05-2	Creation
Prelim 2	2007-05-24	Electrical characteristics and memory description updates
Prelim 3	2007-08-09	Typo errors corrections, Flash memory programming interface update
Prelim 4	2007-08-31	Update of DC characteristics. new 388 and 389 added. LVD chapter added as well as an example characteristics chapter
Prelim 5	2007-09-06	Updates of the DC characteristics, interrupt vector table update, update of the LVD characteristics
Prelim 6	2007-11-14	Memory map for external bus modified. Modifications of the drawing of the pin circuits. Electrical characteristics updates. Rephrasing and typos corrections. Add Slew rate high current outputs chapter. Modification of the block diagram. Memory map modified for Flash. RAM memory map added. Pin circuit type corrected. Type L IO is now included.
Prelim 7	2007-12-12	Memory IO map modified New Flash/ROM configuration presentation Ordering information: MB96300B used as reference. Block diagram modified to included relocated pins. Main Flash becomes Flash memory A and Satellite flash becomes Flash memory B

Revision	Date	Modification

Prelim 8	2008-02-04	• Devices under development added: MB96384/385/F385/F388/F389
		• Block diagram corrected (existing resource pins)
		• Pin assignment: TTG8 -> TTG7
		• Pin function table corrected
		• I/O circuit type diagrams corrected
		• Memory map cleaned up
		• "Flash sector configuration" replaced by corrected "User ROM Memory map for Flash devices", "ROM configuration" replaced by "User ROM Memory map for Mask ROM devices"
		• IO map table regenerated:
		  - Port register: Naming style corrected
		  - Memory control registers renamed (Main/Sat -> A/B)
		  - addresses after 000BFFh removed
		• Absolute maximum ratings: Pd and Ta specified more precisely
		• Run and Sleep mode currents: more conditions added (1WS settings)
		• Run mode current spec in 48/24MHz mode corrected
		• Maximum CLKP2 frequency for MB96F386/F387 corrected
		• High current port input capacitance added
		• External bus timings: missing conditions added and readability improved
		• Alarm comparator spec updated (transition voltages defined)
		• MB96V300A removed
		• Ordering information updated
		• Typos and formatting corrected

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