Document Number: MPC5553
Rev. 3.0, 3 Jun 2008

MPC5553 Microcontroller Data Sheet

by: Microcontroller Division

This document provides electrical specifications, pin assignments, and package diagrams for the MPC5553 microcontroller device. For functional characteristics, refer to the *MPC5553/MPC5554 Microcontroller Reference Manual*.

1 Overview

The MPC5553 microcontroller (MCU) is a member of the MPC5500 family of microcontrollers built on the Power Architecture™ embedded technology. This family of parts has many new features coupled with high performance CMOS technology to provide substantial reduction of cost per feature and significant performance improvement over the MPC500 family.

The host processor core of this device complies with the Power Architecture embedded category that is 100% user-mode compatible (including floating point library) with the original Power PC™ user instruction set architecture (UISA). The embedded architecture enhancements improve the performance in embedded applications. The core also has additional instructions, including digital signal processing (DSP) instructions, beyond the original Power PC instruction set.

Contents

1 Overview . . . 1
2 Ordering Information . . . 3
3 Electrical Characteristics . . . 4
3.1 Maximum Ratings . . . 4
3.2 Thermal Characteristics . . . 6
3.3 Package . . . 9
3.4 EMI Characteristics . . . 9
3.5 ESD Characteristics . . . 9
3.6 VRC and POR Electrical Specifications . . . 10
3.7 Power-Up/Down Sequencing . . . 11
3.8 DC Electrical Specifications . . . 13
3.9 Oscillator and FMPLL Electrical Characteristics . . . 20
3.10 eQADC Electrical Characteristics . . . 22
3.11 H7Fa Flash Memory Electrical Characteristics . . . 23
3.12 AC Specifications . . . 24
3.13 AC Timing . . . 26
3.14 Fast Ethernet Controller Specifications . . . 45
4 Mechanicals . . . 49
4.1 MPC5553 208 MAP BGA Pinout . . . 49
4.2 MPC5553 324 PBGA Pinout . . . 50
4.3 MPC5553 416 PBGA Pinout . . . 51
4.4 MPC5553 208-Pin Package Dimensions . . . 54
4.5 MPC5553 324-Pin Package Dimensions . . . 56
4.6 MPC5553 416-Pin Package Dimensions . . . 58
5 Revision History for the MPC5553 Data Sheet . . . 60
5.1 Information Changed Between Revisions 2.0 and 3.0 . . . 60

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MPC551x and MPC5533 products in 208 MAPBGA packages; MPC5534 and MPC5553 products in 208 and 496 MAPBGA packages; MPC5554, MPC5565, MPC5566 and MPC5567 products in 496 MAPBGA packages

The MPC5500 family of parts contains many new features coupled with high performance CMOS technology to provide significant performance improvement over the MPC565.

The MPC5553 has two levels of memory hierarchy. The fastest accesses are to the 8-kilobytes (KB) unified cache. The next level in the hierarchy contains the 64-KB on-chip internal SRAM and 1.5-megabytes (MB) internal flash memory. The internal SRAM and flash memory hold instructions and data. The external bus interface is designed to support most of the standard memories used with the MPC5*xx* family.

The complex input/output timer functions of the MPC5553 are performed by an enhanced time processor unit (eTPU) engine. The eTPU engine controls 32 hardware channels. The eTPU has been enhanced over the TPU by providing: 24-bit timers, double-action hardware channels, variable number of parameters per channel, angle clock hardware, and additional control and arithmetic instructions. The eTPU is programmed using a high-level programming language.

The less complex timer functions of the MPC5553 are performed by the enhanced modular input/output system (eMIOS). The eMIOS' 24 hardware channels are capable of single-action, double-action, pulse-width modulation (PWM), and modulus-counter operations. Motor control capabilities include edge-aligned and center-aligned PWM.

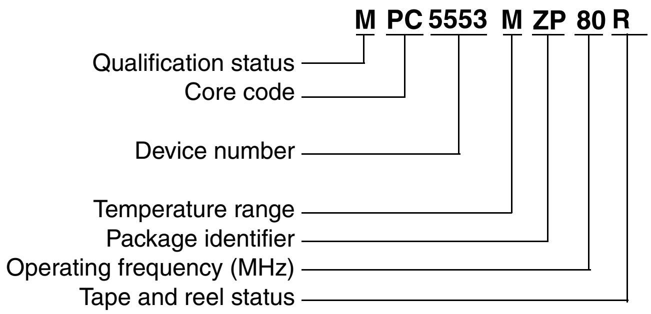
Off-chip communication is performed by a suite of serial protocols including controller area networks (FlexCANs), enhanced deserial/serial peripheral interfaces (DSPIs), and enhanced serial communications interfaces (eSCIs).

The MCU has an on-chip 40-channel enhanced queued dual analog-to-digital converter (eQADC).

The system integration unit (SIU) performs several chip-wide configuration functions. Pad configuration and general-purpose input and output (GPIO) are controlled from the SIU. External interrupts and reset control are also determined by the SIU. The internal multiplexer submodule (SIU_DISR) provides multiplexing of eQADC trigger sources and external interrupt signal multiplexing.

The Fast Ethernet (FEC) module is a RISC-based controller that supports both 10 and 100 Mbps Ethernet/IEEE® 802.3 networks and is compatible with three different standard MAC (media access controller) PHY (physical) interfaces to connect to an external Ethernet bus. The FEC supports the 10 or 100 Mbps MII (media independent interface), and the 10 Mbps-only with a seven-wire interface, which uses a subset of the MII signals. The upper 16-bits of the 32-bit external bus interface (EBI) are used to connect to an external Ethernet device. The FEC contains built-in transmit and receive message FIFOs and DMA support.

2 Ordering Information



Temperature Range
M = –40° C to 125° C

Package Identifier
ZP = 416PBGA SnPb
VR = 416PBGA Pb-free
VF = 208MAPBGA SnPb
VM = 208MAPBGA Pb-free
ZQ = 324PBGA SnPb
VZ = 324PBGA Pb-free

Operating Frequency
80 = 80 MHz
112 = 112 MHz
132 = 132 MHz

Tape and Reel Status
R = Tape and reel
(blank) = Trays

Qualification Status
P = Pre qualification
M = Fully spec. qualified, general market flow
S = Fully spec. qualified, automotive flow

Note: Not all options are available on all devices. Refer to Table 1.

Figure 1. MPC5500 Family Part Number Example

Unless noted in this data sheet, all specifications apply from T_L to T_H.

Table 1. Orderable Part Numbers

Freescale Part Number[1]	Package Description	Speed (MHz)		Operating Temperature [2]	
		Nominal	Max. [3] (f_{MAX})	Min. (T_L)	Max. (T_H)
MPC5553MVR132	MPC5553 416 package Lead-free (Pb-free)	132	132	–40° C	125° C
MPC5553MVR112		112	114		
MPC5553MVR80		80	82		
MPC5553MVZ132	MPC5553 324 package Lead-free (Pb-free)	132	132	–40° C	125° C
MPC5553MVZ112		112	114		
MPC5553MVZ80		80	82		
MPC5553MVM132	MPC5553 208 package Lead-free (Pb-free)	132	132	–40° C	125° C
MPC5553MVM112		112	114		
MPC5553MVM80		80	82		
MPC5553MZP132	MPC5553 416 package Leaded (SnPb)	132	132	–40° C	125° C
MPC5553MZP112		112	114		
MPC5553MZP80		80	82		
MPC5553MZQ132	MPC5553 324 package Leaded (SnPb)	132	132	–40° C	125° C
MPC5553MZQ112		112	114		
MPC5553MZQ80		80	82		

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MPC551x and MPC5533 products in 208 MAPBGA packages; MPC5534 and MPC5553 products in 208 and 496 MAPBGA packages; MPC5554, MPC5565, MPC5566 and MPC5567 products in 496 MAPBGA packages

Table 1. Orderable Part Numbers (continued)

Freescale Part Number[1]	Package Description	Speed (MHz)		Operating Temperature [2]	
		Nominal	Max. [3] (f_{MAX})	Min. (T_L)	Max. (T_H)
MPC5553MVF132	MPC5553 208 package Leaded (SnPb)	132	132	–40° C	125° C
MPC5553MVF112		112	114		
MPC5553MVF80		80	82		

[1] All devices are PPC5553, rather than MPC5553 or SPC5553, until product qualifications are complete. Not all configurations are available in the PPC parts.

[2] The lowest ambient operating temperature is referenced by T_L; the highest ambient operating temperature is referenced by T_H.

[3] Speed is the nominal maximum frequency. Max. speed is the maximum speed allowed including frequency modulation (FM). 82 MHz parts allow for 80 MHz system clock + 2% FM; 114 MHz parts allow for 112 MHz system clock + 2% FM; and132 MHz parts allow for 128 MHz system clock + 2% FM.

3 Electrical Characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MCU.

3.1 Maximum Rating

Table 2. Absolute Maximum Ratings [1]

Spec	Characteristic	Symbol	Min.	Max.	Unit
1	1.5 V core supply voltage [2]	V_{DD}	–0.3	1.7	V
2	Flash program/erase voltage	V_{PP}	–0.3	6.5	V
4	Flash read voltage	V_{FLASH}	–0.3	4.6	V
5	SRAM standby voltage	V_{STBY}	–0.3	1.7	V
6	Clock synthesizer voltage	V_{DDSYN}	–0.3	4.6	V
7	3.3 V I/O buffer voltage	V_{DD33}	–0.3	4.6	V
8	Voltage regulator control input voltage	V_{RC33}	–0.3	4.6	V
9	Analog supply voltage (reference to V_{SSA})	V_{DDA}	–0.3	5.5	V
10	I/O supply voltage (fast I/O pads) [3]	V_{DDE}	–0.3	4.6	V
11	I/O supply voltage (slow and medium I/O pads) [3]	V_{DDEH}	–0.3	6.5	V
12	DC input voltage [4] V_{DDEH} powered I/O pads V_{DDE} powered I/O pads	V_{IN}	 –1.0 [5] –1.0 [5]	 6.5 [6] 4.6 [7]	V
13	Analog reference high voltage (reference to V_{RL})	V_{RH}	–0.3	5.5	V
14	V_{SS} to V_{SSA} differential voltage	$V_{SS} – V_{SSA}$	–0.1	0.1	V
15	V_{DD} to V_{DDA} differential voltage	$V_{DD} – V_{DDA}$	$–V_{DDA}$	V_{DD}	V
16	V_{REF} differential voltage	$V_{RH} – V_{RL}$	–0.3	5.5	V
17	V_{RH} to V_{DDA} differential voltage	$V_{RH} – V_{DDA}$	–5.5	5.5	V

Table 2. Absolute Maximum Ratings [1] (continued)

Spec	Characteristic	Symbol	Min.	Max.	Unit
18	V_{RL} to V_{SSA} differential voltage	$V_{RL} – V_{SSA}$	–0.3	0.3	V
19	V_{DDEH} to V_{DDA} differential voltage	$V_{DDEH} – V_{DDA}$	$–V_{DDA}$	V_{DDEH}	V
20	V_{DDF} to V_{DD} differential voltage	$V_{DDF} – V_{DD}$	–0.3	0.3	V
21	V_{RC33} to V_{DDSYN} differential voltage spec has been moved to Table 9 *DC Electrical Specifications*, Spec 43a.				
22	V_{SSSYN} to V_{SS} differential voltage	$V_{SSSYN} – V_{SS}$	–0.1	0.1	V
23	V_{RCVSS} to V_{SS} differential voltage	$V_{RCVSS} – V_{SS}$	–0.1	0.1	V
24	Maximum DC digital input current [8] (per pin, applies to all digital pins) [4]	I_{MAXD}	–2	2	mA
25	Maximum DC analog input current [9] (per pin, applies to all analog pins)	I_{MAXA}	–3	3	mA
26	Maximum operating temperature range [10] Die junction temperature	T_J	T_L	150.0	°C
27	Storage temperature range	T_{STG}	–55.0	150.0	°C
28	Maximum solder temperature [11] Lead free (Pb-free) Leaded (SnPb)	T_{SDR}	 — —	 260.0 245.0	°C
29	Moisture sensitivity level [12]	MSL	—	3	

[1] Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond any of the listed maxima can affect device reliability or cause permanent damage to the device.

[2] 1.5 V ± 10% for proper operation. This parameter is specified at a maximum junction temperature of 150 °C.

[3] All functional non-supply I/O pins are clamped to V_{SS} and V_{DDE}, or V_{DDEH}.

[4] AC signal overshoot and undershoot of up to ± 2.0 V of the input voltages is permitted for an accumulative duration of 60 hours over the complete lifetime of the device (injection current not limited for this duration).

[5] Internal structures hold the voltage greater than –1.0 V if the injection current limit of 2 mA is met. Keep the negative DC voltage greater than –0.6 V on SINB during the internal power-on reset (POR) state.

[6] Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDEH} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDEH} is within the operating voltage specifications.

[7] Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDE} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDE} is within the operating voltage specifications.

[8] Total injection current for all pins (including both digital and analog) must not exceed 25 mA.

[9] Total injection current for all analog input pins must not exceed 15 mA.

[10] Lifetime operation at these specification limits is not guaranteed.

[11] Moisture sensitivity profile per IPC/JEDEC J-STD-020D.

[12] Moisture sensitivity per JEDEC test method A112.

3.2 Thermal Characteristics

The shaded rows in the following table indicate information specific to a four-layer board.

3.2.1 General Notes for Specifications at Maximum Junction Temperature

Table 3. MPC5553 Thermal Characteristics

Spec	MPC5553 Thermal Characteristic	Symbol	Packages			Unit
			208 MAPBGA	324 PBGA	416 PBGA	
1	Junction to ambient, natural convection (one-layer board) [1, 2]	$R_{\theta JA}$	41	30	29	°C/W
2	Junction to ambient, natural convection [1, 3] (four-layer board 2s2p)	$R_{\theta JA}$	25	21	21	°C/W
3	Junction to ambient (@200 ft./min., one-layer board)	$R_{\theta JMA}$	33	24	23	°C/W
4	Junction to ambient (@200 ft./min., four-layer board 2s2p)	$R_{\theta JMA}$	22	17	18	°C/W
5	Junction to board (four-layer board 2s2p) [4]	$R_{\theta JB}$	15	12	13	°C/W
6	Junction to case [5]	$R_{\theta JC}$	7	8	9	°C/W
7	Junction to package top, natural convection [6]	Ψ_{JT}	2	2	2	°C/W

1 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

An estimation of the device junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The thermal resistance values used are based on the JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined for the single-layer (1s) board compared to a four-layer board that has two signal layers, a power and a ground plane (2s2p), demonstrate that the effective thermal resistance is not a constant. The thermal resistance depends on the:

- Construction of the application board (number of planes)
- Effective size of the board which cools the component

- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single-layer board is within the normal range for the tightly packed printed circuit board. The value obtained on a board with the internal planes is usually within the normal range if the application board has:

- One oz. (35 micron nominal thickness) internal planes
- Components are well separated
- Overall power dissipation on the board is less than 0.02 W/cm^2

The thermal performance of any component depends on the power dissipation of the surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

T_J = junction temperature (^oC)

T_B = board temperature at the package perimeter ($^oC/W$)

$R_{\theta JB}$ = junction-to-board thermal resistance ($^oC/W$) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, an acceptable value for the junction temperature is predictable. Ensure the application board is similar to the thermal test condition, with the component soldered to a board with internal planes.

The thermal resistance is expressed as the sum of a junction-to-case thermal resistance plus a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ = junction-to-case thermal resistance ($^oC/W$)

$R_{\theta CA}$ = case-to-ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ is device related and is not affected by other factors. The thermal environment can be controlled to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where 90% of the heat flow is through the case to heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case thermal resistance describes when using a heat sink or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature by measuring the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_T = thermocouple temperature on top of the package (^oC)

Ψ_{JT} = thermal characterization parameter ($^oC/W$)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and approximately 1 mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
805 East Middlefield Rd.
Mountain View, CA., 94043
(415) 964-5111

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the web at http://www.jedec.org.

- 1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
- 2. G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” Electronic Packaging and Production, pp. 53–58, March 1998.
- 3. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

3.3 Package

The MPC5553 is available in packaged form. Read the package options in Section 2, "Ordering Information." Refer to Section 4, "Mechanicals," for pinouts and package drawings.

3.4 EMI (Electromagnetic Interference) Characteristics

Table 4. EMI Testing Specifications [1]

Spec	Characteristic	Minimum	Typical	Maximum	Unit
1	Scan range	0.15	—	1000	MHz
2	Operating frequency	—	—	f_{MAX}	MHz
3	V_{DD} operating voltages	—	1.5	—	V
4	V_{DDSYN}, V_{RC33}, V_{DD33}, V_{FLASH}, V_{DDE} operating voltages	—	3.3	—	V
5	V_{PP}, V_{DDEH}, V_{DDA} operating voltages	—	5.0	—	V
6	Maximum amplitude	—	—	14 [2] 32 [3]	dBuV
7	Operating temperature	—	—	25	°C

[1] EMI testing and I/O port waveforms per SAE J1752/3 issued 1995-03. Qualification testing was performed on the MPC5554 and applied to the MPC5500 family as generic EMI performance data.

[2] Measured with the single-chip EMI program.

[3] Measured with the expanded EMI program.

3.5 ESD (Electromagnetic Static Discharge) Characteristics

Table 5. ESD Ratings [1, 2]

Characteristic	Symbol	Value	Unit
ESD for human body model (HBM)		2000	V
HBM circuit description	R1	1500	Ω
	C	100	pF
ESD for field induced charge model (FDCM)		500 (all pins)	V
		750 (corner pins)	
Number of pulses per pin: Positive pulses (HBM) Negative pulses (HBM)	 — —	 1 1	 — —
Interval of pulses	—	1	second

[1] All ESD testing conforms to CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

[2] Device failure is defined as: 'If after exposure to ESD pulses, the device does not meet the device specification requirements, which includes the complete DC parametric and functional testing at room temperature and hot temperature.

3.6 Voltage Regulator Controller (V_{RC}) and Power-On Reset (POR) Electrical Specifications

The following table lists the V_{RC} and POR electrical specifications:

Table 6. VRC/POR Electrical Specifications

Spec	Characteristic		Symbol	Min.	Max.	Units
1	1.5 V (V_{DD}) POR [1]	Negated (ramp up) Asserted (ramp down)	V_{POR15}	1.1 1.1	1.35 1.35	V
2	3.3 V (V_{DDSYN}) POR [1]	Asserted (ramp up) Negated (ramp up) Asserted (ramp down) Negated (ramp down)	V_{POR33}	0.0 2.0 2.0 0.0	0.30 2.85 2.85 0.30	V
3	$\overline{\text{RESET}}$ pin supply (V_{DDEH6}) POR [1, 2]	Negated (ramp up) Asserted (ramp down)	V_{POR5}	2.0 2.0	2.85 2.85	V
4	V_{RC33} voltage	Before V_{RC} allows the pass transistor to start turning on	V_{TRANS_START}	1.0	2.0	V
5		When V_{RC} allows the pass transistor to completely turn on [3, 4]	V_{TRANS_ON}	2.0	2.85	V
6		When the voltage is greater than the voltage at which the V_{RC} keeps the 1.5 V supply in regulation [5, 6]	$V_{VRC33REG}$	3.0	—	V
7	Current can be sourced by V_{RCCTL} at Tj:	– 40° C 25° C 150° C	I_{VRCCTL} [7]	11.0 9.0 7.5	— — —	mA mA mA
8	Voltage differential during power up such that: V_{DD33} can lag V_{DDSYN} or V_{DDEH6}, before V_{DDSYN} and V_{DDEH6} reach the V_{POR33} and V_{POR5} minimums respectively.		V_{DD33_LAG}	—	1.0	V
9	Absolute value of slew rate on power supply pins		—	—	50	V/ms
10	Required gain at Tj: $I_{DD} \div I_{VRCCTL}$ (@ $f_{sys} = f_{MAX}$) [6, 7, 8, 9]	– 40° C 25° C 150° C	BETA[10]	40 45 55	— — 500	— — —

1 On power up, assert $\overline{\text{RESET}}$ before V_{POR15}, V_{POR33}, and V_{POR5} negate (internal POR). $\overline{\text{RESET}}$ must remain asserted until the power supplies are within the operating conditions as specified in Table 9 *DC Electrical Specifications*. On power down, assert $\overline{\text{RESET}}$ before any power supplies fall outside the operating conditions and until the internal POR asserts.

2 V_{IL_S} (Table 9, Spec15) is guaranteed to scale with V_{DDEH6} down to V_{POR5}.

3 Supply full operating current for the 1.5 V supply when the 3.3 V supply reaches this range.

4 It is possible to reach the current limit during ramp up—do not treat this event as short circuit current.

5 At peak current for device.

6 Requires compliance with Freescale's recommended board requirements and transistor recommendations. Board signal traces/routing from the V_{RCCTL} package signal to the base of the external pass transistor and between the emitter of the pass transistor to the V_{DD} package signals must have a maximum of 100 nH inductance and minimal resistance (less than 1 Ω). V_{RCCTL} must have a nominal 1 µF phase compensation capacitor to ground. V_{DD} must have a 20 µF (nominal) bulk capacitor (greater than 4 µF over all conditions, including lifetime). Place high-frequency bypass capacitors consisting of eight 0.01 µF, two 0.1 µF, and one 1 µF capacitors around the package on the V_{DD} supply signals.

7 I_{VRCCTL} is measured at the following conditions: V_{DD} = 1.35 V, V_{RC33} = 3.1 V, V_{VRCCTL} = 2.2 V.

8 Refer to Table 1 for the maximum operating frequency.

[9] Values are based on I_{DD} from high-use applications as explained in the I_{DD} Electrical Specification.
[10] BETA is the worst-case external transistor BETA. It is measured on a per-part basis and calculated as ($I_{DD} \div I_{VRCCTL}$).

3.7 Power-Up/Down Sequencing

Power sequencing between the 1.5 V power supply and V_{DDSYN} or the $\overline{RESET}$ power supplies is required if using an external 1.5 V power supply with V_{RC33} tied to ground (GND). To avoid power-sequencing, V_{RC33} must be powered up within the specified operating range, even if the on-chip voltage regulator controller is not used. Refer to Section 3.7.2, "Power-Up Sequence (VRC33 Grounded)," and Section 3.7.3, "Power-Down Sequence (VRC33 Grounded)."

Power sequencing requires that V_{DD33} must reach a certain voltage where the values are read as ones before the POR signal negates. Refer to Section 3.7.1, "Input Value of Pins During POR Dependent on VDD33."

Although power sequencing is not required between V_{RC33} and V_{DDSYN} during power up, V_{RC33} must not lead V_{DDSYN} by more than 600 mV or lag by more than 100 mV for the V_{RC} stage turn-on to operate within specification. Higher spikes in the emitter current of the pass transistor occur if V_{RC33} leads or lags V_{DDSYN} by more than these amounts. The value of that higher spike in current depends on the board power supply circuitry and the amount of board level capacitance.

Furthermore, when all of the PORs negate, the system clock starts to toggle, adding another large increase of the current consumed by V_{RC33}. If V_{RC33} lags V_{DDSYN} by more than 100 mV, the increase in current consumed can drop V_{DD} low enough to assert the 1.5 V POR again. Oscillations are possible when the 1.5 V POR asserts and stops the system clock, causing the voltage on V_{DD} to rise until the 1.5 V POR negates again. All oscillations stop when V_{RC33} is powered sufficiently.

When powering down, V_{RC33} and V_{DDSYN} have no delta requirement to each other, because the bypass capacitors internal and external to the device are already charged. When not powering up or down, no delta between V_{RC33} and V_{DDSYN} is required for the V_{RC} to operate within specification.

There are no power up/down sequencing requirements to prevent issues such as latch-up, excessive current spikes, and so on. Therefore, the state of the I/O pins during power up and power down varies depending on which supplies are powered.

Table 7 gives the pin state for the sequence cases for all pins with pad type pad_fc (fast type).

Table 7. Pin Status for Fast Pads During the Power Sequence

V_{DDE}	V_{DD33}	V_{DD}	POR	Pin Status for Fast Pad Output Driver pad_fc (fast)
Low	—	—	Asserted	Low
V_{DDE}	Low	Low	Asserted	High
V_{DDE}	Low	V_{DD}	Asserted	High
V_{DDE}	V_{DD33}	Low	Asserted	High impedance (Hi-Z)
V_{DDE}	V_{DD33}	V_{DD}	Asserted	Hi-Z
V_{DDE}	V_{DD33}	V_{DD}	Negated	Functional

Table 8 gives the pin state for the sequence cases for all pins with pad type pad_mh (medium type) and pad_sh (slow type).

Table 8. Pin Status for Medium and Slow Pads During the Power Sequence

V_{DDEH}	V_{DD}	POR	Pin Status for Medium and Slow Pad Output Driver pad_mh (medium) pad_sh (slow)
Low	—	Asserted	Low
V_{DDEH}	Low	Asserted	High impedance (Hi-Z)
V_{DDEH}	V_{DD}	Asserted	Hi-Z
V_{DDEH}	V_{DD}	Negated	Functional

The values in Table 7 and Table 8 do not include the effect of the weak-pull devices on the output pins during power up.

Before exiting the internal POR state, the voltage on the pins goes to high-impedance until POR negates. When the internal POR negates, the functional state of the signal during reset applies and the weak-pull devices (up or down) are enabled as defined in the device *Reference Manual*. If V_{DD} is too low to correctly propagate the logic signals, the weak-pull devices can pull the signals to V_{DDE} and V_{DDEH}.

To avoid this condition, minimize the ramp time of the V_{DD} supply to a time period less than the time required to enable the external circuitry connected to the device outputs.

3.7.1 Input Value of Pins During POR Dependent on V_{DD33}

When powering up the device, V_{DD33} must not lag the latest V_{DDSYN} *or* $\overline{\text{RESET}}$ power pin (V_{DDEH6}) by more than the V_{DD33} lag specification listed in Table 6, spec 8. This avoids accidentally selecting the bypass clock mode because the internal versions of PLLCFG[0:1] and $\overline{\text{RSTCFG}}$ are not powered and therefore cannot read the default state when POR negates. V_{DD33} can lag V_{DDSYN} *or* the $\overline{\text{RESET}}$ power pin (V_{DDEH6}), but cannot lag both by more than the V_{DD33} lag specification. This V_{DD33} lag specification applies during power up only. V_{DD33} has no lead or lag requirements when powering down.

3.7.2 Power-Up Sequence (V_{RC33} Grounded)

The 1.5 V V_{DD} power supply must rise to 1.35 V before the 3.3 V V_{DDSYN} power supply and the $\overline{\text{RESET}}$ power supply rises above 2.0 V. This ensures that digital logic in the PLL for the 1.5 V power supply does not begin to operate below the specified operation range lower limit of 1.35 V. Because the internal 1.5 V POR is disabled, the internal 3.3 V POR or the $\overline{\text{RESET}}$ power POR must hold the device in reset. Since they can negate as low as 2.0 V, V_{DD} must be within specification before the 3.3 V POR and the $\overline{\text{RESET}}$ POR negate.

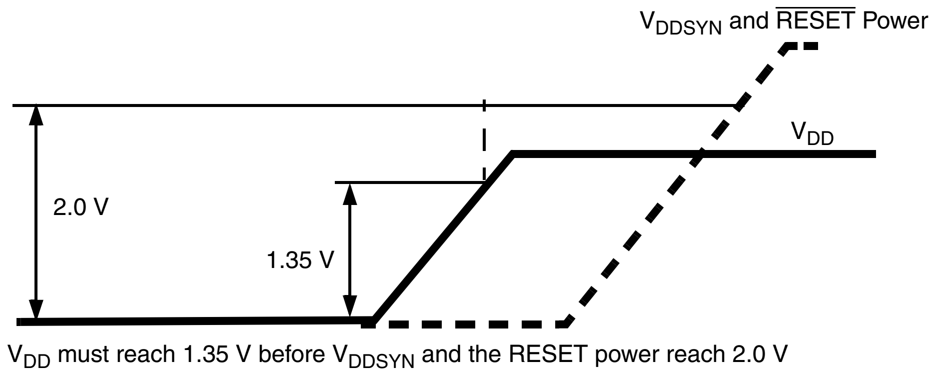


Figure 2. Power-Up Sequence (V_{RC33} Grounded)

3.7.3 Power-Down Sequence (V_{RC33} Grounded)

The only requirement for the power-down sequence with V_{RC33} grounded is if V_{DD} decreases to less than its operating range, V_{DDSYN} or the $\overline{\text{RESET}}$ power must decrease to less than 2.0 V before the V_{DD} power increases to its operating range. This ensures that the digital 1.5 V logic, which is reset only by an ORed POR and can cause the 1.5 V supply to decrease less than its specification value, resets correctly.

3.8 DC Electrical Specifications

Table 9. DC Electrical Specifications ($T_A = T_L – T_H$)

Spec	Characteristic	Symbol	Min	Max.	Unit
1	Core supply voltage (average DC RMS voltage)	V_{DD}	1.35	1.65	V
2	Input/output supply voltage (fast input/output) [1]	V_{DDE}	1.62	3.6	V
3	Input/output supply voltage (slow and medium input/output)	V_{DDEH}	3.0	5.25	V
4	3.3 V input/output buffer voltage	V_{DD33}	3.0	3.6	V
5	Voltage regulator control input voltage	V_{RC33}	3.0	3.6	V
6	Analog supply voltage [2]	V_{DDA}	4.5	5.25	V
8	Flash programming voltage [3]	V_{PP}	4.5	5.25	V
9	Flash read voltage	V_{FLASH}	3.0	3.6	V
10	SRAM standby voltage [4]	V_{STBY}	0.8	1.2	V
11	Clock synthesizer operating voltage	V_{DDSYN}	3.0	3.6	V
12	Fast I/O input high voltage	V_{IH_F}	$0.65 \times V_{DDE}$	$V_{DDE} + 0.3$	V
13	Fast I/O input low voltage	V_{IL_F}	$V_{SS} – 0.3$	$0.35 \times V_{DDE}$	V
14	Medium and slow I/O input high voltage	V_{IH_S}	$0.65 \times V_{DDEH}$	$V_{DDEH} + 0.3$	V
15	Medium and slow I/O input low voltage	V_{IL_S}	$V_{SS} – 0.3$	$0.35 \times V_{DDEH}$	V
16	Fast input hysteresis	V_{HYS_F}	$0.1 \times V_{DDE}$		V

Table 9. DC Electrical Specifications ($T_A = T_L – T_H$) (continued)

Spec	Characteristic	Symbol	Min	Max.	Unit
17	Medium and slow I/O input hysteresis	V_{HYS_S}	0.1 × V_{DDEH}		V
18	Analog input voltage	V_{INDC}	V_{SSA} – 0.3	V_{DDA} + 0.3	V
19	Fast output high voltage (I_{OH_F} = –2.0 mA)	V_{OH_F}	0.8 × V_{DDE}	—	V
20	Slow and medium output high voltage I_{OH_S} = –2.0 mA I_{OH_S} = –1.0 mA	V_{OH_S}	0.80 × V_{DDEH} 0.85 × V_{DDEH}	—	V
21	Fast output low voltage (I_{OL_F} = 2.0 mA)	V_{OL_F}	—	0.2 × V_{DDE}	V
22	Slow and medium output low voltage I_{OL_S} = 2.0 mA I_{OL_S} = 1.0 mA	V_{OL_S}	—	0.20 × V_{DDEH} 0.15 × V_{DDEH}	V
23	Load capacitance (fast I/O) [5] DSC (SIU_PCR[8:9]) = 0b00 = 0b01 = 0b10 = 0b11	C_L	— — — —	10 20 30 50	pF pF pF pF
24	Input capacitance (digital pins)	C_{IN}	—	7	pF
25	Input capacitance (analog pins)	C_{IN_A}	—	10	pF
26	Input capacitance: (Shared digital and analog pins AN[12]_MA[0]_$\overline{SDS}$, AN[13]_MA[1]_SDO, AN[14]_MA[2]_SDI, and AN[15]_FCK)	C_{IN_M}	—	12	pF
27a	Operating current 1.5 V supplies @ 132 MHz: [6, 7] V_{DD} (including V_{DDF} max current) @1.65 V typical use [8, 9] V_{DD} (including V_{DDF} max current) @1.35 V typical use [8, 9] V_{DD} (including V_{DDF} max current) @1.65 V high use [9, 10] V_{DD} (including V_{DDF} max current) @1.35 V high use [9, 10]	I_{DD} I_{DD} I_{DD} I_{DD}	— — — —	460 360 510 410	mA mA mA mA
27b	Operating current 1.5 V supplies @ 114 MHz: [6, 7] V_{DD} (including V_{DDF} max current) @1.65 V typical use [8, 9] V_{DD} (including V_{DDF} max current) @1.35 V typical use [8, 9] V_{DD} (including V_{DDF} max current) @1.65 V high use [9, 10] V_{DD} (including V_{DDF} max current) @1.35 V high use [9, 10]	I_{DD} I_{DD} I_{DD} I_{DD}	— — — —	410 310 460 370	mA mA mA mA
27c	Operating current 1.5 V supplies @ 82 MHz: [6, 7] V_{DD} (including V_{DDF} max current) @1.65 V typical use [8, 9] V_{DD} (including V_{DDF} max current) @1.35 V typical use [8, 9] V_{DD} (including V_{DDF} max current) @1.65 V high use [9, 10] V_{DD} (including V_{DDF} max current) @1.35 V high use [9, 10]	I_{DD} I_{DD} I_{DD} I_{DD}	— — — —	330 225 385 290	mA mA mA mA

Table 9. DC Electrical Specifications ($T_A = T_L – T_H$) (continued)

Spec	Characteristic	Symbol	Min	Max.	Unit
27d	Refer to Figure 3 for an interpolation of this data.[11] I_{DD_STBY} @ 25° C V_{STBY} @ 0.8 V V_{STBY} @ 1.0 V V_{STBY} @ 1.2 V I_{DD_STBY} @ 60° C V_{STBY} @ 0.8 V V_{STBY} @ 1.0 V V_{STBY} @ 1.2 V I_{DD_STBY} @ 150° C (Tj) V_{STBY} @ 0.8 V V_{STBY} @ 1.0 V V_{STBY} @ 1.2 V	 I_{DD_STBY} I_{DD_STBY} I_{DD_STBY} I_{DD_STBY} I_{DD_STBY} I_{DD_STBY} I_{DD_STBY} I_{DD_STBY} I_{DD_STBY}	 — — — — — — — — —	 20 30 50 70 100 200 1200 1500 2000	 µA µA µA µA µA µA µA µA µA
28	Operating current 3.3 V supplies @ f_{MAX} MHz V_{DD33} [12]	 I_{DD_33}	 —	 2 + (values derived from procedure of footnote [12])	 mA
	V_{FLASH}	I_{VFLASH}	—	10	mA
	V_{DDSYN}	I_{DDSYN}	—	15	mA
29	Operating current 5.0 V supplies (12 MHz ADCLK): V_{DDA} ($V_{DDA0} + V_{DDA1}$) Analog reference supply current (V_{RH}, V_{RL}) V_{PP}	 I_{DD_A} I_{REF} I_{PP}	 — — —	 20.0 1.0 25.0	 mA mA mA
30	Operating current V_{DDE} supplies: [13] V_{DDEH1} V_{DDE2} V_{DDE3} V_{DDEH4} V_{DDE5} V_{DDEH6} V_{DDE7} V_{DDEH8} V_{DDEH9}	 I_{DD1} I_{DD2} I_{DD3} I_{DD4} I_{DD5} I_{DD6} I_{DD7} I_{DD8} I_{DD9}	 — — — — — — — — —	 Refer to Footnote [13]	 mA mA mA mA mA mA mA mA mA
31	Fast I/O weak pullup current [14] 1.62–1.98 V 2.25–2.75 V 3.00–3.60 V	I_{ACT_F}	 10 20 20	 110 130 170	 µA µA µA
	Fast I/O weak pulldown current [14] 1.62–1.98 V 2.25–2.75 V 3.00–3.60 V		 10 20 20	 100 130 170	 µA µA µA

Table 9. DC Electrical Specifications ($T_A = T_L – T_H$) (continued)

Spec	Characteristic	Symbol	Min	Max.	Unit
32	Slow and medium I/O weak pullup/down current [14] 3.0–3.6 V 4.5–5.5 V	I_{ACT_S}	 10 20	 150 170	 µA µA
33	I/O input leakage current [15]	I_{INACT_D}	–2.5	2.5	µA
34	DC injection current (per pin)	I_{IC}	–2.0	2.0	mA
35	Analog input current, channel off [16]	I_{INACT_A}	–150	150	nA
35a	Analog input current, shared analog / digital pins (AN[12], AN[13], AN[14], AN[15])	I_{INACT_AD}	–2.5	2.5	µA
36	V_{SS} to V_{SSA} differential voltage [17]	$V_{SS} – V_{SSA}$	–100	100	mV
37	Analog reference low voltage	V_{RL}	$V_{SSA} – 0.1$	$V_{SSA} + 0.1$	V
38	V_{RL} differential voltage	$V_{RL} – V_{SSA}$	–100	100	mV
39	Analog reference high voltage	V_{RH}	$V_{DDA} – 0.1$	$V_{DDA} + 0.1$	V
40	V_{REF} differential voltage	$V_{RH} – V_{RL}$	4.5	5.25	V
41	V_{SSSYN} to V_{SS} differential voltage	$V_{SSSYN} – V_{SS}$	–50	50	mV
42	V_{RCVSS} to V_{SS} differential voltage	$V_{RCVSS} – V_{SS}$	–50	50	mV
43	V_{DDF} to V_{DD} differential voltage	$V_{DDF} – V_{DD}$	–100	100	mV
43a	V_{RC33} to V_{DDSYN} differential voltage	$V_{RC33} – V_{DDSYN}$	–0.1	0.1 [18]	V
44	Analog input differential signal range (with common mode 2.5 V)	V_{IDIFF}	–2.5	2.5	V
45	Operating temperature range, ambient (packaged)	$T_A = (T_L$ to $T_H)$	T_L	T_H	°C
46	Slew rate on power-supply pins	—	—	50	V/ms

1 V_{DDE2} and V_{DDE3} are limited to 2.25–3.6 V only if EBTS = 0; V_{DDE2} and V_{DDE3} have a range of 1.6–3.6 V if EBTS = 1.
2 | $V_{DDA0} – V_{DDA1}$ | must be < 0.1 V.
3 V_{PP} can drop to 3.0 V during read operations.
4 If standby operation is not required, connect V_{STBY} to ground.
5 Applies to CLKOUT, external bus pins, and Nexus pins.
6 Maximum average RMS DC current.
7 Figure 3 shows an illustration of the I_{DD_STBY} values interpolated for these temperature values.
8 Average current measured on Automotive benchmark.
9 Peak currents can be higher on specialized code.
10 High use current measured while running optimized SPE assembly code with all code and data 100% locked in cache (0% miss rate) with all channels of the eMIOS and eTPU running autonomously, plus the eDMA transferring data continuously from SRAM to SRAM. Higher currents are possible if an idle loop that crosses cache lines is run from cache. Design and write code to avoid this condition.
11 Figure 3 shows an illustration of the I_{DD_STBY} values interpolated for these temperature values.
12 Power requirements for the V_{DD33} supply depend on the frequency of operation, load of all I/O pins, and the voltages on the I/O segments. Refer to Table 11 for values to calculate the power dissipation for a specific operation.
13 Power requirements for each I/O segment are dependent on the frequency of operation and load of the I/O pins on a particular I/O segment, and the voltage of the I/O segment. Refer to Table 10 for values to calculate power dissipation for specific operation. The total power consumption of an I/O segment is the sum of the individual power consumptions for each pin on the segment.
14 Absolute value of current, measured at V_{IL} and V_{IH}.

15 Weak pullup/down inactive. Measured at V_{DDE} = 3.6 V and V_{DDEH} = 5.25 V. Applies to pad types: pad_fc, pad_sh, and pad_mh.
16 Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 °C to 12 °C, in the ambient temperature range of 50 °C to 125 °C. Applies to pad types: pad_a and pad_ae.
17 V_{SSA} refers to both V_{SSA0} and V_{SSA1}. $| V_{SSA0} – V_{SSA1} |$ must be < 0.1 V.
18 Up to 0.6 V during power up and power down.

Figure 3 shows an approximate interpolation of the I_{STBY} worst-case specification to estimate values at different voltages and temperatures. The vertical lines shown at 25 °C, 60 °C, and 150 °C in Figure 3 are the I_{DD_STBY} specifications (27d) listed in Table 9.

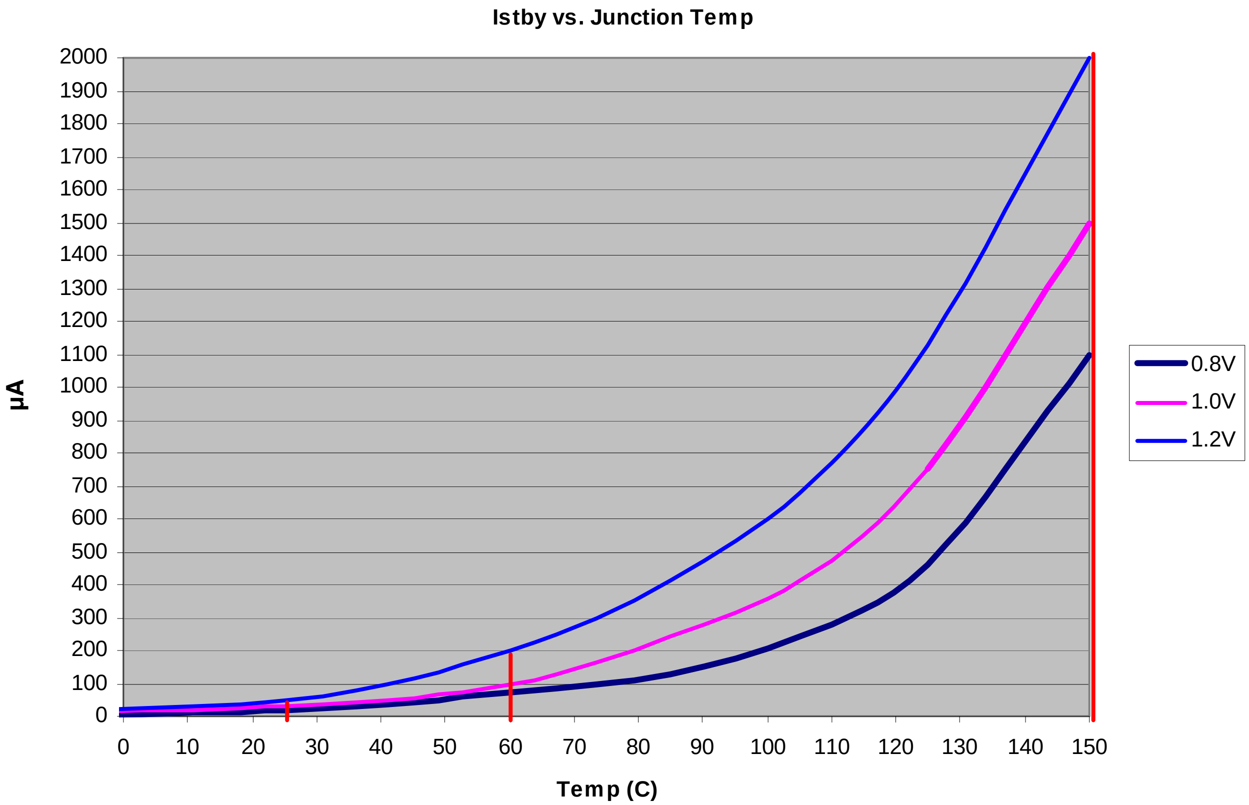


Figure 3. I_{STBY} Worst-case Specifications

3.8.1 I/O Pad Current Specifications

The power consumption of an I/O segment depends on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a segment. The output pin current can be calculated from Table 10 based on the voltage, frequency, and load on the pin. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 10.

Table 10. I/O Pad Average DC Current ($T_A = T_L – T_H$)[1]

Spec	Pad Type	Symbol	Frequency (MHz)	Load[2] (pF)	Voltage (V)	Drive Select / Slew Rate Control Setting	Current (mA)
1	Slow	I_{DRV_SH}	25	50	5.25	11	8.0
2			10	50	5.25	01	3.2
3			2	50	5.25	00	0.7
4			2	200	5.25	00	2.4
5	Medium	I_{DRV_MH}	50	50	5.25	11	17.3
6			20	50	5.25	01	6.5
7			3.33	50	5.25	00	1.1
8			3.33	200	5.25	00	3.9
9	Fast	I_{DRV_FC}	66	10	3.6	00	2.8
10			66	20	3.6	01	5.2
11			66	30	3.6	10	8.5
12			66	50	3.6	11	11.0
13			66	10	1.98	00	1.6
14			66	20	1.98	01	2.9
15			66	30	1.98	10	4.2
16			66	50	1.98	11	6.7
17			56	10	3.6	00	2.4
18			56	20	3.6	01	4.4
19			56	30	3.6	10	7.2
20			56	50	3.6	11	9.3
21			56	10	1.98	00	1.3
22			56	20	1.98	01	2.5
23			56	30	1.98	10	3.5
24			56	50	1.98	11	5.7
25			40	10	3.6	00	1.7
26			40	20	3.6	01	3.1
27			40	30	3.6	10	5.1
28			40	50	3.6	11	6.6
29			40	10	1.98	00	1.0
30			40	20	1.98	01	1.8
31			40	30	1.98	10	2.5
32			40	50	1.98	11	4.0

1 These values are estimates from simulation and are not tested. Currents apply to output pins only.

2 All loads are lumped.

3.8.2 I/O Pad V_{DD33} Current Specifications

The power consumption of the V_{DD33} supply dependents on the usage of the pins on all I/O segments. The power consumption is the sum of all input and output pin V_{DD33} currents for all I/O segments. The output pin V_{DD33} current can be calculated from Table 11 based on the voltage, frequency, and load on all fast (pad_fc) pins. The input pin V_{DD33} current can be calculated from Table 11 based on the voltage, frequency, and load on all pad_sh and pad_mh pins. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 11.

Table 11. V_{DD33} Pad Average DC Current ($T_A = T_L – T_H$) [1]

Spec	Pad Type	Symbol	Frequency (MHz)	Load [2] (pF)	V_{DD33} (V)	V_{DDE} (V)	Drive Select	Current (mA)
Inputs								
1	Slow	I_{33_SH}	66	0.5	3.6	5.5	NA	0.003
2	Medium	I_{33_MH}	66	0.5	3.6	5.5	NA	0.003
Outputs								
3	Fast	I_{33_FC}	66	10	3.6	3.6	00	0.35
4			66	20	3.6	3.6	01	0.53
5			66	30	3.6	3.6	10	0.62
6			66	50	3.6	3.6	11	0.79
7			66	10	3.6	1.98	00	0.35
8			66	20	3.6	1.98	01	0.44
9			66	30	3.6	1.98	10	0.53
10			66	50	3.6	1.98	11	0.70
11			56	10	3.6	3.6	00	0.30
12			56	20	3.6	3.6	01	0.45
13			56	30	3.6	3.6	10	0.52
14			56	50	3.6	3.6	11	0.67
15			56	10	3.6	1.98	00	0.30
16			56	20	3.6	1.98	01	0.37
17			56	30	3.6	1.98	10	0.45
18			56	50	3.6	1.98	11	0.60
19			40	10	3.6	3.6	00	0.21
20			40	20	3.6	3.6	01	0.31
21			40	30	3.6	3.6	10	0.37
22			40	50	3.6	3.6	11	0.48
23			40	10	3.6	1.98	00	0.21
24			40	20	3.6	1.98	01	0.27
25			40	30	3.6	1.98	10	0.32
26			40	50	3.6	1.98	11	0.42

[1] These values are estimated from simulation and not tested. Currents apply to output pins for the fast pads only and to input pins for the slow and medium pads only.

[2] All loads are lumped.

3.9 Oscillator and FMPLL Electrical Characteristics

Table 12. FMPLL Electrical Specifications

(V_{DDSYN} = 3.0–3.6 V; V_{SS} = V_{SSSYN} = 0.0 V; T_A = T_L to T_H)

Spec	Characteristic	Symbol	Minimum	Maximum	Unit
1	PLL reference frequency range: [1] Crystal reference External reference Dual controller (1:1 mode)	 $f_{ref\_crystal}$ f_{ref_ext} $f_{ref\_1:1}$	 8 8 24	 20 20 $f_{sys} \div 2$	MHz
2	System frequency [2]	f_{sys}	$f_{ICO(MIN)} \div 2^{RFD}$	f_{MAX} [3]	MHz
3	System clock period	t_{CYC}	—	$1 \div f_{sys}$	ns
4	Loss of reference frequency [4]	f_{LOR}	100	1000	kHz
5	Self-clocked mode (SCM) frequency [5]	f_{SCM}	7.4	17.5	MHz
6	EXTAL input high voltage crystal mode [6] All other modes [dual controller (1:1), bypass, external reference]	V_{IHEXT} V_{IHEXT}	V_{XTAL} + 0.4 V ($V_{DDE5} \div 2$) + 0.4 V	— —	V V
7	EXTAL input low voltage crystal mode [7] All other modes [dual controller (1:1), bypass, external reference]	V_{ILEXT} V_{ILEXT}	— —	V_{XTAL} – 0.4 V ($V_{DDE5} \div 2$) – 0.4 V	V V
8	XTAL current [8]	I_{XTAL}	0.8	3	mA
9	Total on-chip stray capacitance on XTAL	C_{S_XTAL}	—	1.5	pF
10	Total on-chip stray capacitance on EXTAL	C_{S_EXTAL}	—	1.5	pF
11	Crystal manufacturer’s recommended capacitive load	C_L	Refer to crystal specification	Refer to crystal specification	pF
12	Discrete load capacitance to connect to EXTAL	C_{L_EXTAL}	—	$(2 \times C_L) - C_{S\_EXTAL} - C_{PCB\_EXTAL}$ [9]	pF
13	Discrete load capacitance to connect to XTAL	C_{L_XTAL}	—	$(2 \times C_L) - C_{S\_XTAL} - C_{PCB\_XTAL}$ [9]	pF
14	PLL lock time [10]	t_{lpll}	—	750	µs
15	Dual controller (1:1) clock skew (between CLKOUT and EXTAL) [11, 12]	t_{skew}	–2	2	ns
16	Duty cycle of reference	t_{DC}	40	60	%
17	Frequency unLOCK range	f_{UL}	–4.0	4.0	% f_{SYS}
18	Frequency LOCK range	f_{LCK}	–2.0	2.0	% f_{SYS}

Table 12. FMPLL Electrical Specifications (continued)

(V_{DDSYN} = 3.0–3.6 V; V_{SS} = V_{SSSYN} = 0.0 V; T_A = T_L to T_H)

Spec	Characteristic	Symbol	Minimum	Maximum	Unit
19	CLKOUT period jitter, measured at f_{SYS} max: [13, 14] Peak-to-peak jitter (clock edge to clock edge) Long term jitter (averaged over a 2 ms interval)	C_{JITTER}	 — —	 5.0 0.01	% f_{CLKOUT}
20	Frequency modulation range limit [15] (do not exceed f_{sys} maximum)	C_{MOD}	0.8	2.4	$\%f_{SYS}$
21	ICO frequency $f_{ico} = [f_{ref\_crystal} \times (MFD + 4)] \div (PREDIV + 1)$ [16] $f_{ico} = [f_{ref\_ext} \times (MFD + 4)] \div (PREDIV + 1)$	f_{ico}	48	f_{MAX}	MHz
22	Predivider output frequency (to PLL)	f_{PREDIV}	4	20 [17]	MHz

1 Nominal crystal and external reference values are worst-case not more than 1%. The device operates correctly if the frequency remains within ± 5% of the specification limit. This tolerance range allows for a slight frequency drift of the crystals over time. The designer must thoroughly understand the drift margin of the source clock.

2 All internal registers retain data at 0 Hz.

3 Up to the maximum frequency rating of the device (refer to Table 1).

4 Loss of reference frequency is defined as the reference frequency detected internally, which transitions the PLL into self-clocked mode.

5 The PLL operates at self-clocked mode (SCM) frequency when the reference frequency falls below f_{LOR}. SCM frequency is measured on the CLKOUT ball with the divider set to divide-by-two of the system clock.
NOTE: In SCM, the MFD and PREDIV have no effect and the RFD is bypassed.

6 Use the EXTAL input high voltage parameter when using the FlexCAN oscillator in crystal mode (no quartz crystals or resonators). ($V_{extal} - V_{xtal}$) must be ≥ 400 mV for the oscillator's comparator to produce the output clock.

7 Use the EXTAL input low voltage parameter when using the FlexCAN oscillator in crystal mode (no quartz crystals or resonators). ($V_{xtal} - V_{extal}$) must be ≥ 400 mV for the oscillator's comparator to produce the output clock.

8 I_{xtal} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded.

9 C_{PCB_EXTAL} and C_{PCB_XTAL} are the measured PCB stray capacitances on EXTAL and XTAL, respectively.

10 This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR). From power up with crystal oscillator reference, the lock time also includes the crystal startup time.

11 PLL is operating in 1:1 PLL mode.

12 V_{DDE} = 3.0–3.6 V.

13 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDSYN} and V_{SSSYN} and variation in crystal oscillator frequency increase the jitter percentage for a given interval. CLKOUT divider is set to divide-by-two.

14 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of (jitter + Cmod).

15 Modulation depth selected must not result in f_{sys} value greater than the f_{sys} maximum specified value.

16 $f_{sys} = f_{ico} \div (2^{RFD})$

17 Maximum value for dual controller (1:1) mode is ($f_{MAX} \div 2$) with the predivider set to 1 (FMPLL_SYNCR[PREDIV] = 0b001).

3.10 eQADC Electrical Characteristics

Table 13. eQADC Conversion Specifications ($T_A = T_L$ to T_H)

Spec	Characteristic	Symbol	Minimum	Maximum	Unit
1	ADC clock (ADCLK) frequency [1]	F_{ADCLK}	1	12	MHz
2	Conversion cycles Differential Single ended	CC	 13 + 2 (15) 14 + 2 (16)	 13 + 128 (141) 14 + 128 (142)	ADCLK cycles
3	Stop mode recovery time [2]	T_{SR}	10	—	µs
4	Resolution [3]	—	1.25	—	mV
5	INL: 6 MHz ADC clock	INL6	–4	4	Counts [3]
6	INL: 12 MHz ADC clock	INL12	–8	8	Counts
7	DNL: 6 MHz ADC clock	DNL6	–3 [4]	3 [4]	Counts
8	DNL: 12 MHz ADC clock	DNL12	–6 [4]	6 [4]	Counts
9	Offset error with calibration	OFFWC	–4 [5]	4 [5]	Counts
10	Full-scale gain error with calibration	GAINWC	–8 [6]	8 [6]	Counts
11	Disruptive input injection current [7, 8, 9, 10]	I_{INJ}	–1	1	mA
12	Incremental error due to injection current. All channels are 10 kΩ < Rs <100 kΩ Channel under test has Rs = 10 kΩ, $I_{INJ} = I_{INJMAX}, I_{INJMIN}$	E_{INJ}	–4	4	Counts
13	Total unadjusted error (TUE) for single ended conversions with calibration [11, 12, 13, 14, 15]	TUE	–4	4	Counts

1 Conversion characteristics vary with F_{ADCLK} rate. Reduced conversion accuracy occurs at maximum F_{ADCLK} rate. The maximum value is based on 800 KS/s and the minimum value is based on 20 MHz oscillator clock frequency divided by a maximum 16 factor.

2 Stop mode recovery time begins when the ADC control register enable bits are set until the ADC is ready to perform conversions.

3 At $V_{RH} – V_{RL}$ = 5.12 V, one least significant bit (LSB) = 1.25, mV = one count.

4 Guaranteed 10-bit mono tonicity.

5 The absolute value of the offset error without calibration ≤ 100 counts.

6 The absolute value of the full scale gain error without calibration ≤ 120 counts.

7 Below disruptive current conditions, the channel being stressed has conversion values of: 0x3FF for analog inputs greater than V_{RH}, and 0x000 for values less than V_{RL}. This assumes that $V_{RH} \leq V_{DDA}$ and $V_{RL} \geq V_{SSA}$ due to the presence of the sample amplifier. Other channels are not affected by non-disruptive conditions.

8 Exceeding the limit can cause a conversion error on both stressed and unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.

9 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP} = V_{DDA}$ + 0.5 V and $V_{NEGCLAMP}$ = – 0.3 V, then use the larger of the calculated values.

10 This condition applies to two adjacent pads on the internal pad.

11 The TUE specification is always less than the sum of the INL, DNL, offset, and gain errors due to canceling errors.

12 TUE does not apply to differential conversions.

13 Measured at 6 MHz ADC clock. TUE with a 12 MHz ADC clock is: –16 counts < TUE < 16 counts.

14 TUE includes all internal device errors such as internal reference variation (75% Ref, 25% Ref).

15 Depending on the input impedance, the analog input leakage current (Table 9. *DC Electrical Specifications*, spec 35a) can affect the actual TUE measured on analog channels AN[12], AN[13], AN[14], AN[15].

3.11 H7Fa Flash Memory Electrical Characteristics

Table 14. Flash Program and Erase Specifications ($T_A = T_L$ to T_H)

Spec	Flash Program Characteristic	Symbol	Min.	Typical [1]	Initial Max. [2]	Max. [3]	Unit
3	Doubleword (64 bits) program time [4]	$T_{dwprogram}$	—	10	—	500	µs
4	Page program time [4]	$T_{pprogram}$	—	22	44 [5]	500	µs
7	16 KB block pre-program and erase time	$T_{16kpperase}$	—	265	400	5000	ms
9	48 KB block pre-program and erase time	$T_{48kpperase}$	—	345	400	5000	ms
10	64 KB block pre-program and erase time	$T_{64kpperase}$	—	415	500	5000	ms
8	128 KB block pre-program and erase time	$T_{128kpperase}$	—	500	1250	7500	ms
11	Minimum operating frequency for program and erase operations [6]	—	25	—	—	—	MHz

1 Typical program and erase times are calculated at 25 °C operating temperature using nominal supply values.

2 Initial factory condition: ≤ 100 program/erase cycles, 25 °C, using a typical supply voltage measured at a minimum system frequency of 80 MHz.

3 The maximum erase time occurs after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.

4 Actual hardware programming times. This does not include software overhead.

5 Page size is 256 bits (8 words).

6 The read frequency of the flash can range up to the maximum operating frequency. There is no minimum read frequency condition.

Table 15. Flash EEPROM Module Life ($T_A = T_L$ to T_H)

Spec	Characteristic	Symbol	Min.	Typical [1]	Unit
1a	Number of program/erase cycles per block for 16 KB, 48 KB, and 64 KB blocks over the operating temperature range (T_J)	P/E	100,000	—	cycles
1b	Number of program/erase cycles per block for 128 KB blocks over the operating temperature range (T_J)	P/E	1000	100,000	cycles
2	Data retention Blocks with 0–1,000 P/E cycles Blocks with 1,001–100,000 P/E cycles	Retention	 20 5	 — —	years

1 Typical endurance is evaluated at 25° C. Product qualification is performed to the minimum specification. For additional information on the Freescale definition of typical endurance, refer to engineering bulletin EB619 *Typical Endurance for Nonvolatile Memory.*

Table 16 shows the FLASH_BIU settings versus frequency of operation. Refer to the device reference manual for definitions of these bit fields.

Table 16. FLASH_BIU Settings vs. Frequency of Operation [1]

Maximum Frequency (MHz)	APC	RWSC	WWSC	DPFEN [2]	IPFEN [2]	PFLIM [3]	BFEN [4]
Up to and including 82 MHz [5]	0b001	0b001	0b01	0b00 0b01 0b11	0b00 0b01 0b11	0b000 to 0b110	0b0 0b1
Up to and including 102 MHz [6]	0b001	0b010	0b01	0b00 0b01 0b11	0b00 0b01 0b11	0b000 to 0b110	0b0 0b1
Up to and including 132 MHz [7]	0b010	0b011	0b01	0b00 0b01 0b11	0b00 0b01 0b11	0b000 to 0b110	0b0 0b1
Default setting after reset	0b111	0b111	0b11	0b00	0b00	0b000	0b0

1 Illegal combinations exist. Use entries from the same row in this table.
2 For maximum flash performance, set to 0b11.
3 For maximum flash performance, set to 0b110.
4 For maximum flash performance, set to 0b1.
5 82 MHz parts allow for 80 MHz system clock + 2% frequency modulation (FM).
6 102 MHz parts allow for 100 MHz system clock + 2% FM.
7 132 MHz parts allow for 128 MHz system clock + 2% FM.

3.12 AC Specifications

3.12.1 Pad AC Specifications

Table 17. Pad AC Specifications (V_{DDEH} = 5.0 V, V_{DDE} = 1.8 V) [1]

Spec	Pad	SRC / DSC (binary)	Out Delay [2, 3, 4] (ns)	Rise / Fall [4, 5] (ns)	Load Drive (pF)
1	Slow high voltage (SH)	11	26	15	50
			82	60	200
		01	75	40	50
			137	80	200
		00	377	200	50
			476	260	200
2	Medium high voltage (MH)	11	16	8	50
			43	30	200
		01	34	15	50
			61	35	200
		00	192	100	50
			239	125	200

Table 17. Pad AC Specifications (V_{DDEH} = 5.0 V, V_{DDE} = 1.8 V) [1] (continued)

Spec	Pad	SRC / DSC (binary)	Out Delay [2, 3, 4] (ns)	Rise / Fall [4, 5] (ns)	Load Drive (pF)
3	Fast	00	3.1	2.7	10
		01		2.5	20
		10		2.4	30
		11		2.3	50
4	Pullup/down (3.6 V max)	—	—	7500	50
5	Pullup/down (5.5 V max)	—	—	9000	50

1 These are worst-case values that are estimated from simulation (not tested). The values in the table are simulated at: V_{DD} = 1.35–1.65 V; V_{DDE} = 1.62–1.98 V; V_{DDEH} = 4.5–5.25 V; V_{DD33} and V_{DDSYN} = 3.0–3.6 V; and T_A = T_L to T_H.
2 This parameter is supplied for reference and is guaranteed by design (not tested).
3 The output delay is shown in Figure 4. To calculate the output delay with respect to the system clock, add a maximum of one system clock to the output delay.
4 The output delay and rise and fall are measured to 20% or 80% of the respective signal.
5 This parameter is guaranteed by characterization rather than 100% tested.

Table 18. Derated Pad AC Specifications (V_{DDEH} = 3.3 V, V_{DDE} = 3.3 V) [1]

Spec	Pad	SRC/DSC (binary)	Out Delay [2, 3, 4] (ns)	Rise / Fall [3, 5] (ns)	Load Drive (pF)
1	Slow high voltage (SH)	11	39	23	50
			120	87	200
		01	101	52	50
			188	111	200
		00	507	248	50
			597	312	200
2	Medium high voltage (MH)	11	23	12	50
			64	44	200
		01	50	22	50
			90	50	200
		00	261	123	50
			305	156	200
3	Fast	00	3.2	2.4	10
		01		2.2	20
		10		2.1	30
		11		2.1	50
4	Pullup/down (3.6 V max)	—	—	7500	50
5	Pullup/down (5.5 V max)	—	—	9500	50

1 These are worst-case values that are estimated from simulation (not tested). The values in the table are simulated at: V_{DD} = 1.35–1.65 V; V_{DDE} = 3.0–3.6 V; V_{DDEH} = 3.0–3.6 V; V_{DD33} and V_{DDSYN} = 3.0–3.6 V; and T_A = T_L to T_H.
2 This parameter is supplied for reference and guaranteed by design (not tested).

3 The output delay, and the rise and fall, are calculated to 20% or 80% of the respective signal.

4 The output delay is shown in Figure 4. To calculate the output delay with respect to the system clock, add a maximum of one system clock to the output delay.

5 This parameter is guaranteed by characterization rather than 100% tested.

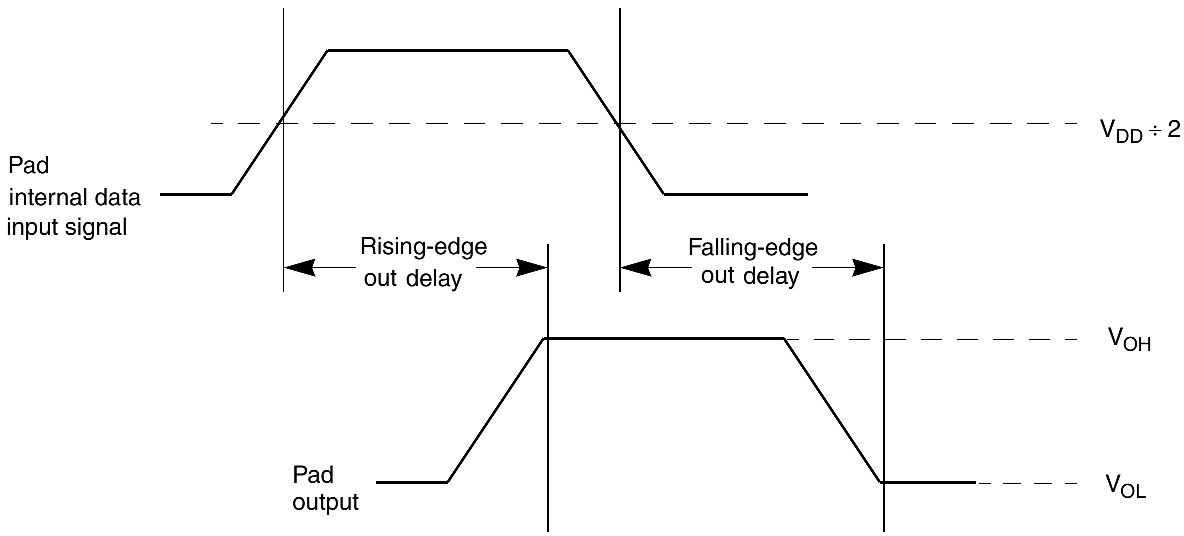


Figure 4. Pad Output Delay

3.13 AC Timing

3.13.1 Reset and Configuration Pin Timing

Table 19. Reset and Configuration Pin Timing [1]

Spec	Characteristic	Symbol	Min.	Max.	Unit
1	$\overline{\text{RESET}}$ pulse width	t_{RPW}	10	—	t_{CYC}
2	$\overline{\text{RESET}}$ glitch detect pulse width	t_{GPW}	2	—	t_{CYC}
3	PLLCFG, BOOTCFG, WKPCFG, $\overline{\text{RSTCFG}}$ setup time to $\overline{\text{RSTOUT}}$ valid	t_{RCSU}	10	—	t_{CYC}
4	PLLCFG, BOOTCFG, WKPCFG, $\overline{\text{RSTCFG}}$ hold time from $\overline{\text{RSTOUT}}$ valid	t_{RCH}	0	—	t_{CYC}

1 Reset timing specified at: V_{DDEH} = 3.0–5.25 V and $T_A = T_L$ to T_H.

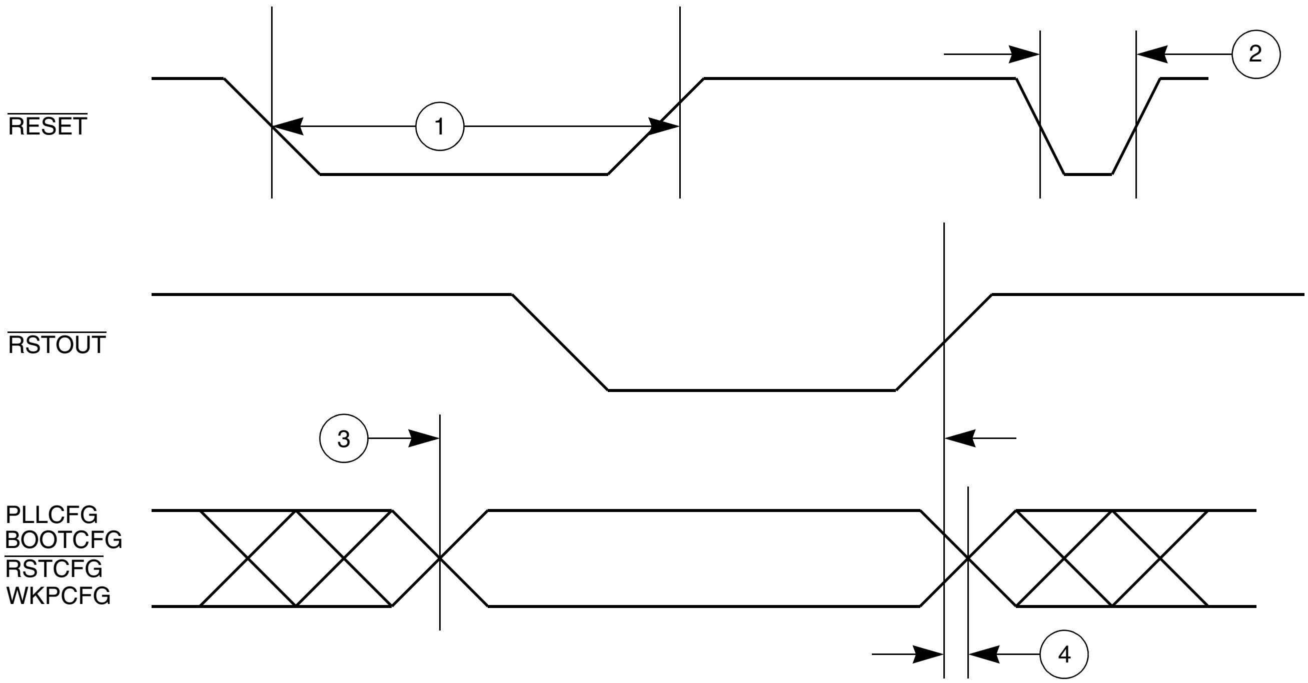


Figure 5. Reset and Configuration Pin Timing

3.13.2 IEEE 1149.1 Interface Timing

Table 20. JTAG Pin AC Electrical Characteristics [1]

Spec	Characteristic	Symbol	Min.	Max.	Unit
1	TCK cycle time	t_{JCYC}	100	—	ns
2	TCK clock pulse width (measured at $V_{DDE} \div 2$)	t_{JDC}	40	60	ns
3	TCK rise and fall times (40% to 70%)	$t_{TCKRISE}$	—	3	ns
4	TMS, TDI data setup time	t_{TMSS}, t_{TDIS}	5	—	ns
5	TMS, TDI data hold time	t_{TMSH}, t_{TDIH}	25	—	ns
6	TCK low to TDO data valid	t_{TDOV}	—	20	ns
7	TCK low to TDO data invalid	t_{TDOI}	0	—	ns
8	TCK low to TDO high impedance	t_{TDOHZ}	—	20	ns
9	JCOMP assertion time	t_{JCMPPW}	100	—	ns
10	JCOMP setup time to TCK low	t_{JCMPS}	40	—	ns
11	TCK falling-edge to output valid	t_{BSDV}	—	50	ns
12	TCK falling-edge to output valid out of high impedance	t_{BSDVZ}	—	50	ns
13	TCK falling-edge to output high impedance (Hi-Z)	t_{BSDHZ}	—	50	ns
14	Boundary scan input valid to TCK rising-edge	t_{BSDST}	50	—	ns
15	TCK rising-edge to boundary scan input invalid	t_{BSDHT}	50	—	ns

[1] These specifications apply to JTAG boundary scan only. JTAG timing specified at: V_{DDE} = 3.0–3.6 V and $T_A = T_L$ to T_H. Refer to Table 21 for Nexus specifications.

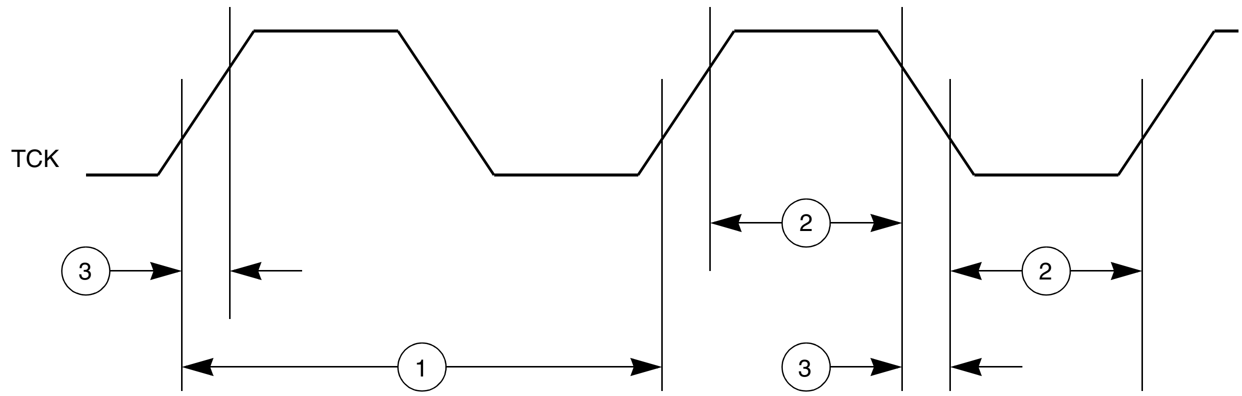


Figure 6. JTAG Test Clock Input Timing

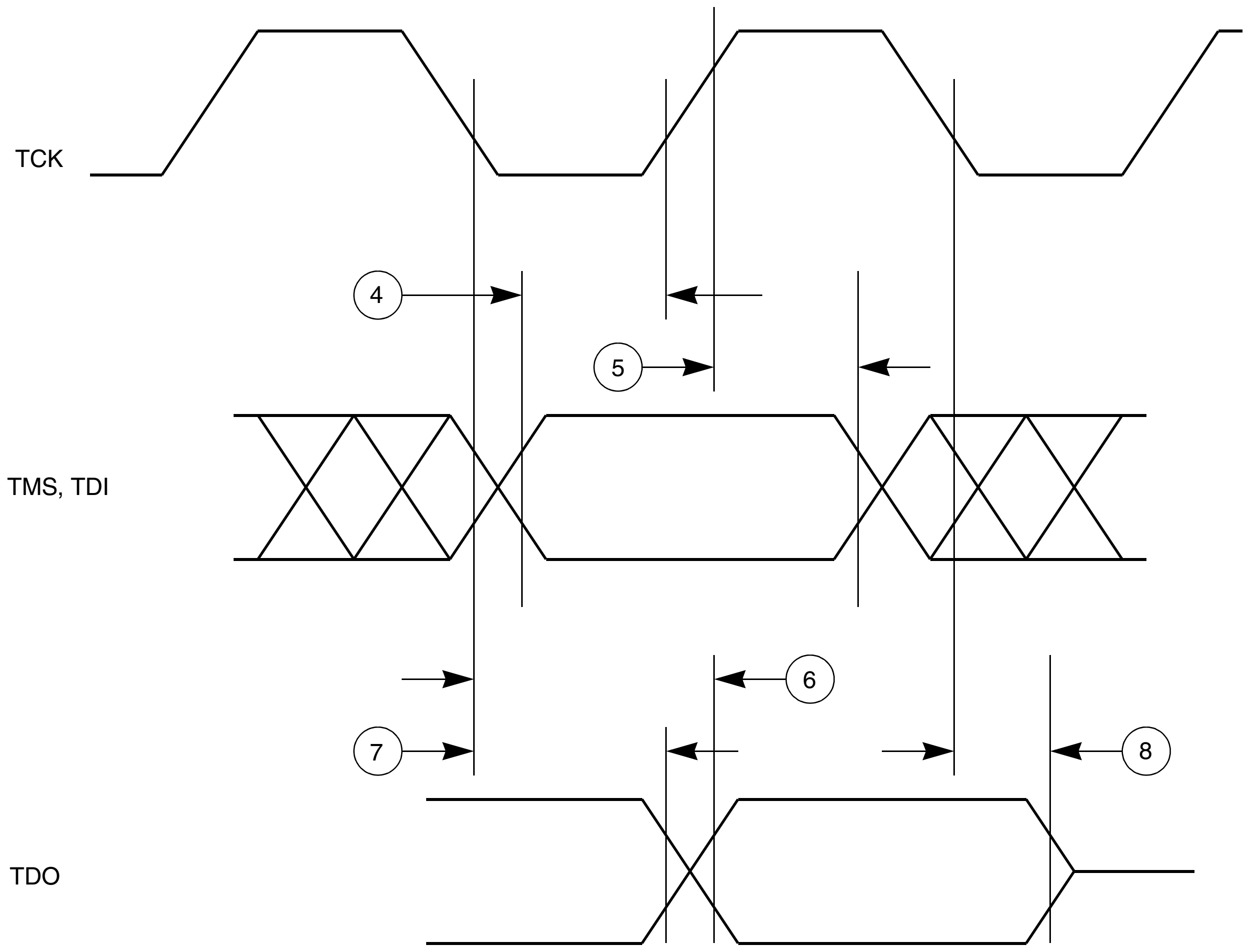


Figure 7. JTAG Test Access Port Timing

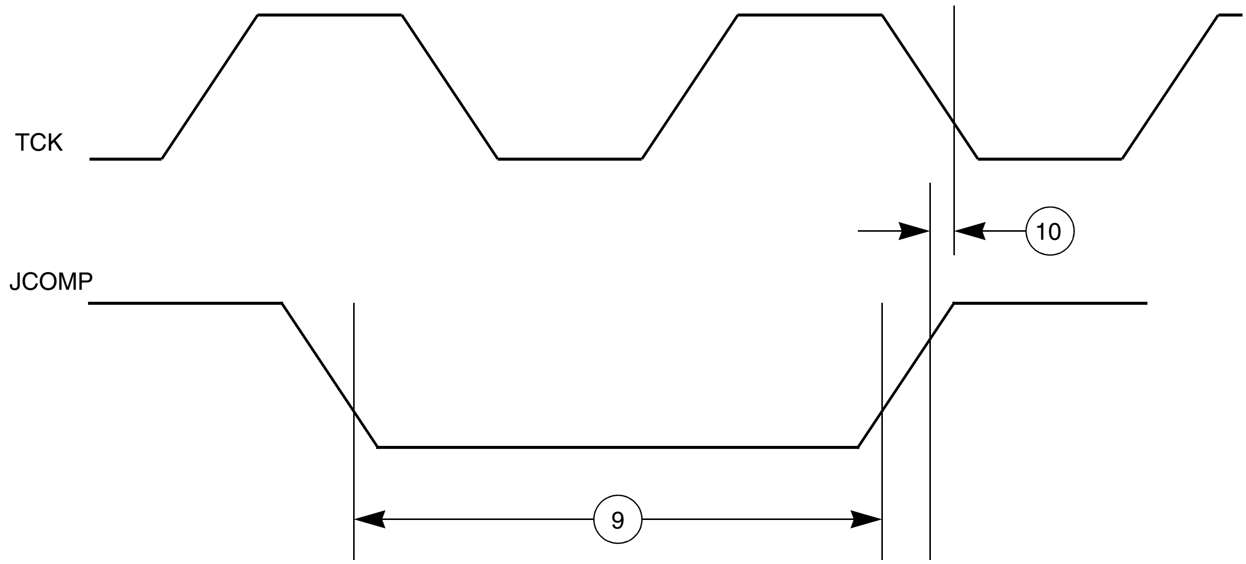


Figure 8. JTAG JCOMP Timing

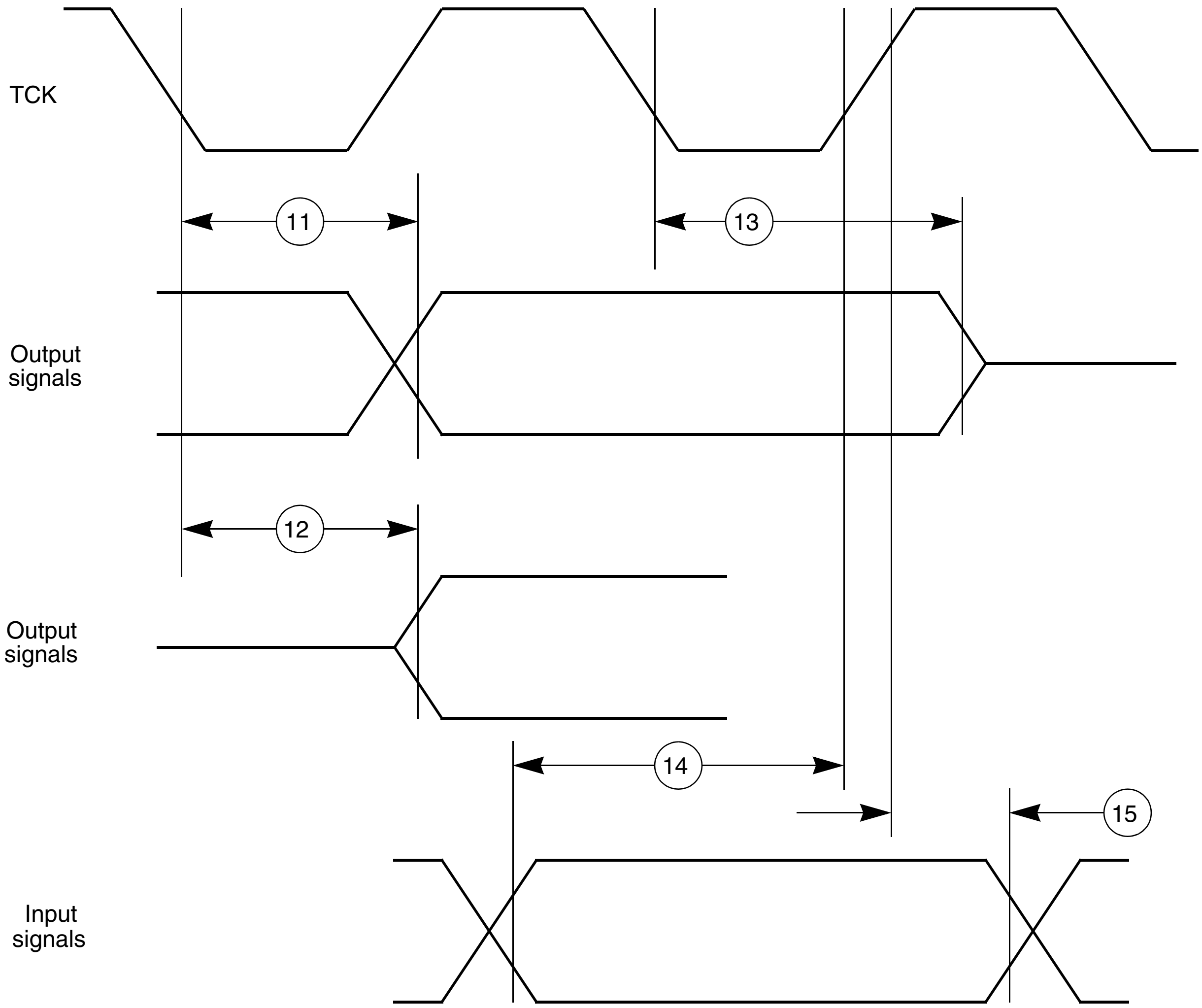


Figure 9. JTAG Boundary Scan Timing

3.13.3 Nexus Timing

Table 21. Nexus Debug Port Timing [1]

Spec	Characteristic	Symbol	Min.	Max.	Unit
1	MCKO cycle time	t_{MCYC}	1 [2]	8	t_{CYC}
2	MCKO duty cycle	t_{MDC}	40	60	%
3	MCKO low to MDO data valid [3]	t_{MDOV}	–1.5	3.0	ns
4	MCKO low to $\overline{\text{MSEO}}$ data valid [3]	t_{MSEOV}	–1.5	3.0	ns
5	MCKO low to $\overline{\text{EVTO}}$ data valid [3]	t_{EVTOV}	–1.5	3.0	ns
6	$\overline{\text{EVTI}}$ pulse width	t_{EVTIPW}	4.0	—	t_{TCYC}
7	$\overline{\text{EVTO}}$ pulse width	t_{EVTOPW}	1	—	t_{MCYC}
8	TCK cycle time	t_{TCYC}	4 [4]	—	t_{CYC}
9	TCK duty cycle	t_{TDC}	40	60	%

Table 21. Nexus Debug Port Timing [1] (continued)

Spec	Characteristic	Symbol	Min.	Max.	Unit
10	TDI, TMS data setup time	t_{NTDIS}, t_{NTMSS}	8	—	ns
11	TDI, TMS data hold time	t_{NTDIH}, t_{NTMSH}	5	—	ns
12	TCK low to TDO data valid	t_{JOV}			
	V_{DDE} = 2.25–3.0 V		0	12	ns
	V_{DDE} = 3.0–3.6 V		0	10	ns
13	$\overline{RDY}$ valid to MCKO [5]	—	—	—	—

1 JTAG specifications apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at V_{DD} = 1.35–1.65 V, V_{DDE} = 2.25–3.6 V, V_{DD33} and V_{DDSYN} = 3.0–3.6 V, $T_A = T_L$ to T_H, and CL = 30 pF with DSC = 0b10.

2 The Nexus AUX port runs up to 82 MHz. Set NPC_PCR[MCKO_DIV] to divide-by-two if the system frequency is greater than 82 MHz.

3 MDO, $\overline{MSEO}$, and $\overline{EVTO}$ data is held valid until the next MCKO low cycle occurs.

4 Limit the maximum frequency to approximately 16 MHz (V_{DDE} = 2.25–3.0 V) or 20 MHz (V_{DDE} = 3.0–3.6 V) to meet the timing specification for t_{JOV} of [0.2 x t_{JCYC}] as outlined in the IEEE-ISTO 5001-2003 specification.

5 The $\overline{RDY}$ pin timing is asynchronous to MCKO and is guaranteed by design to function correctly.

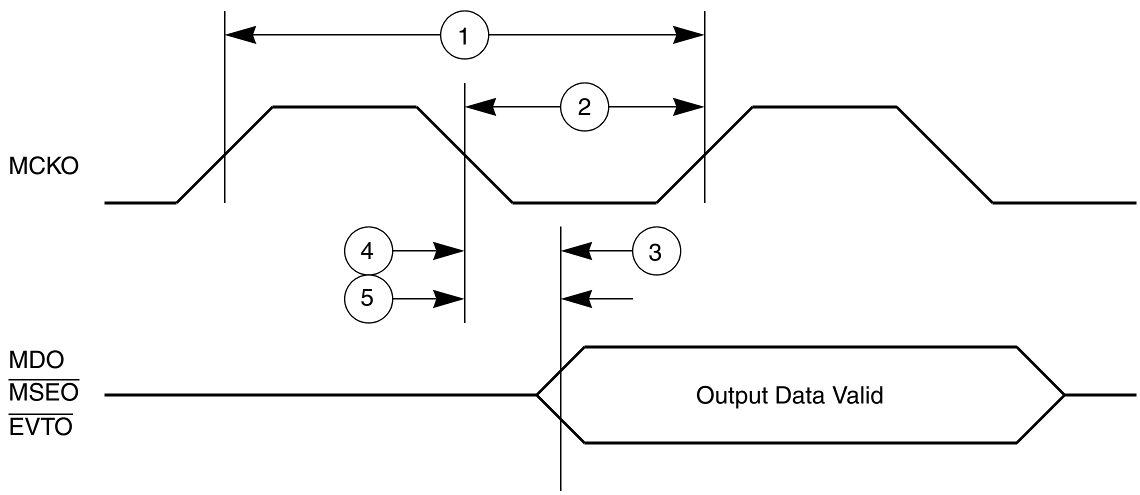


Figure 10. Nexus Output Timing

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MPC551x and MPC5533 products in 208 MAPBGA packages; MPC5534 and MPC5553 products in 208 and 496 MAPBGA packages; MPC5554, MPC5565, MPC5566 and MPC5567 products in 496 MAPBGA packages

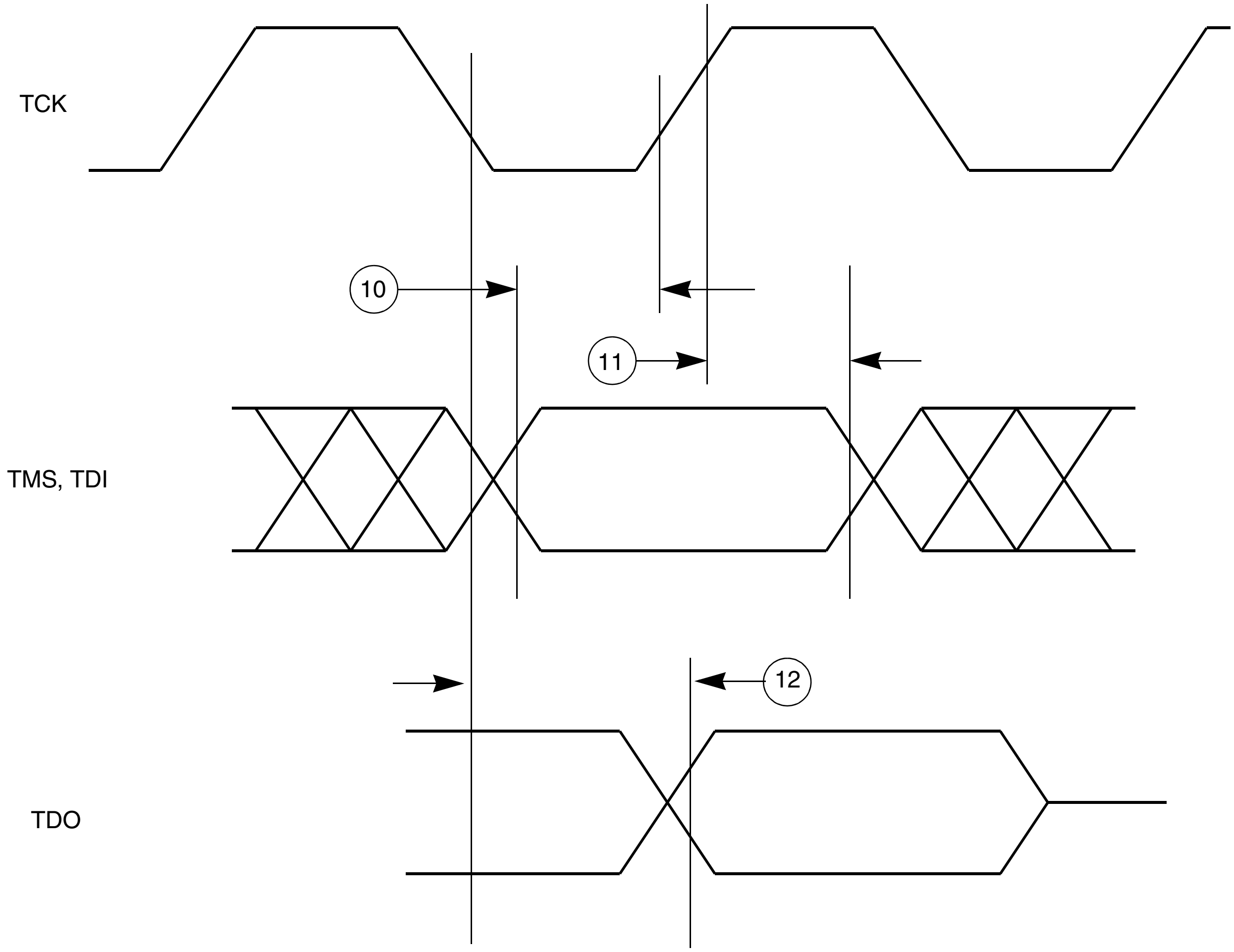


Figure 11. Nexus TDI, TMS, TDO Timing

3.13.4 External Bus Interface (EBI) Timing

Table 22 lists the timing information for the external bus interface (EBI).

Table 22. Bus Operation Timing[1]

Spec	Characteristic and Description	Symbol	External Bus Frequency [2, 3]						Unit	Notes
			40 MHz		56 MHz		66 MHz			
			Min.	Max.	Min.	Max.	Min.	Max.		
1	CLKOUT period	T_C	24.4	—	17.5	—	15.2	—	ns	Signals are measured at 50% V_{DDE}.
2	CLKOUT duty cycle	t_{CDC}	45%	55%	45%	55%	45%	55%	T_C	
3	CLKOUT rise time	t_{CRT}	—	—[4]	—	—[4]	—	—[4]	ns	
4	CLKOUT fall time	t_{CFT}	—	—[4]	—	—[4]	—	—[4]	ns	
5	CLKOUT positive edge to output signal *invalid* or Hi-Z (hold time) External bus interface $\overline{\text{CS}}$[0:3] ADDR[8:31] DATA[0:31] [5] $\overline{\text{BDIP}}$ $\overline{\text{OE}}$ RD_$\overline{\text{WR}}$ $\overline{\text{TA}}$ $\overline{\text{TEA}}$ [6] $\overline{\text{TS}}$ $\overline{\text{WE}}$/$\overline{\text{BE}}$[0:3] [7]	t_{COH}	1.0[8] 1.5	—	1.0[8] 1.5	—	1.0[8] 1.5	—	ns	EBTS = 0 EBTS = 1 Hold time selectable via SIU_ECCR [EBTS] bit.
	CLKOUT positive edge to output signal *invalid* or Hi-Z (hold time) Calibration bus interface CAL_$\overline{\text{CS}}$[0, 2:3] CAL_ADDR[10:11, 27:30] CAL_DATA[0:15] CAL_$\overline{\text{WE}}$/$\overline{\text{BE}}$[0:1]	t_{CCOH}	1.0[8] 1.5	—	1.0[8] 1.5	—	1.0[8] 1.5	—	ns	EBTS = 0 EBTS = 1 Hold time selectable via SIU_ECCR [EBTS] bit.
6	CLKOUT positive edge to output signal *valid* (output delay) External bus interface $\overline{\text{CS}}$[0:3] ADDR[8:31] DATA[0:31] [5] $\overline{\text{BDIP}}$ $\overline{\text{OE}}$ RD_$\overline{\text{WR}}$ $\overline{\text{TA}}$ $\overline{\text{TEA}}$ [6] $\overline{\text{TS}}$ $\overline{\text{WE}}$/$\overline{\text{BE}}$[0:3] [7]	t_{COV}	—	10.0[8] 11.0	—	7.5[8] 8.5	—	6.0[8] 7.0	ns	EBTS = 0 EBTS = 1 Output valid time selectable via SIU_ECCR [EBTS] bit.

Table 22. Bus Operation Timing[1] (continued)

Spec	Characteristic and Description	Symbol	External Bus Frequency [2, 3] 40 MHz Min.	40 MHz Max.	56 MHz Min.	56 MHz Max.	66 MHz Min.	66 MHz Max.	Unit	Notes
6a	CLKOUT positive edge to output signal valid (output delay) Calibration bus interface CAL_CS[0, 2:3] CAL_ADDR[10:11, 27:30] CAL_DATA[0:15] CAL_WE/BE[0:1]	t_{CCOV}	—	11.0[8] 12.0	—	8.5[8] 9.5	—	7.0[8] 8.0	ns	EBTS = 0 EBTS = 1 Output valid time selectable via SIU_ECCR [EBTS] bit.
7	Input signal *valid* to CLKOUT positive edge (setup time) External bus interface ADDR[8:31] DATA[0:31] [5] RD_WR TA TEA [6] TS	t_{CIS}	10.0	—	7.0	—	5.0	—	ns	
	Input signal valid to CLKOUT positive edge (setup time) Calibration bus interface CAL_ADDR[10:11, 27:30] CAL_DATA[0:15]	t_{CCIS}	11.0	—	8.0	—	6.0	—	ns	
8	CLKOUT positive edge to input signal *invalid* (hold time) External bus interface ADDR[8:31] DATA[0:31] [5] RD_WR TA TEA [6] TS	t_{CIH}	1.0	—	1.0	—	1.0	—	ns	
	CLKOUT positive edge to input signal *invalid* (hold time) Calibration bus interface CAL_ADDR[10:11, 27:30] CAL_DATA[0:15]	t_{CCIH}	1.0	—	1.0	—	1.0	—	ns	

1 EBI timing specified at: V_{DDE} = 1.6–3.6 V (unless stated otherwise); $T_A = T_L$ to T_H; and CL = 30 pF with DSC = 0b10.

2 Speed is the nominal maximum frequency. Max. speed is the maximum speed allowed including frequency modulation (FM). 82 MHz parts allow for 80 MHz system clock + 2% FM; 114 MHz parts allow for 112 MHz system clock + 2% FM; and 132 MHz parts allow for 128 MHz system clock + 2% FM.

3 The external bus is limited to half the speed of the internal bus.

4 Refer to fast pad timing in Table 17 and Table 18 (different values for 1.8 V and 3.3 V).

5 Due to pin limitations, the DATA[16:31] signals are not available on the 324 package.

6 Due to pin limitations, the $\overline{TEA}$ signal is not available on the 324 package.

7 Due to pin limitations, the $\overline{WE}/\overline{BE}$[2:3] signals are not available on the 324 package.

8 EBTS = 0 timings are tested and valid at V_{DDE} = 2.25–3.6 V only; EBTS = 1 timings are tested and valid at V_{DDE} = 1.6–3.6 V.

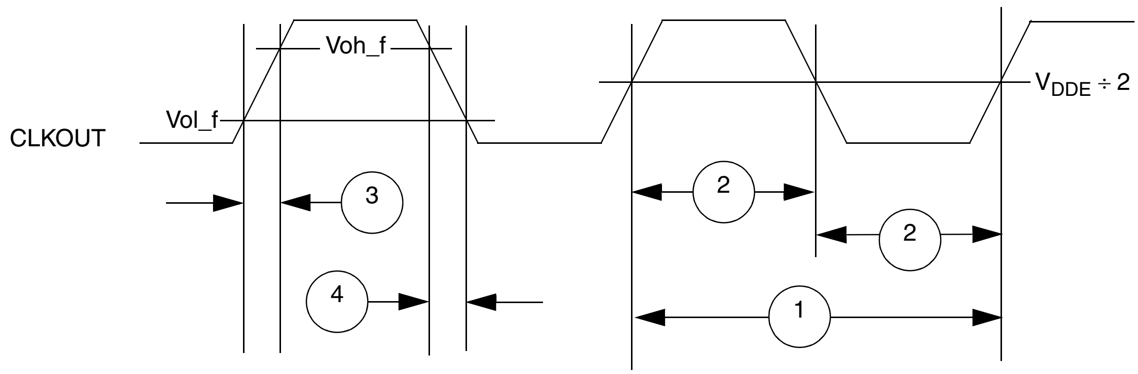


Figure 12. CLKOUT Timing

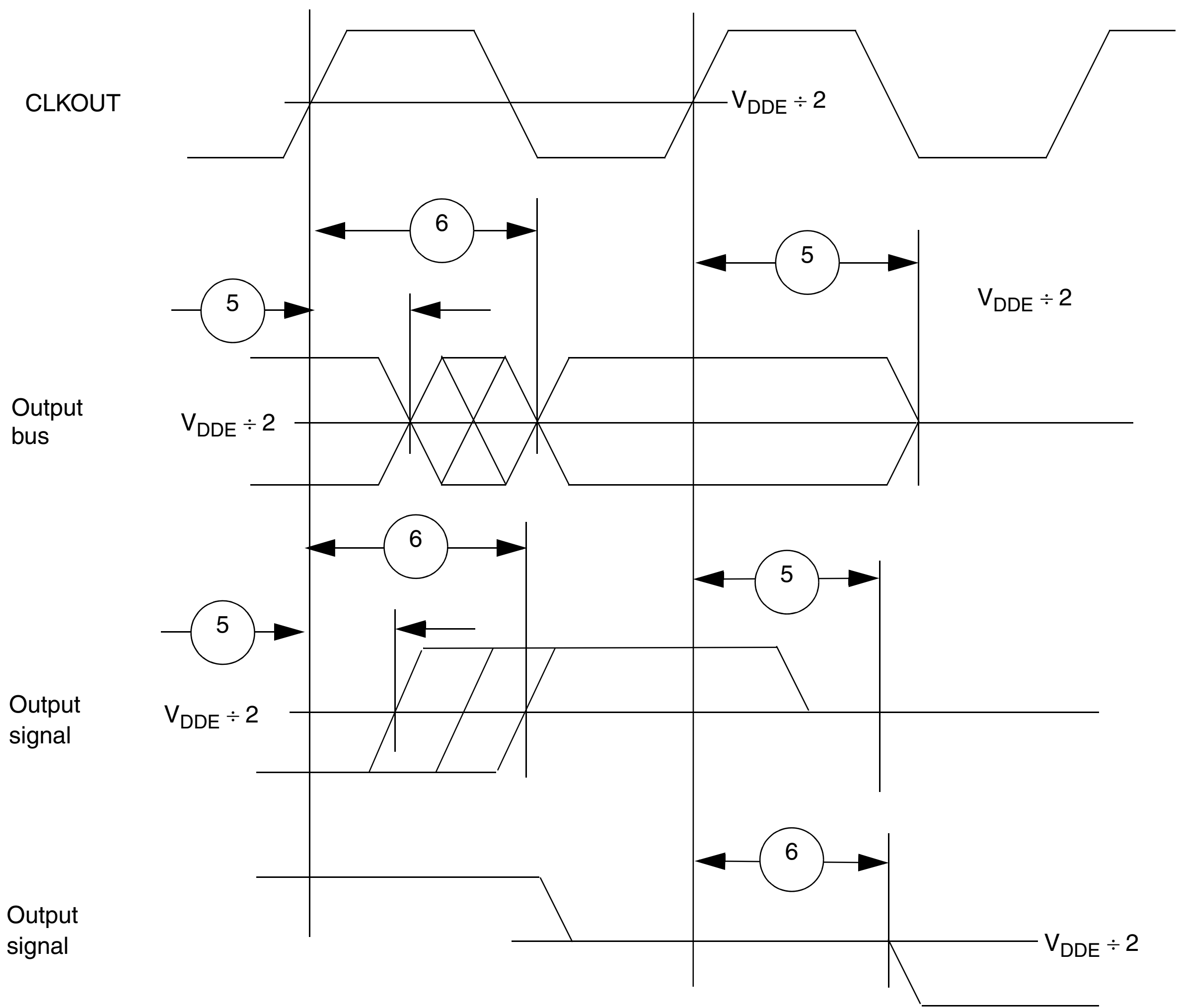


Figure 13. Synchronous Output Timing

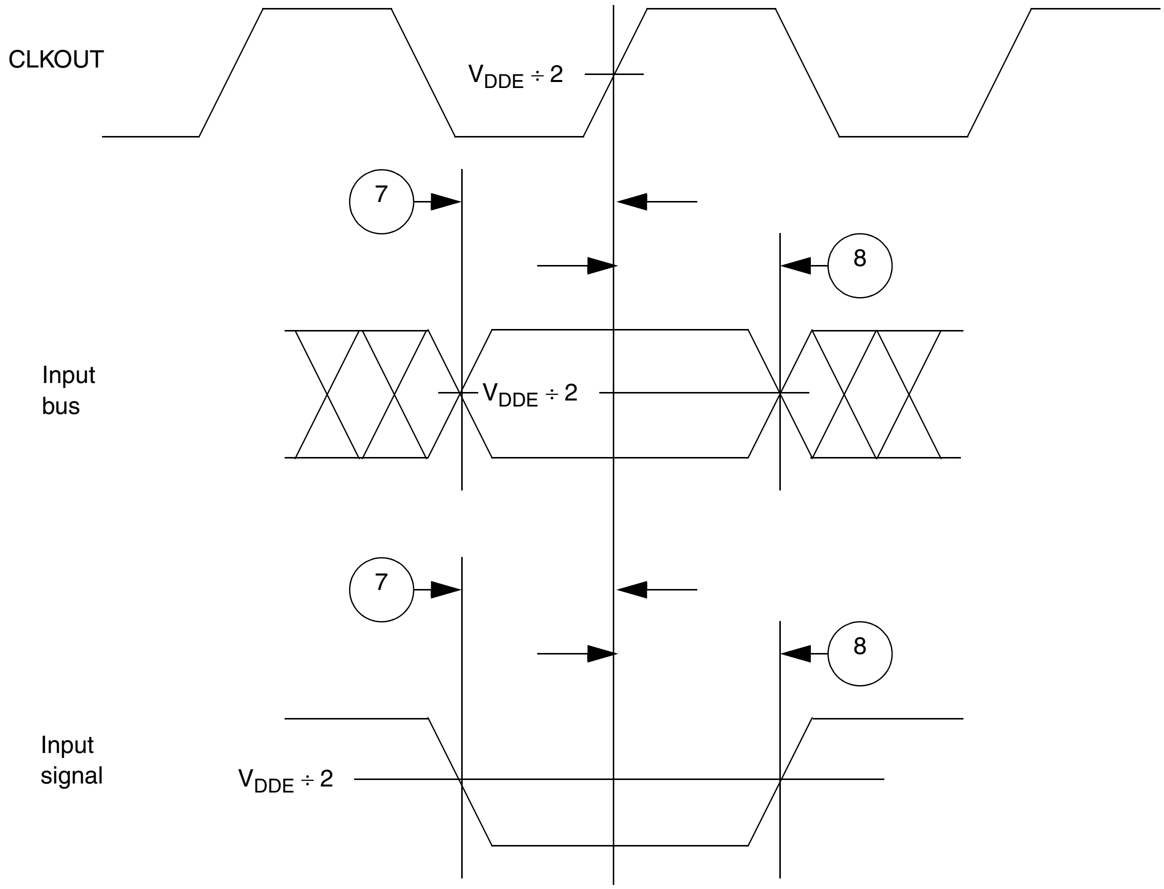


Figure 14. Synchronous Input Timing

3.13.5 External Interrupt Timing (IRQ Signals)

Table 23. External Interrupt Timing [1]

Spec	Characteristic	Symbol	Min.	Max.	Unit
1	IRQ pulse-width low	t_{IPWL}	3	—	t_{CYC}
2	IRQ pulse-width high	T_{IPWH}	3	—	t_{CYC}
3	IRQ edge-to-edge time [2]	t_{ICYC}	6	—	t_{CYC}

1 IRQ timing specified at: V_{DDEH} = 3.0–5.25 V and $T_A = T_L$ to T_H.

2 Applies when IRQ signals are configured for rising-edge or falling-edge events, but not both.

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MPC551x and MPC5533 products in 208 MAPBGA packages; MPC5534 and MPC5553 products in 208 and 496 MAPBGA packages; MPC5554, MPC5565, MPC5566 and MPC5567 products in 496 MAPBGA packages

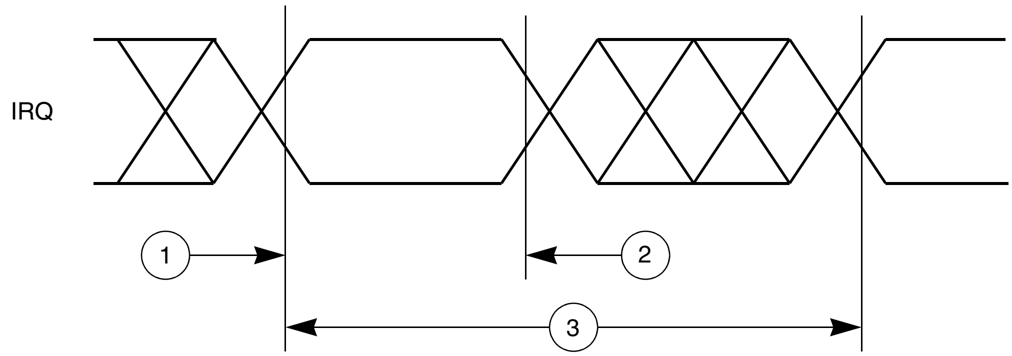


Figure 15. External Interrupt Timing

3.13.6 eTPU Timing

Table 24. eTPU Timing [1]

Spec	Characteristic	Symbol	Min.	Max	Unit
1	eTPU input channel pulse width	t_{ICPW}	4	—	t_{CYC}
2	eTPU output channel pulse width	t_{OCPW}	2 [2]	—	t_{CYC}

1 eTPU timing specified at: V_{DDEH} = 3.0–5.25 V and $T_A = T_L$ to T_H.

2 This specification does not include the rise and fall times. When calculating the minimum eTPU pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

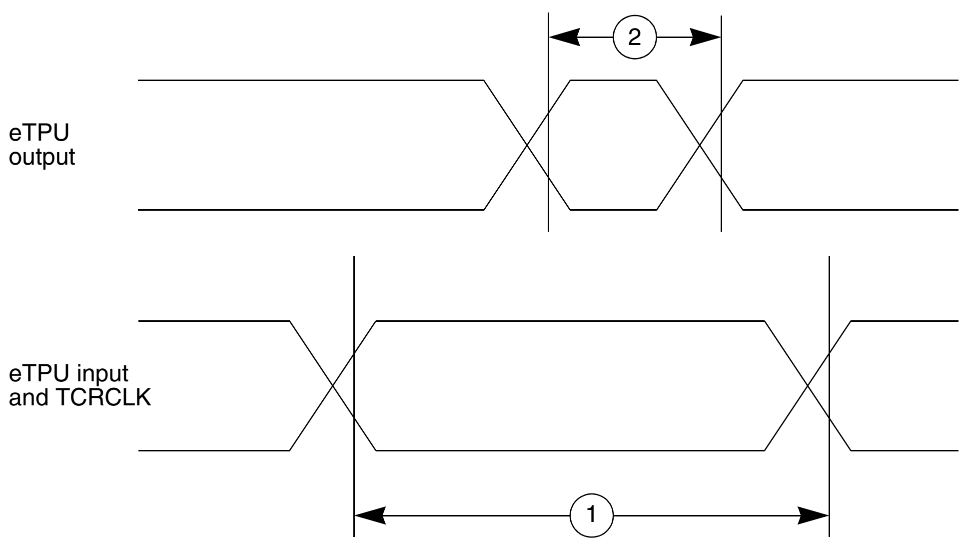


Figure 16. eTPU Timing

3.13.7 eMIOS Timing

Table 25. eMIOS Timing [1]

Spec	Characteristic	Symbol	Min.	Max.	Unit
1	eMIOS input pulse width	t_{MIPW}	4	—	t_{CYC}
2	eMIOS output pulse width	t_{MOPW}	1 [2]	—	t_{CYC}

[1] eMIOS timing specified at: V_{DDEH} = 3.0–5.25 V and $T_A = T_L$ to T_H.

[2] This specification does not include the rise and fall times. When calculating the minimum eMIOS pulse width, include the rise and fall times defined in the slew rate control field (SRC) in the pad configuration register (PCR).

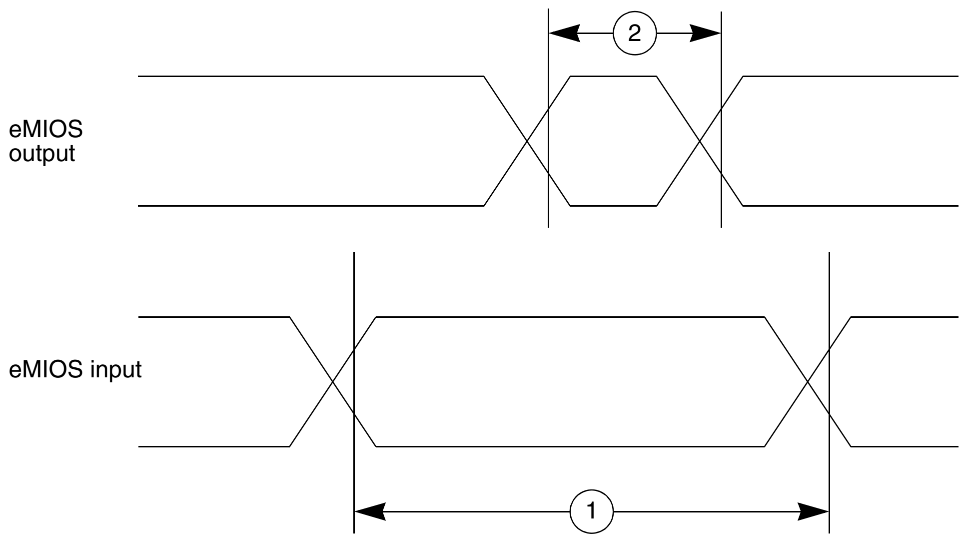


Figure 17. eMIOS Timing

3.13.8 DSPI Timing

Table 26. DSPI Timing[1, 2]

Spec	Characteristic	Symbol	80 MHz		112 MHz		132 MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
1	SCK cycle time[3, 4]	t_{SCK}	24.4 ns	2.9 ms	17.5 ns	2.1 ms	15.2 ns	1.7 ms	—
2	PCS to SCK delay[5]	t_{CSC}	23	—	15	—	13	—	ns
3	After SCK delay[6]	t_{ASC}	22	—	14	—	12	—	ns
4	SCK duty cycle	t_{SDC}	(t_{SCK} ÷ 2) – 2 ns	(t_{SCK} ÷ 2) + 2 ns	(t_{SCK} ÷ 2) – 2 ns	(t_{SCK} ÷ 2) + 2 ns	(t_{SCK} ÷ 2) – 2 ns	(t_{SCK} ÷ 2) + 2 ns	ns
5	Slave access time ($\overline{SS}$ active to SOUT driven)	t_A	—	25	—	25	—	25	ns
6	Slave SOUT disable time ($\overline{SS}$ inactive to SOUT Hi-Z, or invalid)	t_{DIS}	—	25	—	25	—	25	ns
7	PCS*x* to $\overline{PCSS}$ time	t_{PCSC}	4	—	4	—	4	—	ns
8	$\overline{PCSS}$ to PCS*x* time	t_{PASC}	5	—	5	—	5	—	ns

Table 26. DSPI Timing[1, 2] (continued)

Spec	Characteristic	Symbol	80 MHz		112 MHz		132 MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
9	Data setup time for inputs	t_{SUI}							
	Master (MTFE = 0)		20	—	20	—	20	—	ns
	Slave		2	—	2	—	2	—	ns
	Master (MTFE = 1, CPHA = 0)[7]		–4	—	3	—	6	—	ns
	Master (MTFE = 1, CPHA = 1)		20	—	20	—	20	—	ns
10	Data hold time for inputs	t_{HI}							
	Master (MTFE = 0)		–4	—	–4	—	–4	—	ns
	Slave		7	—	7	—	7	—	ns
	Master (MTFE = 1, CPHA = 0)[7]		21	—	14	—	12	—	ns
	Master (MTFE = 1, CPHA = 1)		–4	—	–4	—	–4	—	ns
11	Data valid (after SCK edge)	t_{SUO}							
	Master (MTFE = 0)		—	5	—	5	—	5	ns
	Slave		—	25	—	25	—	25	ns
	Master (MTFE = 1, CPHA = 0)		—	18	—	14	—	13	ns
	Master (MTFE = 1, CPHA = 1)		—	5	—	5	—	5	ns
12	Data hold time for outputs	t_{HO}							
	Master (MTFE = 0)		–5	—	–5	—	–5	—	ns
	Slave		5.5	—	5.5	—	5.5	—	ns
	Master (MTFE = 1, CPHA = 0)		8	—	4	—	3	—	ns
	Master (MTFE = 1, CPHA = 1)		–5	—	–5	—	–5	—	ns

1 All DSPI timing specifications use the fastest slew rate (SRC = 0b11) on pad type M or MH. DSPI signals using pad types of S or SH have an additional delay based on the slew rate. DSPI timing is specified at: V_{DDEH} = 3.0–5.5 V;$T_A = T_L$ to T_H; and CL = 50 pF with SRC = 0b11.

2 Speed is the nominal maximum frequency. Max. speed is the maximum speed allowed including frequency modulation (FM). 82 MHz parts allow for 80 MHz system clock + 2% FM; 114 MHz parts allow for 112 MHz system clock + 2% FM; and 132 MHz parts allow for 128 MHz system clock + 2% FM.

3 The minimum SCK cycle time restricts the baud rate selection for the given system clock rate. These numbers are calculated based on two MPC55xx devices communicating over a DSPI link.

4 The actual minimum SCK cycle time is limited by pad performance.

5 The maximum value is programmable in DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK].

6 The maximum value is programmable in DSPI_CTARx[PASC] and DSPI_CTARx[ASC].

7 This number is calculated using the SMPL_PT field in DSPI_MCR set to 0b10.

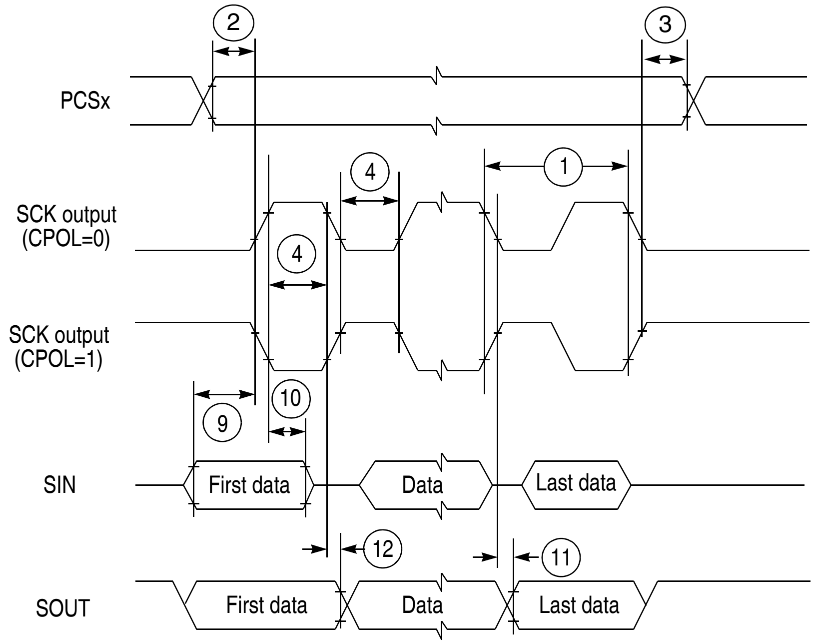


Figure 18. DSPI Classic SPI Timing—Master, CPHA = 0

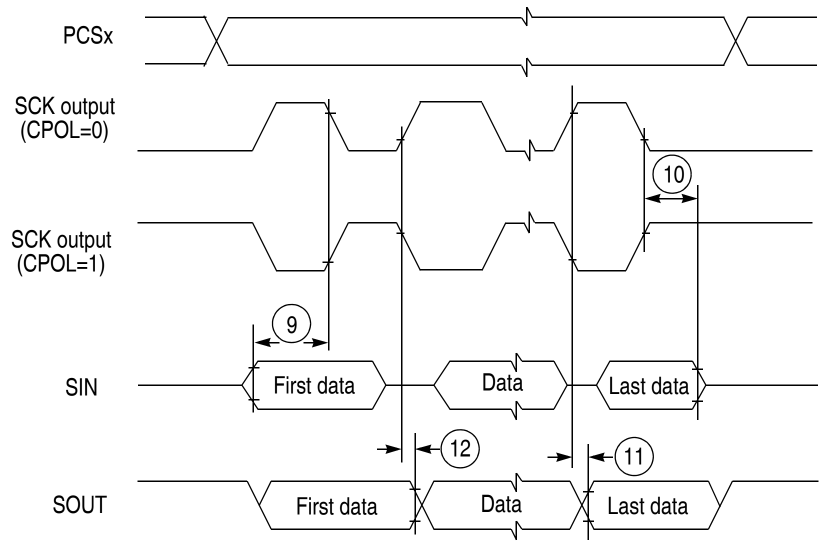


Figure 19. DSPI Classic SPI Timing—Master, CPHA = 1

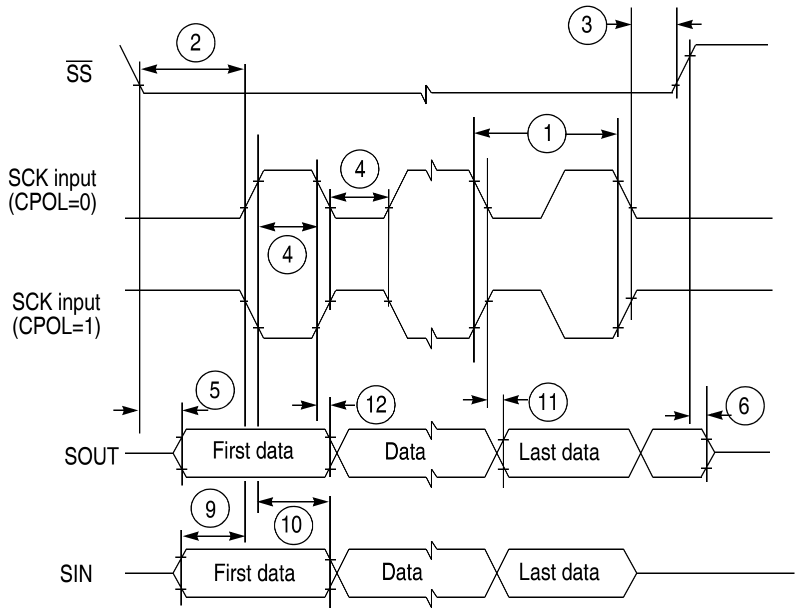


Figure 20. DSPI Classic SPI Timing—Slave, CPHA = 0

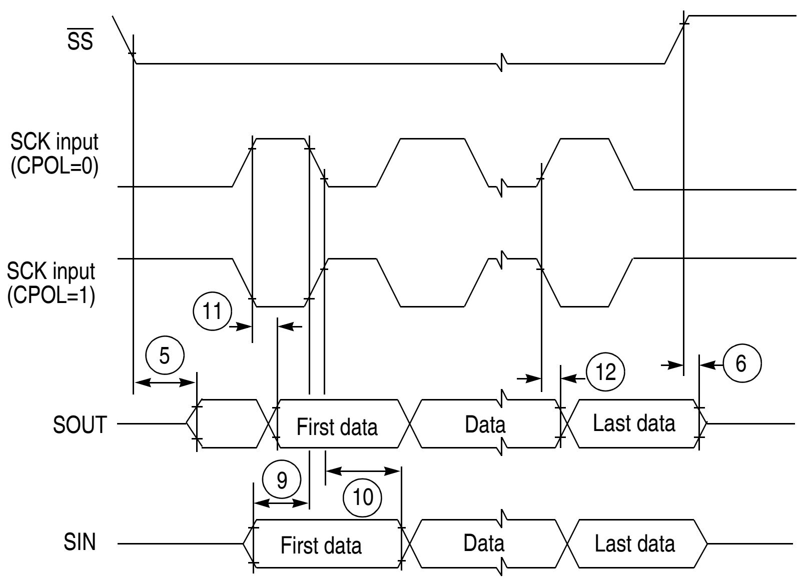


Figure 21. DSPI Classic SPI Timing—Slave, CPHA = 1

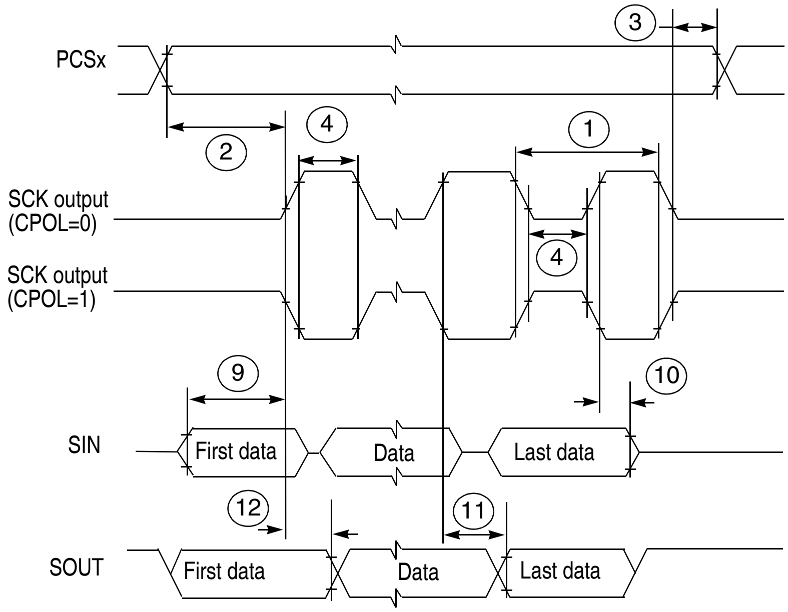


Figure 22. DSPI Modified Transfer Format Timing—Master, CPHA = 0

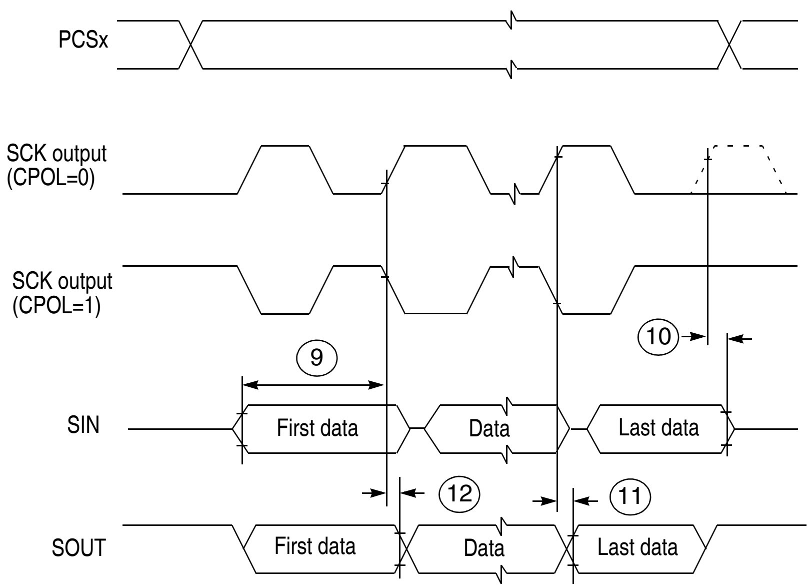


Figure 23. DSPI Modified Transfer Format Timing—Master, CPHA = 1

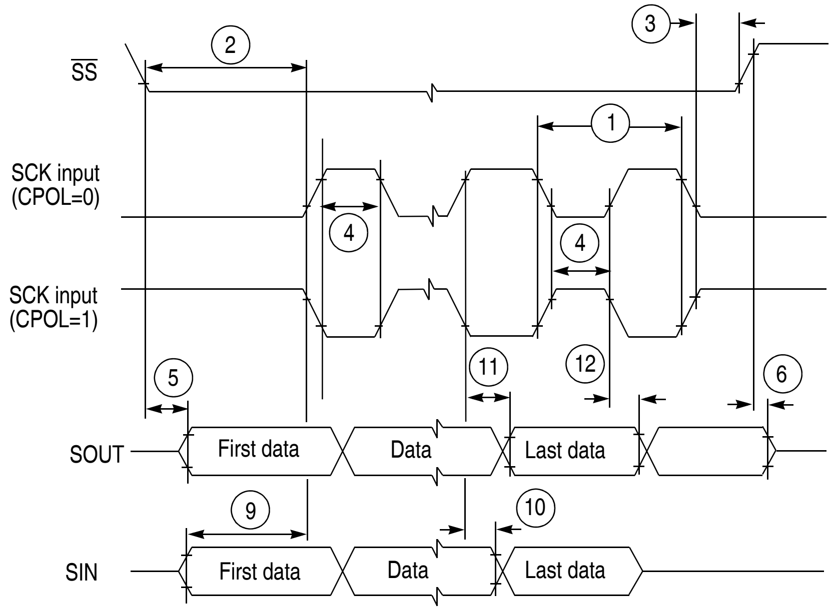


Figure 24. DSPI Modified Transfer Format Timing—Slave, CPHA = 0

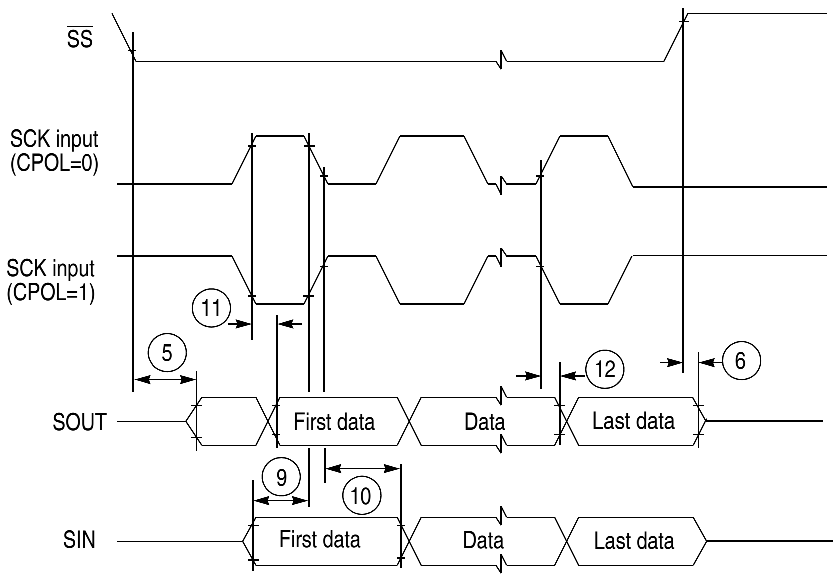


Figure 25. DSPI Modified Transfer Format Timing—Slave, CPHA = 1

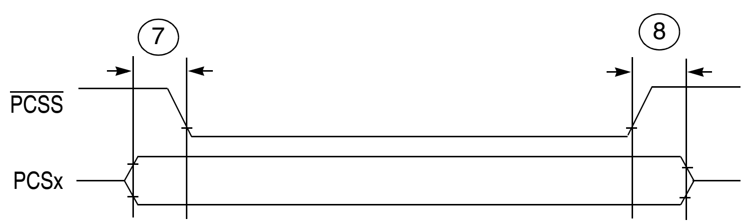


Figure 26. DSPI PCS Strobe ($\overline{PCSS}$) Timing

3.13.9 eQADC SSI Timing

Table 27. EQADC SSI Timing Characteristics

Spec	Rating	Symbol	Minimum	Typical	Maximum	Unit
2	FCK period ($t_{FCK} = 1 \div f_{FCK}$) [1, 2]	t_{FCK}	2	—	17	t_{SYS_CLK}
3	Clock (FCK) high time	t_{FCKHT}	$t_{SYS\_CLK} - 6.5$	—	$9 \times (t_{SYS\_CLK} + 6.5)$	ns
4	Clock (FCK) low time	t_{FCKLT}	$t_{SYS\_CLK} - 6.5$	—	$8 \times (t_{SYS\_CLK} + 6.5)$	ns
5	SDS lead / lag time	t_{SDS_LL}	–7.5	—	+7.5	ns
6	SDO lead / lag time	t_{SDO_LL}	–7.5	—	+7.5	ns
7	EQADC data setup time (inputs)	t_{EQ_SU}	22	—	—	ns
8	EQADC data hold time (inputs)	t_{EQ_HO}	1	—	—	ns

1 $\overline{SS}$ timing specified at $V_{DDEH} = 3.0–5.25$ V, $T_A = T_L$ to T_H, and CL = 25 pF with SRC = 0b11. Maximum operating frequency varies depending on track delays, master pad delays, and slave pad delays.

2 FCK duty cycle is not 50% when it is generated through the division of the system clock by an odd number.

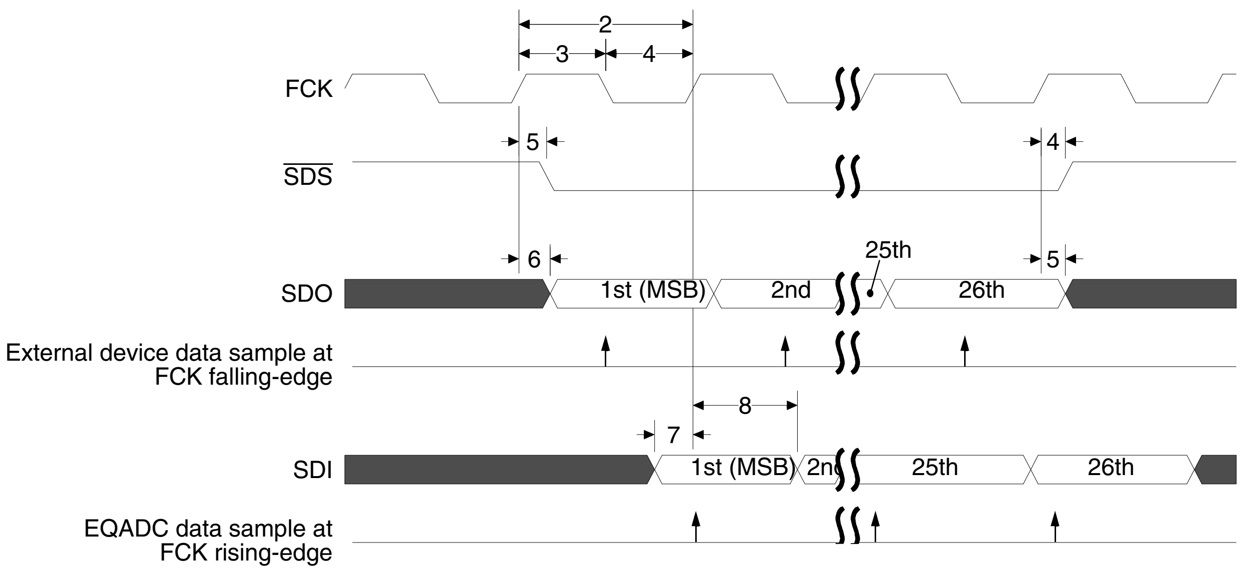


Figure 27. EQADC SSI Timing

3.14 Fast Ethernet AC Timing Specifications

Media Independent Interface (MII) Fast Ethernet Controller (FEC) signals use transistor-to-transistor logic (TTL) signal levels compatible with devices operating at 3.3 V. The timing specifications for the MII FEC signals are independent of the system clock frequency (part speed designation).

3.14.1 MII FEC Receive Signal Timing FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER, and FEC_RX_CLK

The receive functions correctly up to an FEC_RX_CLK maximum frequency of 25 MHz plus one percent. There is no minimum frequency requirement. The processor clock frequency must exceed four times the FEC_RX_CLK frequency.

Table 28 lists MII FEC receive channel timings.

Table 28. MII FEC Receive Signal Timing

Spec	Characteristic	Min.	Max	Unit
1	FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER to FEC_RX_CLK setup	5	—	ns
2	FEC_RX_CLK to FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER hold	5	—	ns
3	FEC_RX_CLK pulse-width high	35%	65%	FEC_RX_CLK period
4	FEC_RX_CLK pulse-width low	35%	65%	FEC_RX_CLK period

Figure 28 shows MII FEC receive signal timings listed in Table 28.

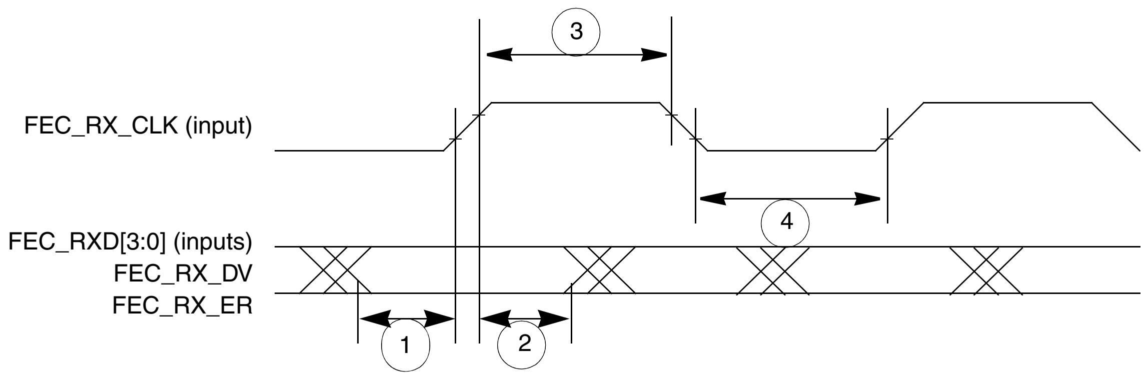


Figure 28. MII FEC Receive Signal Timing Diagram

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MPC551x and MPC5533 products in 208 MAPBGA packages; MPC5534 and MPC5553 products in 208 and 496 MAPBGA packages; MPC5554, MPC5565, MPC5566 and MPC5567 products in 496 MAPBGA packages

3.14.2 MII FEC Transmit Signal Timing FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER, FEC_TX_CLK

The transmitter functions correctly up to the FEC_TX_CLK maximum frequency of 25 MHz plus one percent. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed twice the FEC_TX_CLK frequency.

The transmit outputs (FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER) can be programmed to transition from either the rising- or falling-edge of TX_CLK, and the timing is the same in either case. These options allow the use of non-compliant MII PHYs.

Refer to the Fast Ethernet Controller (FEC) chapter of the device reference manual for details of this option and how to enable it.

Table 29 lists MII FEC transmit channel timings.

Table 29. MII FEC Transmit Signal Timing

Spec	Characteristic	Min.	Max	Unit
5	FEC_TX_CLK to FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER invalid	5	—	ns
6	FEC_TX_CLK to FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER valid	—	25	ns
7	FEC_TX_CLK pulse-width high	35%	65%	FEC_TX_CLK period
8	FEC_TX_CLK pulse-width low	35%	65%	FEC_TX_CLK period

Figure 29 shows MII FEC transmit signal timings listed in Table 29.

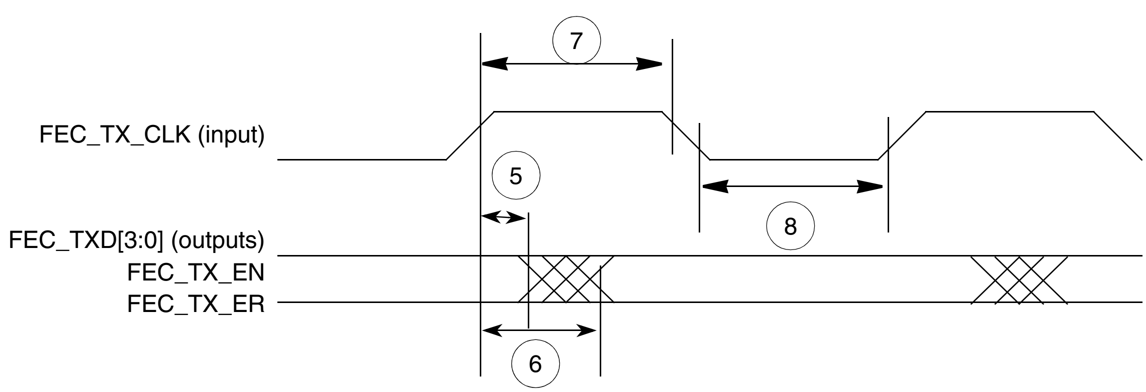


Figure 29. MII FEC Transmit Signal Timing Diagram

3.14.3 MII FEC Asynchronous Inputs Signal Timing FEC_CRS and FEC_COL

Table 30 lists MII FEC asynchronous input signal timing.

Table 30. MII FEC Asynchronous Inputs Signal Timing

Spec	Characteristic	Min.	Max	Unit
9	FEC_CRS, FEC_COL minimum pulse width	1.5	—	FEC_TX_CLK period

Figure 30 shows MII FEC asynchronous input timing listed in Table 30.

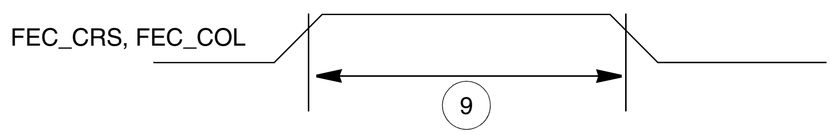


Figure 30. MII FEC Asynchronous Inputs Timing Diagram

3.14.4 MII FEC Serial Management Channel Timing FEC_MDIO and FEC_MDC

Table 31 lists MII FEC serial management channel timing. The FEC functions correctly with a maximum FEC_MDC frequency of 2.5 MHz.

Table 31. MII FEC Serial Management Channel Timing

Spec	Characteristic	Min.	Max	Unit
10	FEC_MDC falling-edge to FEC_MDIO output invalid (minimum propagation delay)	0	—	ns
11	FEC_MDC falling-edge to FEC_MDIO output valid (maximum propagation delay)	—	25	ns
12	FEC_MDIO (input) to FEC_MDC rising-edge setup	10	—	ns
13	FEC_MDIO (input) to FEC_MDC rising-edge hold	0	—	ns
14	FEC_MDC pulse-width high	40%	60%	FEC_MDC period
15	FEC_MDC pulse-width low	40%	60%	FEC_MDC period

Figure 31 shows MII FEC serial management channel timing listed in Table 31.

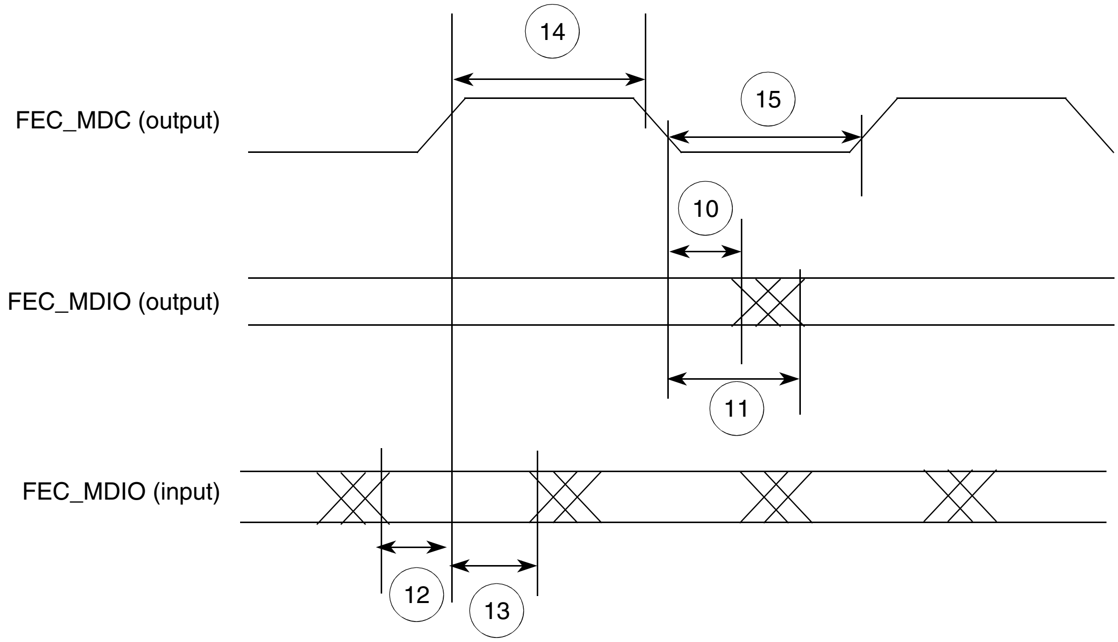


Figure 31. MII FEC Serial Management Channel Timing Diagram

4 Mechanicals

4.1 MPC5553 208 MAP BGA Pinout

Figure 32 is a pinout for the MPC5553 208 MAP BGA package.

NOTES

V_{DDEH10} and V_{DDEH6} are connected internally on the 208-ball package and are listed as V_{DDEH6}.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	VSS	AN9	AN11	VDDA1	VSSA1	AN1	AN5	VRH	VRL	AN27	VSSA0	AN12	MDO2	MDO0	VDD33	VSS
B	VDD	VSS	AN38	AN21	AN0	AN4	REF BYPC	AN22	AN25	AN28	VDDA0	AN13	MDO3	MDO1	VSS	VDD
C	VSTBY	VDD	VSS	AN17	AN34	AN16	AN3	AN7	AN23	AN32	AN33	AN14	AN15	VSS	MSEO0	TCK
D	VDD33	AN39	VDD	VSS	AN18	AN2	AN6	AN24	AN30	AN31	AN35	VDDEH 9	VSS	TMS	EVTO	TEST
E	ETPUA 30	ETPUA 31	AN37	VDD									VDDE7	TDI	EVTI	MSEO1
F	ETPUA 28	ETPUA 29	ETPUA 26	AN36									VDDEH 6	TDO	MCKO	JCOMP
G	ETPUA 24	ETPUA 27	ETPUA 25	ETPUA 21			VSS	VSS	VSS	VSS			SOUTB	PCSB3	SINB	PCSB0
H	ETPUA 23	ETPUA 22	ETPUA 17	ETPUA 18			VSS	VSS	VSS	VSS			PCSA3	PCSB4	PCSB2	PCSB1
J	ETPUA 20	ETPUA 19	ETPUA 14	ETPUA 13			VSS	VSS	VSS	VSS			PCSB5	TXDA	PCSA2	SCKB
K	ETPUA 16	ETPUA 15	ETPUA 7	VDDEH 1			VSS	VSS	VSS	VSS			CNTXC	RXDA	RSTOUT	VPP
L	ETPUA 12	ETPUA 11	ETPUA 6	TCRCLK A									TXDB	CNRXC	WKP CFG	RESET
M	ETPUA 10	ETPUA 9	ETPUA 1	ETPUA 5									RXDB	PLL CFG0	BOOT CFG1	VSS SYN
N	ETPUA 8	ETPUA 4	ETPUA 0	VSS	VDD	VDD33	EMIOS 2	EMIOS 10	VDDEH 4	EMIOS 12	EMIOS 21	VDD33	VSS	VRC CTL	PLL CFG1	EXTAL
P	ETPUA 3	ETPUA 2	VSS	VDD	GPIO 207	VDDE2	EMIOS 6	EMIOS 8	EMIOS 16	EMIOS 17	EMIOS 22	CNTXA	VDD	VSS	VRC33	XTAL
R	CS0	VSS	VDD	GPIO 206	EMIOS 4	EMIOS 3	EMIOS 9	EMIOS 11	EMIOS 14	EMIOS 19	EMIOS 23	CNRXA	CNRXB	VDD	VSS	VDD SYN
T	VSS	VDD	OE	EMIOS 0	EMIOS 1	EMIOS 5	EMIOS 7	EMIOS 13	EMIOS 15	EMIOS 18	EMIOS 20	CNTXB	VDDE5	ENG CLK	VDD	VSS

Figure 32. MPC5553 208 Package

4.2 MPC5553 324 PBGA Pinout

Figure 33 is a pinout for the MPC5553 324 PBGA package.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
A	VSS	VDD	VSTBY	AN37	AN11	VDDA1	VSSA1	AN1	AN5	VRH	VRL	AN27	AN28	AN35	VSSA0	AN12	MDO11	MDO10	MDO8	VDD	VDD33	VSS	A
B	VDD33	VSS	VDD	AN36	AN39	AN19	AN16	AN0	AN4	REF BYPC	AN23	AN26	AN31	AN32	VSSA0	AN13	MDO9	MDO7	MDO4	MDO0	VSS	VDDE7	B
C	ETPUA 30	ETPUA 31	VSS	VDD	AN8	AN17	AN20	AN21	AN3	AN7	AN22	AN25	AN30	AN33	VDDA0	AN14	MDO5	MDO2	MDO1	VSS	VDDE7	VDD	C
D	ETPUA 28	ETPUA 29	ETPUA 26	VSS	VDD	AN38	AN9	AN10	AN18	AN2	AN6	AN24	AN29	AN34	VDDEH 9	AN15	MDO6	MDO3	VSS	VDDE7	TCK	TDI	D
E	ETPUA 24	ETPUA 27	ETPUA 25	ETPUA 21															VDDE7	TMS	TDO	TEST	E
F	ETPUA 23	ETPUA 22	ETPUA 17	ETPUA 18															VDDE7	JCOMP	EVTI	EVTO	F
G	ETPUA 20	ETPUA 19	ETPUA 14	ETPUA 13															RDY	MCKO	MSEO0	MSEO1	G
H	ETPUA 16	ETPUA 15	ETPUA 10	VDDEH 1															VDDEH 10	GPIO 203	GPIO 204	SINB	H
J	ETPUA 12	ETPUA 11	ETPUA 6	ETPUA 9					VSS	VSS	VSS	VSS	VSS	VDDE7					SOUTB	PCSB3	PCSB0	PCSB1	J
K	ETPUA 8	ETPUA 7	ETPUA 2	ETPUA 5					VSS	VSS	VSS	VSS	VSS	VSS					PCSA3	PCSB4	SCKB	PCSB2	K
L	ETPUA 4	ETPUA 3	ETPUA 0	ETPUA 1					VSS	VSS	VSS	VSS	VSS	VSS					PCSB5	SOUTA	SINA	SCKA	L
M	BDIP	TCRCLK A	CS1	CS0					VDDE2	VDDE2	VSS	VSS	VSS	VSS					PCSA1	PCSA0	PCSA2	VPP	M
N	CS3	CS2	WE1	WE0					VSS	VSS	VDDE2	VSS	VSS	VSS					PCSA4	TXDA	PCSA5	VFLASH	N
P	ADDR 16	ADDR 17	RD_WR	VDD33					VSS	VSS	VDDE2	VSS	VSS	VSS					CNTXC	RXDA	RSTOUT	RST CFG	P
R	ADDR 18	ADDR 19	VDDE2	TA															WKP CFG	CNRXC	TXDB	RESET	R
T	ADDR 20	ADDR 21	ADDR 12	TS															RXDB	BOOT CFG1	VRC VSS	VSS SYN	T
U	ADDR 22	ADDR 23	ADDR 13	ADDR 14															VDDEH 6	PLL CFG1	BOOT CFG0	EXTAL	U
V	ADDR 24	ADDR 25	ADDR 15	ADDR 31															VDD	VRC CTL	PLL CFG0	XTAL	V
W	ADDR 26	VDDE2	ADDR 30	VSS	VDD	VDDE2	VDD33	VDDE2	DATA 11	DATA 12	DATA 14	EMIOS 2	EMIOS 8	VDDEH 4	EMIOS 12	EMIOS 21	VDDE5	NC	VSS	VDD	VRC33	VDD SYN	W
Y	ADDR 28	ADDR 27	VSS	VDD	VDDE2	DATA 8	DATA 9	DATA 10	GPIO 207	DATA 13	DATA 15	EMIOS 6	EMIOS 10	EMIOS 15	EMIOS 17	EMIOS 22	CNTXA	VDDE5	NC	VSS	VDD	VDD33	Y
AA	ADDR 29	VSS	VDD	VDDE2	DATA 1	VDDE2	GPIO 206	DATA 5	DATA 7	VDDE2	EMIOS 3	EMIOS 5	EMIOS 9	EMIOS 13	EMIOS 16	EMIOS 19	EMIOS 23	CNRXA	VDDE5	CLKOUT	VSS	VDD	AA
AB	VSS	VDD	VDDE2	DATA 0	DATA 2	DATA 3	DATA 4	DATA 6	OE	EMIOS 0	EMIOS 1	EMIOS 4	EMIOS 7	EMIOS 11	EMIOS 14	EMIOS 18	EMIOS 20	CNTXB	CNRXB	VDDE5	ENG CLK	VSS	AB
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	

Note: NC No connect. Reserved (W18 & Y19 are shorted to each other)

Figure 33. MPC5553 324 Package

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MPC551x and MPC5533 products in 208 MAPBGA packages; MPC5534 and MPC5553 products in 208 and 496 MAPBGA packages; MPC5554, MPC5565, MPC5566 and MPC5567 products in 496 MAPBGA packages

4.3 MPC5553 416 PBGA Pinout

Figure 34, Figure 35, and Figure 35 show the pinout for the MPC5553 416 PBGA package. While the MPC5553 and the MPC5554/MPC5565/MPC5566 are pin-compatible, the MPC5553 BGA is shown to highlight the balls that are not connected to any signal on the MPC5553 (eTPUB[0:31] and TSIZ[0:1]). The alternate Fast Ethernet Controller (FEC) signals that are multiplexed with the data bus are not shown for the MPC5553.

NOTE

Some pins have names that include functions that are not available on all MPC55*xx* devices. For example, ball R25 of the 416 BGA package is named 'SINA,' but the MPC5553 does not have a DSPI A module. In this case, the SINA pin can only be used for its alternate functions of GPIO[94] or PCSC[2]. Refer to the specific device Reference Manual for functions available on each device.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	VSS	VSTBY	AN37	AN11	VDDA1	AN16	AN1	AN5	VRH	AN23	AN27	AN28	AN35	VSSA0	AN15	ETRIG 1	NC_1	NC_2	NC_3	NC_4	GPIO 205	MDO11	MDO8	VDD	VDD33	VSS
B	VDD	VSS	AN36	AN39	AN19	AN20	AN0	AN4	REF BYPC	AN22	AN26	AN31	AN32	VSSA0	AN14	ETRIG 0	NC_5	NC_6	NC_7	NC_8	MDO10	MDO7	MDO4	MDO0	VSS	VDDE7
C	VDD33	VDD	VSS	AN8	AN17	VSSA1	AN21	AN3	AN7	VRL	AN25	AN30	AN33	VDDA0	AN13	NC_9	NC_10	NC_11	NC_12	MDO9	MDO6	MDO3	MDO1	VSS	VDDE7	VDD
D	ETPUA 30	ETPUA 31	VDD	VSS	AN38	AN9	AN10	AN18	AN2	AN6	AN24	AN29	AN34	VDDEH 9	AN12	NC_13	NC_14	NC_15	NC_16	MDO5	MDO2	VDDEH 8	VSS	VDDE7	TCK	TDI
E	ETPUA 28	ETPUA 29	VDDEH 1	VDD																			VDDE7	TMS	TDO	TEST
F	ETPUA 24	ETPUA 27	ETPUA 26	VDDEH 1																			MSEO0	JCOMP	EVTI	EVTO
G	ETPUA 23	ETPUA 22	ETPUA 25	ETPUA 21																			MSEO1	MCKO	GPIO 204	NC_17
H	ETPUA 20	ETPUA 19	ETPUA 18	ETPUA 17																			RDY	GPIO 203	NC_18	NC_19
J	ETPUA 16	ETPUA 15	ETPUA 14	ETPUA 13																			VDDEH 6	NC_20	NC_21	NC_22
K	ETPUA 12	ETPUA 11	ETPUA 10	ETPUA 9						VSS	VSS	VSS	VSS	VDDE7	VDDE7	VDDE7	VDDE7						NC_23	NC_24	NC_25	NC_26
L	ETPUA 8	ETPUA 7	ETPUA 6	ETPUA 5						VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDE7						NC_27	NC_28	NC_29	NC_30
M	ETPUA 4	ETPUA 3	ETPUA 2	ETPUA 1						VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VDDE7						NC_31	NC_32	NC_33	SINB
N	BDIP	TEA	ETPUA 0	TCRCLK A						VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VDDE7						SOUTB	PCSB3	PCSB0	PCSB1
P	CS3	CS2	CS1	CS0						VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VSS						PCSA3	PCSB4	SCKB	PCSB2
R	WE3	WE2	WE1	WE0						VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VSS						PCSB5	SOUTA	SINA	SCKA
T	VDDE2	NC_34	RD_WR	VDDE2						VDDE2	VSS	VDDE2	VDDE2	VDDE2	VDDE2	VSS	VSS						PCSA1	PCSA0	PCSA2	VPP
U	ADDR 16	NC_35	TA	VDD33						VSS	VDDE2	VDDE2	VDDE2	VDDE2	VDDE2	VSS	VSS						PCSA4	TXDA	PCSA5	VFLASH
V	ADDR 18	ADDR 17	TS	ADDR 8																			CNTXC	RXDA	RSTOUT	RST CFG
W	ADDR 20	ADDR 19	ADDR 9	ADDR 10																			RXDB	CNRXC	TXDB	RESET
Y	ADDR 22	ADDR 21	ADDR 11	VDDE2																			WKP CFG	BOOT CFG1	VRC VSS	VSS SYN
AA	ADDR 24	ADDR 23	ADDR 13	ADDR 12																			VDDEH 6	PLL CFG1	BOOT CFG0	EXTAL
AB	VDDE2	ADDR 25	ADDR 15	ADDR 14																			VDD	VRC CTL	PLL CFG0	XTAL
AC	ADDR 26	ADDR 27	ADDR 31	VSS	VDD	DATA 26	DATA 28	VDDE2	DATA 30	DATA 31	DATA 8	DATA 10	VDDE2	DATA 12	DATA 14	EMIOS 2	EMIOS 8	EMIOS 12	EMIOS 21	VDDEH 4	VDDE5	NC_36	VSS	VDD	VRC33	VDD SYN
AD	ADDR 28	ADDR 30	VSS	VDD	DATA 24	DATA 25	DATA 27	DATA 29	VDD33	GPIO 207	DATA 9	DATA 11	DATA 13	DATA 15	EMIOS 3	EMIOS 6	EMIOS 10	EMIOS 15	EMIOS 17	EMIOS 22	CNTXA	VDDE5	NC_37	VSS	VDD	VDD33
AE	ADDR 29	VSS	VDD	DATA 17	DATA 19	DATA 21	DATA 23	DATA 0	DATA 2	DATA 4	DATA 6	OE	BR	BG	EMIOS 1	EMIOS 5	EMIOS 9	EMIOS 13	EMIOS 16	EMIOS 19	EMIOS 23	CNRXA	VDDE5	CLKOUT	VSS	VDD
AF	VSS	VDD	DATA 16	DATA 18	VDDE2	DATA 20	DATA 22	GPIO 206	DATA 1	DATA 3	VDDE2	DATA 5	DATA 7	NC_38	EMIOS 0	EMIOS 4	EMIOS 7	EMIOS 11	EMIOS 14	EMIOS 18	EMIOS 20	CNTXB	CNRXB	VDDE5	ENG CLK	VSS

Note: NC_X No connects (x = 1 to 38)

NC_36 NC_37 No connect. AC22 & AD23 reserved

Figure 34. MPC5553 416 Package

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MPC551x and MPC5533 products in 208 MAPBGA packages; MPC5534 and MPC5553 products in 208 and 496 MAPBGA packages; MPC5554, MPC5565, MPC5566 and MPC5567 products in 496 MAPBGA packages

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	VSS	VSTBY	AN37	AN11	VDDA1	AN16	AN1	AN5	VRH	AN23	AN27	AN28	AN35
B	VDD	VSS	AN36	AN39	AN19	AN20	AN0	AN4	REF BYPC	AN22	AN26	AN31	AN32
C	VDD33	VDD	VSS	AN8	AN17	VSSA1	AN21	AN3	AN7	VRL	AN25	AN30	AN33
D	ETPUA 30	ETPUA 31	VDD	VSS	AN38	AN9	AN10	AN18	AN2	AN6	AN24	AN29	AN34
E	ETPUA 28	ETPUA 29	VDDEH 1	VDD									
F	ETPUA 24	ETPUA 27	ETPUA 26	VDDEH 1									
G	ETPUA 23	ETPUA 22	ETPUA 25	ETPUA 21									
H	ETPUA 20	ETPUA 19	ETPUA 18	ETPUA 17									
J	ETPUA 16	ETPUA 15	ETPUA 14	ETPUA 13									
K	ETPUA 12	ETPUA 11	ETPUA 10	ETPUA 9						VSS	VSS	VSS	VSS
L	ETPUA 8	ETPUA 7	ETPUA 6	ETPUA 5						VSS	VSS	VSS	VSS
M	ETPUA 4	ETPUA 3	ETPUA 2	ETPUA 1						VDDE2	VDDE2	VSS	VSS
N	BDIP	TEA	ETPUA 0	TCRCLK A						VDDE2	VDDE2	VSS	VSS
P	CS3	CS2	CS1	CS0						VDDE2	VDDE2	VSS	VSS
R	WE3	WE2	WE1	WE0						VDDE2	VDDE2	VSS	VSS
T	VDDE2	NC_34	RD_WR	VDDE2						VDDE2	VSS	VDDE2	VDDE2
U	ADDR 16	NC_35	TA	VDD33						VSS	VDDE2	VDDE2	VDDE2
V	ADDR 18	ADDR 17	TS	ADDR 8									
W	ADDR 20	ADDR 19	ADDR 9	ADDR 10									
Y	ADDR 22	ADDR 21	ADDR 11	VDDE2									
AA	ADDR 24	ADDR 23	ADDR 13	ADDR 12									
AB	VDDE2	ADDR 25	ADDR 15	ADDR 14									
AC	ADDR 26	ADDR 27	ADDR 31	VSS	VDD	DATA 26	DATA 28	VDDE2	DATA 30	DATA 31	DATA 8	DATA 10	VDDE2
AD	ADDR 28	ADDR 30	VSS	VDD	DATA 24	DATA 25	DATA 27	DATA 29	VDD33	GPIO 207	DATA 9	DATA 11	DATA 13
AE	ADDR 29	VSS	VDD	DATA 17	DATA 19	DATA 21	DATA 23	DATA 0	DATA 2	DATA 4	DATA 6	OE	BR
AF	VSS	VDD	DATA 16	DATA 18	VDDE2	DATA 20	DATA 22	GPIO 206	DATA 1	DATA 3	VDDE2	DATA 5	DATA 7
	1	2	3	4	5	6	7	8	9	10	11	12	13

Note: NC_X — No connects (x = 1 to 38)

NC_36 NC_37 — No connect. AC22 & AD23 reserved

Figure 35. MPC5553 416 Package Left Side (view 1 of 2)

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MPC551x and MPC5533 products in 208 MAPBGA packages; MPC5534 and MPC5553 products in 208 and 496 MAPBGA packages; MPC5554, MPC5565, MPC5566 and MPC5567 products in 496 MAPBGA packages

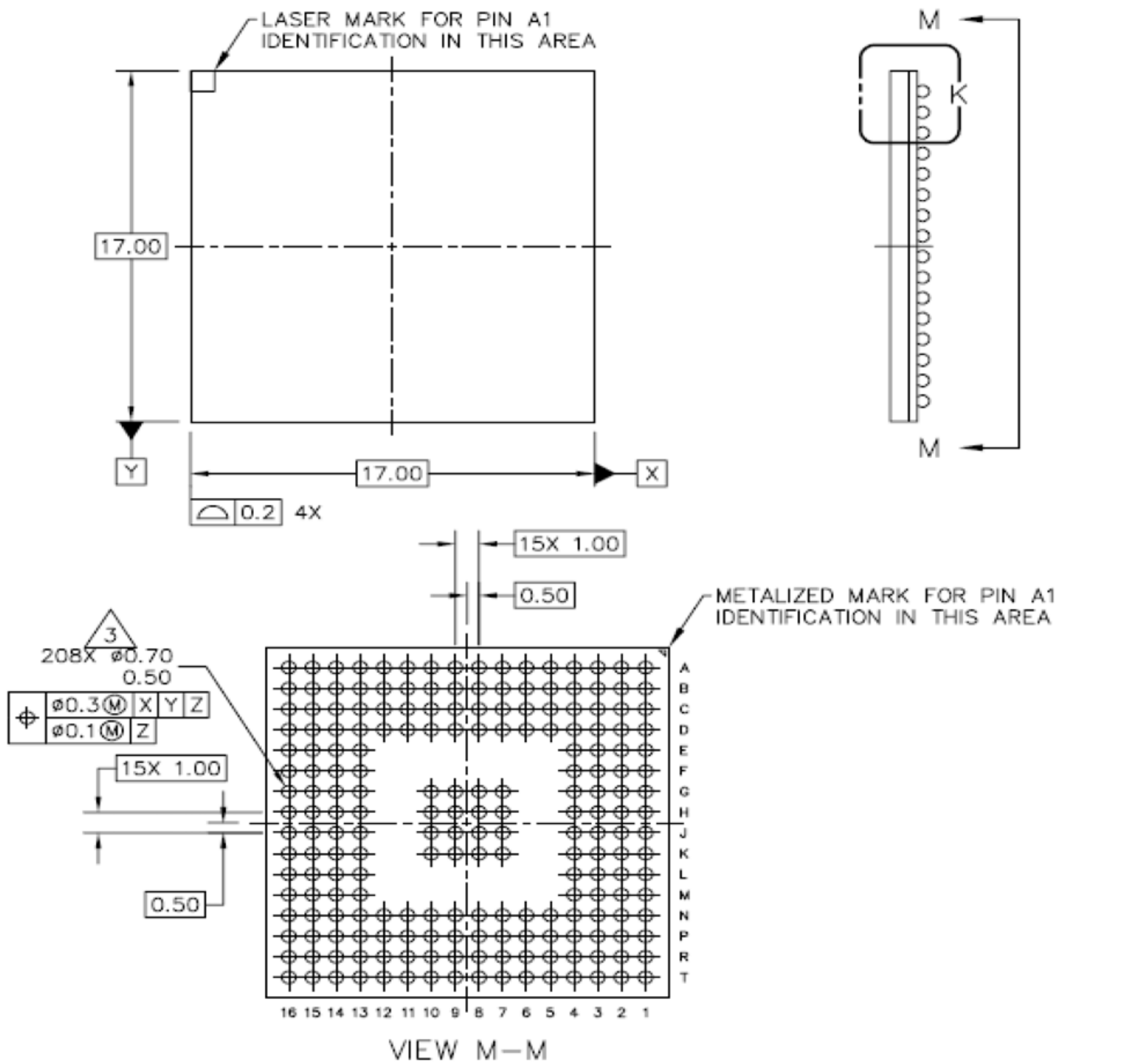
14	15	16	17	18	19	20	21	22	23	24	25	26	
VSSA0	AN15	ETRIG 1	NC_1	NC_2	NC_3	NC_4	GPIO 205	MDO11	MDO8	VDD	VDD33	VSS	A
VSSA0	AN14	ETRIG 0	NC_5	NC_6	NC_7	NC_8	MDO10	MDO7	MDO4	MDO0	VSS	VDDE7	B
VDDA0	AN13	NC_9	NC_10	NC_11	NC_12	MDO9	MDO6	MDO3	MDO1	VSS	VDDE7	VDD	C
VDDEH 9	AN12	NC_13	NC_14	NC_15	NC_16	MDO5	MDO2	VDDEH 8	VSS	VDDE7	TCK	TDI	D
									VDDE7	TMS	TDO	TEST	E
									MSEO0	JCOMP	EVTI	EVTO	F
									MSEO1	MCKO	GPIO 204	NC_17	G
									RDY	GPIO 203	NC_18	NC_19	H
									VDDEH 6	NC_20	NC_21	NC_22	J
VDDE7	VDDE7	VDDE7	VDDE7						NC_23	NC_24	NC_25	NC_26	K
VSS	VSS	VSS	VDDE7						NC_27	NC_28	NC_29	NC_30	L
VSS	VSS	VSS	VDDE7						NC_31	NC_32	NC_33	SINB	M
VSS	VSS	VSS	VDDE7						SOUTB	PCSB3	PCSB0	PCSB1	N
VSS	VSS	VSS	VSS						PCSA3	PCSB4	SCKB	PCSB2	P
VSS	VSS	VSS	VSS						PCSB5	SOUTA	SINA	SCKA	R
VDDE2	VDDE2	VSS	VSS						PCSA1	PCSA0	PCSA2	VPP	T
VDDE2	VDDE2	VSS	VSS						PCSA4	TXDA	PCSA5	VFLASH	U
									CNTXC	RXDA	RSTOUT	RST CFG	V
									RXDB	CNRXC	TXDB	RESET	W
									WKP CFG	BOOT CFG1	VRC VSS	VSS SYN	Y
									VDDEH 6	PLL CFG1	BOOT CFG0	EXTAL	AA
									VDD	VRC CTL	PLL CFG0	XTAL	AB
DATA 12	DATA 14	EMIOS 2	EMIOS 8	EMIOS 12	EMIOS 21	VDDEH 4	VDDE5	NC_36	VSS	VDD	VRC33	VDD SYN	AC
DATA 15	EMIOS 3	EMIOS 6	EMIOS 10	EMIOS 15	EMIOS 17	EMIOS 22	CNTXA	VDDE5	NC_37	VSS	VDD	VDD33	AD
BG	EMIOS 1	EMIOS 5	EMIOS 9	EMIOS 13	EMIOS 16	EMIOS 19	EMIOS 23	CNRXA	VDDE5	CLKOUT	VSS	VDD	AE
NC_38	EMIOS 0	EMIOS 4	EMIOS 7	EMIOS 11	EMIOS 14	EMIOS 18	EMIOS 20	CNTXB	CNRXB	VDDE5	ENG CLK	VSS	AF
14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 35. MPC5553 416 Package Right Side (view 2 of 2)

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MPC551x and MPC5533 products in 208 MAPBGA packages; MPC5534 and MPC5553 products in 208 and 496 MAPBGA packages; MPC5554, MPC5565, MPC5566 and MPC5567 products in 496 MAPBGA packages

4.4 MPC5553 208-Pin Package Dimensions

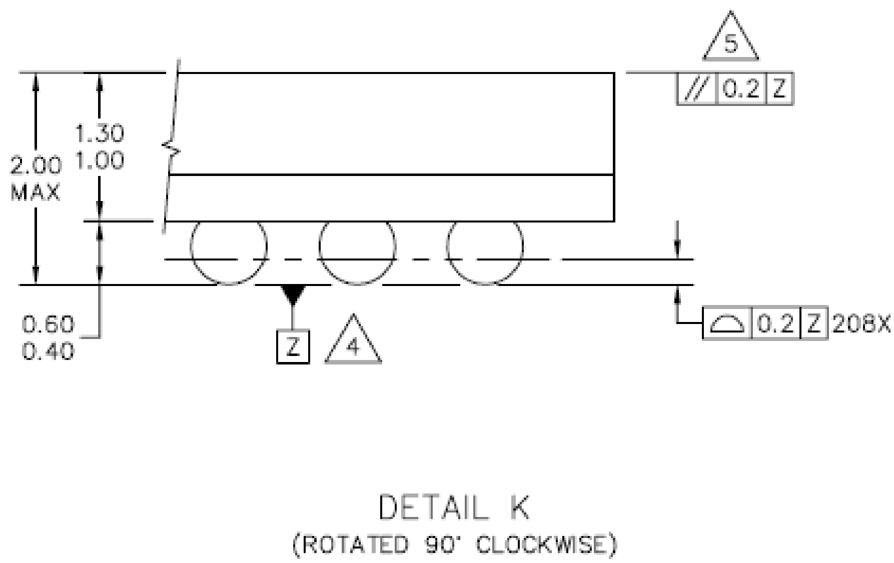
The package drawings of the MPC5553 208-pin MAP BGA are shown in Figure 36.



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: 208 I/O MAP BGA, 17 X 17 PKG, 1–MM PITCH		DOCUMENT NO: 98ARS23882W	REV: D
		CASE NUMBER: 1159A–01	02 AUG 2005
		STANDARD: JEDEC MO–151 AAF–1	

Figure 36. MPC5553 208-Pin Package

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MPC551x and MPC5533 products in 208 MAPBGA packages; MPC5534 and MPC5553 products in 208 and 496 MAPBGA packages; MPC5554, MPC5565, MPC5566 and MPC5567 products in 496 MAPBGA packages



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: 208 I/O MAP BGA, 17 X 17 PKG, 1–MM PITCH		DOCUMENT NO: 98ARS23882W	REV: D
		CASE NUMBER: 1159A–01	02 AUG 2005
		STANDARD: JEDEC MO–151 AAF–1	

Figure 36. MPC5553 208 MAP BGA Package (continued)

4.5 MPC5553 324-Pin Package Dimensions

The package drawings of the MPC5553 324-pin TEPBGA package are shown in Figure 37.

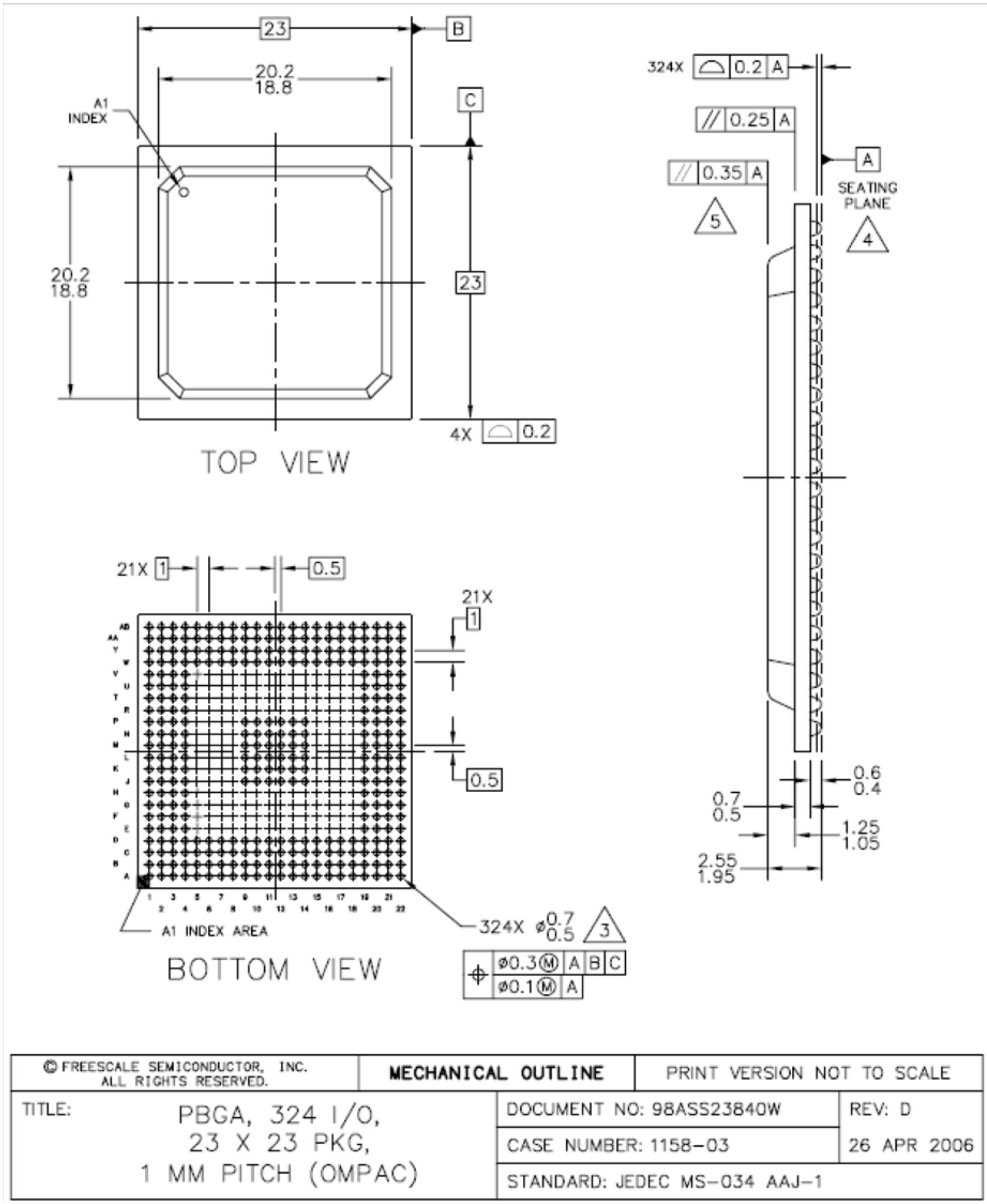


Figure 37. MPC5553 324 TEPBGA Package

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MPC551x and MPC5533 products in 208 MAPBGA packages; MPC5534 and MPC5553 products in 208 and 496 MAPBGA packages; MPC5554, MPC5565, MPC5566 and MPC5567 products in 496 MAPBGA packages

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M—1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: PBGA, 324 I/O, 23 X 23 PKG, 1 MM PITCH (OMPAC)		DOCUMENT NO: 98ASS23840W	REV: D
		CASE NUMBER: 1158—03	26 APR 2006
		STANDARD: JEDEC MS—034 AAJ—1	

Figure 37. MPC5553 324 TEPBGA Package (continued)

4.6 MPC5553 416-Pin Package Dimensions

The package drawings of the MPC5553 416 pin TEPBGA package are shown in Figure 38.

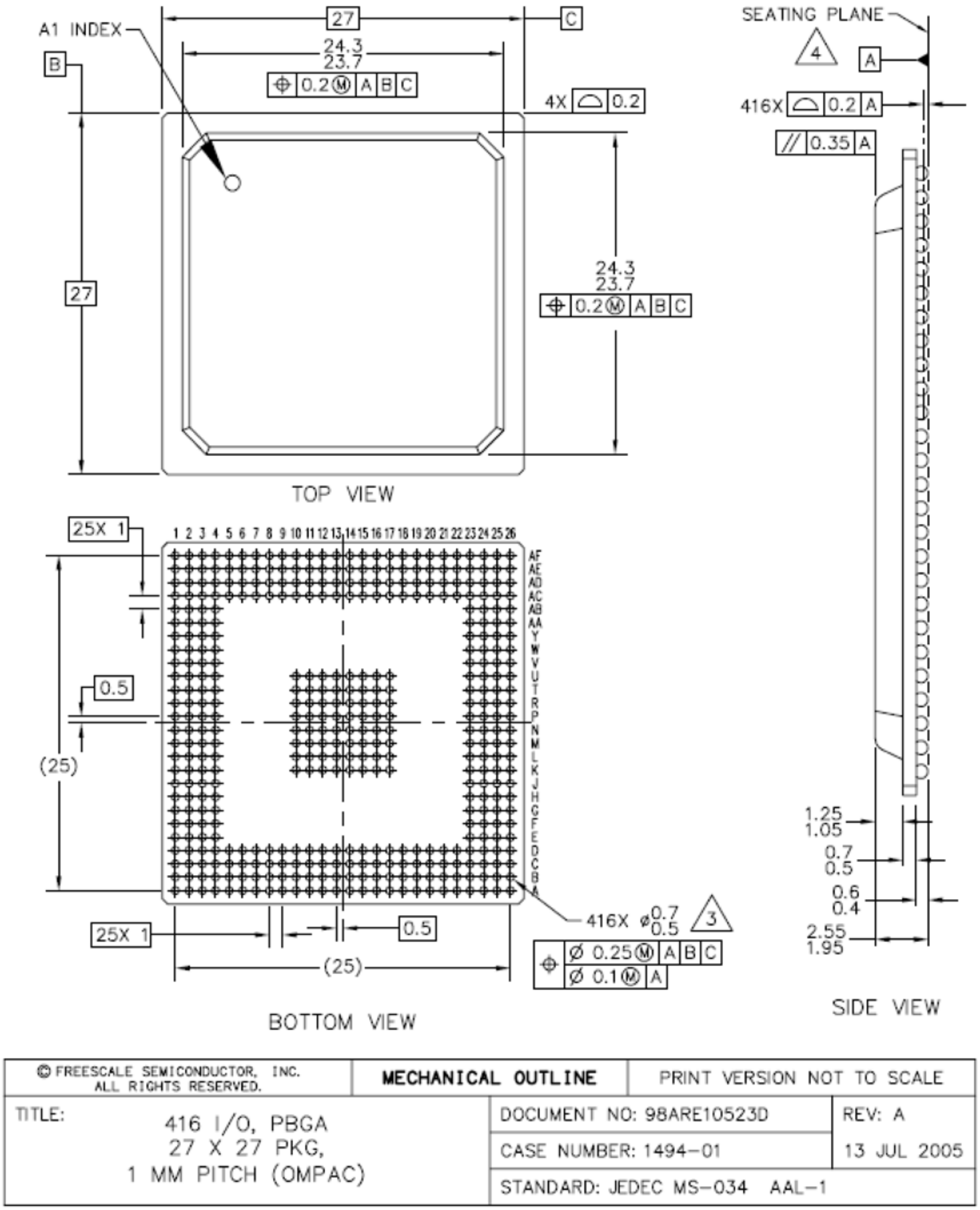


Figure 38. MPC5553 416 TEPBGA Package

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. (△) MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. (△) DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: 416 I/O, PBGA 27 X 27 PKG, 1 MM PITCH (OMPAC)	DOCUMENT NO: 98ARE10523D		REV: A
	CASE NUMBER: 1494–01		13 JUL 2005
	STANDARD: JEDEC MS–034 AAL–1		

Figure 38. MPC5553 416 TEPBGA Package (continued)

5 Revision History for the MPC5553 Data Sheet

The history of revisions made to this data sheet are described in this section. The changes are divided into each revision of this document.

The substantive changes incorporated in MPC5553 Data Sheet Rev. 2.0 to produce Rev. 3.0 are:

- Global and text changes
- Table and figure changes

Within each group, the changes are listed in sequential page number order.

5.1 Information Changed Between Revisions 2.0 and 3.0

The following table lists the global changes incorporated throughout the document, and substantive text changes made to paragraphs.

Table 32. Global and Text Changes Between Rev. 2.0 and 3.0

Location	Description of Change
Global Changes	
	Starting at the third paragraph and throughout the document, replaced: • kilobytes with KB • megabytes with MB • Changed $\overline{WE}$[0:1]/$\overline{BE}$[0:1] to $\overline{WE}$/$\overline{BE}$[0:1]. • First paragraph, text changed from “ based on the PowerPC Book E architecture” to “built on the Power Architecture embedded technology.” • Second paragraph: Changed terminology from PowerPC Book E architecture to Power Architecture terminology. • Put overbars on the following signals: $\overline{BDIP}$, $\overline{OE}$, $\overline{TA}$, $\overline{TS}$, $\overline{TEA}$
Section 1, “Overview”:	
	• Added the sentence directly preceding Table 1: ‘Unless noted in this data sheet, all specifications apply from T_L to T_H.’ • First paragraph, text changed from “ based on the PowerPC Book E architecture” to “built on the Power Architecture embedded technology.” • Second paragraph: Changed terminology from PowerPC Book E architecture to Power Architecture terminology.
3.7.1, 3.7.2 and 3.7.3: Reordered sections resulting in the following order and section renumbering:	
	• Section 3.7.1, “Input Value of Pins During POR Dependent on VDD33,” then • Section 3.7.2, “Power-Up Sequence (VRC33 Grounded),” then • Section 3.7.3, “Power-Down Sequence (VRC33 Grounded).

Table 32. Global and Text Changes Between Rev. 2.0 and 3.0 (continued)

Location	Description of Change
Section 3.7.1, "Input Value of Pins During POR Dependent on VDD33," changed:	
	From: 'To avoid accidentally selecting the bypass clock because PLLCFG[0:1] and RSTCFG are not treated as ones (1s) when POR negates, V_{DD33} must not lag V_{DDSYN} and the RESET pin power (V_{DDEH6}) when powering the device by more than the V_{DD33} lag specification in Table 6. V_{DD33} individually can lag either V_{DDSYN} or the RESET power pin (V_{DDEH6}) by more than the V_{DD33} lag specification. V_{DD33} can lag one of the V_{DDSYN} or V_{DDEH6} supplies, but cannot lag both by more than the V_{DD33} lag specification. This V_{DD33} lag specification only applies during power up. V_{DD33} has no lead or lag requirements when powering down.' To: 'When powering the device, V_{DD33} must not lag V_{DDSYN} and the RESET power pin (V_{DDEH6}) by more than the V_{DD33} lag specification listed in Table 6. This avoids accidentally selecting the bypass clock mode because the internal versions of PLLCFG[0:1] and RSTCFG are not powered and therefore cannot read the default state when POR negates. V_{DD33} can lag V_{DDSYN} or the RESET power pin (V_{DDEH6}), but cannot lag both by more than the V_{DD33} lag specification. This V_{DD33} lag specification only applies during power up. V_{DD33} has no lead or lag requirements when powering down.'
	Added the following text directly before this section and after Table 8 *Pin Status for Medium / Slow Pads During the Power-on Sequence*: 'The values in Table 7 and Table 8 do not include the effect of the weak pull devices on the output pins during power up. Before exiting the internal POR state, the voltage on the pins goes to high-impedance until POR negates. When the internal POR negates, the functional state of the signal during reset applies and the weak pull devices (up or down) are enabled as defined in the device *Reference Manual*. If V_{DD} is too low to correctly propagate the logic signals, the weak-pull devices can pull the signals to V_{DDE} and V_{DDEH}. To avoid this condition, minimize the ramp time of the V_{DD} supply to a time period less than the time required to enable the external circuitry connected to the device outputs.'

The following table describes the changes made to information in tables and figures, and is presented in sequential page number order.

Table 33. Table and Figure Changes Between Rev. 2.0 and 3.0

Location	Description of Changes
Figure 1 MPC5500 Family Part Numbers:	
	• Removed the 2 in the tape and reel designator in both the graphic and in the Tape and Reel Status text. • Changed Qualification Status by adding ‘, general market flow’ to the M designator, and added an ‘S’ designator with the description of ‘Fully spec. qualified, automotive flow.
Table 1 Orderable Part Numbers:	
	• Moved the ‘Lead-free’ or ‘Lead’ in the Package Description column to a second line and added ‘Pb-free’ and ‘SnPb’ respectively. Changed Lead to Leaded. • Footnote 2 changed to read:’ The lowest ambient operating temperature is referenced by T_L; the highest ambient operating temperature is referenced by T_H.’ • Footnote 3 changed to read: ‘Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including frequency modulation (FM): 82 MHz parts allow for 80 MHz system clock + 2% FM; 114 MHz parts allow for 112 MHz system clock + 2% FM; and 132 MHz parts allow for 128 MHz system clock + 2% FM;.’
Table 2 Absolute Maximum Ratings:	
	• Deleted Spec 3, “Flash core voltage.” • Spec 21, Added the name of the spec, ‘*V_{RC33} to V_{DDSYN} differential voltage,’* as well as the name and cross reference to Table 9, *DC Electrical Specification*s, to which the Spec was moved. • Spec 28 “Maximum Solder Temperature”: Added two lines: Lead-free (Pb-free) and Leaded (SnPb) with maximum values of 260 C and 245 C respectively. • Footnote 1, added: ‘any of’ between ‘beyond’ and ‘the listed maxima.’ • Deleted footnote 2: ‘Absolute maximum voltages are currently maximum burn-in voltages. Absolute maximum specifications for device stress have not yet been determined.’ • Footnote 6 (now footnote 5): Changed to the following sentence to the end, “Internal structures hold the input voltage greater than -1.0 V if the injection current limit of 2 mA is met. Keep the negative DC voltage greater than -0.6 V on eTPU[15] and on SINB during the internal power-on reset (POR) state.”
Table 4 EMI Testing Specifications: Changed the maximum operating frequency to from 132 to f_{MAX}.	
Table 5 ESD Characteristics: Added *(Electromagnetic Static Discharge)* in the section title.	
Table 6, VCR/POR Electrical Specifications:	

	• Subscript all symbol names that appear after the first underscore character.
	• Removed ‘Tj ‘ after ‘150 C’ in the last line, second column: Characteristic.
	• Reformatted columns.
	• Added footnote 1 to specs 1, 2, and 3 that reads: On power up, assert $\overline{RESET}$ before V_{POR15}, V_{POR33}, and V_{POR5} negate (internal POR). RESET must remain asserted until the power supplies are within the operating conditions as specified in Table 9 *DC Electrical Specifications*. On power down, assert $\overline{RESET}$ before any power supplies fall outside the operating conditions and until the internal POR asserts.
	• Added to Spec 2:
	3.3 V (V_{DDSYN}) POR negated (ramp down) Min. 0.0 Max 0.30 V
	3.3 V (V_{DDSYN}) POR asserted (ramp up) Min. 0.0 Max 0.30 V
	• Specs 7 and 10: added ‘at Tj ‘ at the end of the first line in the second column: Characteristic.
	• Spec 10:
	  • Changed the minimum values of: -40 C = 40; 25 C = 45; 150 C = 55.
	  • Added cross-reference to footnote 6: ‘I_{VRCCTL} is measured at the following conditions: V_{DD} = 1.35 V, V_{RC33} = 3.1 V, V_{VRCCTL} = 2.2 V.’ Changed ‘(@ V_{DD} = 1.35 V, f_{sys} = f_{MAX})‘ to ‘(@ f_{sys} = f_{MAX}).
	• Added a new footnote 7, ‘Refer to Table 1 for the maximum operating frequency.’
	• Rewrote old footnote 8 (new footnote 9) to read: Represents the worst-case external transistor BETA. It is measured on a per-part basis and calculated as (I_{DD} ÷ I_{VRCCTL}).
	• Deleted old footnote 9: ‘Preliminary value. Final specification pending characterization.’

Table 33. Table and Figure Changes Between Rev. 2.0 and 3.0 (continued)

Location	Description of Changes
Table 7 *Power Sequence Pin Status for Fast Pads*	
	• Changed title to *Pin Status for Fast Pads During the Power Sequence* • Changed preceding paragraph From: Although there are no power up/down sequencing requirements to prevent issues like latch-up, excessive current spikes, etc., the state of the I/O pins during power up/down varies depending on power. Prior to exiting POR, the pads are in a high impedance state (Hi-Z). To: There are no power up/down sequencing requirements to prevent issues such as latch-up, excessive current spikes, and so on. Therefore, the state of the I/O pins during power up/down varies depending on which supplies are powered.
Table 8 *Power Sequence Pin Status for Medium/Slow Pads:*	
	• Changed title to *Pin Status for Medium and Slow Pads During the Power Sequence* • Updated preceding paragraph.
Table 9 *DC Electrical Specifications*:	
	• Spelled the slash '/' as 'and' as well as 'I/O' as 'input/output.' Still very confusing. Deleted 'input/output'. • Added footnote that reads: V_{DDE2} and V_{DDE3} are limited to 2.25–3.6 V only if EBTS = 0; V_{DDE2} and V_{DDE3} have a range of 1.6–3.6 V if EBTS =1. • Spec 20, column 2, *Characteristics*,' Slow and medium output high voltage (I_{OH_S} = –2.0 mA):' Created a left-justified second line and moved 'I_{OH_S} = –2.0 mA' from the 1st line to the second line and deleted the parentheses. Created a left-justified third line that reads 'I_{OH_S} = –1.0 mA.' • Spec 20, column 4, *Min.*: Added a blank line before and after '0.80 × V_{DDEH}' and put '0.85 × V_{DDEH}' on the last line. • Spec 22, column 2, '*Slow and medium output low voltage (I_{OL_S} = 2.0 mA)*:' Created a left-justified second line and moved 'I_{OL_S} = 2.0 mA.' from the 1st line to the second line and deleted the parentheses. Created a left-justified third line that reads 'I_{OL_S} = 1.0 mA.' Column 5, *Max*: Added a blank line before and after '0.20 × V_{DDEH}' and put '0.15 × V_{DDEH}' on the last line. • Spec 26: Changed 'AN[12]_MA[1]_SDO' to 'AN[13]_MA[1]_SDO'. • Spec 27a: Operating current 1.5 V supplies @ 132 MHz changed to: 1.65 typical = 460 1.35 typical = 360 1.65 high = 510 1.35 high = 410 • Spec 27b, Operating current 1.5 V supplies @ 114 MHz changed to: 1.65 typical = 410 1.35 typical = 310 1.65 high = 460 1.35 high = 370 • Spec 27c, Operating current 1.5 V supplies @ 82 MHz changed to: 1.65 typical = 330 1.35 typical = 225 1.65 high = 385 1.35 high = 290 • Spec 28: Changed 132 MHz to f_{MAX} MHz. • Footnote 3 changed to read: If standby operation is not required, connect V_{STBY} to ground. • Footnote 6 is now: Figure 3 shows an illustration of the IDD_STBY values interpolated for these temperature values. • Deleted footnote 9: 'Preliminary. Final specification pending characterization.' • Deleted duplicate footnote: ' Absolute value of current, measured at V_{IL} and V_{IH}.

Table 33. Table and Figure Changes Between Rev. 2.0 and 3.0 (continued)

Location	Description of Changes
Table 10 I/O Pad Average DC Current: Added ($T_A = T_L – T_H$)	
Table 11 V_{DD3} Pad Average DC Current: Added ($T_A = T_L – T_H$)	
Table 12 FMPLL Electrical Characteristics:	
	• Spec 1, footnote 1 in column 2: *'PLL reference frequency range*': Added that reads 'Nominal crystal and external reference values are worst-case not more than 1%. The device operates correctly if the frequency remains within ± 5% of the specification limit. This tolerance range allows for a slight frequency drift of the crystals over time. The designer must thoroughly understand the drift margin of the source clock.' • Spec 21, column 2: Changed $f_{ref\_crystal}$ to f_{ref} in ICO frequency equation, and added the same equation but substituted f_{ref_ext} for f_{ref} for the external reference clock, giving: $f_{ico} = [f_{ref\_crystal} \times (MFD + 4)] \div (PREDIV + 1)$ $f_{ico} = [f_{ref\_ext} \times (MFD + 4)] \div (PREDIV + 1)$ • Spec 21: Changed column 5 from 'f_{SYS}' MHz' to: 'f_{MAX}'. • Spec 22: Changed column 4, *Max Value* from f_{MAX} to 20, and added footnote 17 to read, 'Maximum value for dual controller (1:1) mode is ($f_{MAX} \div 2$) and the predivider set to 1 (FMPLL_SYNCR[PREDIV] = 0b001).'
Table 13 eQADC Conversion Specifications: Added ($T_A = T_L – T_H$) to the table title.	
Table 14 Flash Program and Erase Specifications:	
	• Added ($T_A = T_L – T_H$) to the table title. • Specs 9 and 10: Changed typical values for the H7Fa Flash pre-program and erase times: -- 48 KB: from 435 to 345 -- 64 KB: from 525 to 415 • Spec 8, 128KB block pre-program and erase time: -- Typical column values from 675 to 500. -- Initial Max column from 1800 to 1250. -- Max column values from 15,000 to 7,500. • Moved footnote 1 from the table title to directly after the 'Typical' in the column 5 header. • Footnote 2: Changed from: 'Initial factory condition: ≤ 100 program/erase cycles, 25 ^{o}C, typical supply voltage, 80 MHz minimum system frequency.'To: 'Initial factory condition: ≤ 100 program/erase cycles, 25 ^{o}C, using a typical supply voltage measured at a minimum system frequency of 80 MHz.'
Table 15 Flash EEPROM Module Life:	
	• Replaced (Full Temperature Range) with ($T_A = T_L – T_H$) in the table title. • Spec 1b, Min. column value changed from 10,000 to 1,000.
Table 16 FLASH BIU Settings vs. Frequency of Operations:	
	• 'Added footnote 1 to the end of the table title, The footnote reads: 'Illegal combinations exist. Use entries from the same row in this table.' • Moved footnote 2:' For maximum flash performance, set to 0b11' to the 'DPFEN' column header. • Deleted the x-refs in the 'DPFEN' column for the rows. • Created a x-ref for footnote 2 and inserted in the 'IPFEN' column header. • Deleted the x-refs in the 'IPFEN' column for the rows. • Moved footnote 3:' For maximum flash performance, set to 0b110' to the 'PFLIM' column header. • Deleted the x-refs in the 'PFLIM' column for the rows. • Moved footnote 4:' For maximum flash performance, set to 0b1' to the 'BFEN' column header. • Deleted the x-refs in the 'BFEN' column for the rows. • Changed footnotes 1, 5, and 6 to become footnotes 5, 6, and 7 -- footnote 5 82 MHz parts allow for 80 MHz system clock + 2% frequency modulation (FM). -- footnote 6 102 MHz parts allow for 100 MHz system clock + 2% FM. -- footnote 7 132 MHz parts allow for 128 MHz system clock + 2% FM.

Table 33. Table and Figure Changes Between Rev. 2.0 and 3.0 (continued)

Location	Description of Changes
Table 17 Pad AC Specifications and *Table 18 Derated Pad AC Specifications*: The changes are identical in the tables.	
	• Table 17 Pad AC Specifications ONLY: Footnote 1, changed 'V_{DDEH} = 4.5–5.5;' to 'V_{DDEH} = 4.5–5.25;' • Footnote 1, deleted 'F_{SYS} = 132 MHz.' • Footnote 2, changed from 'tested' to '(not tested).' • Footnote 3, changed from 'Out delay' to 'The output delay', • Changed from 'Add a maximum of one system clock to the output delay to get the output delay with respect to the system clock' to 'To calculate the output delay with respect to the system clock, add a maximum of one system clock to the output delay.' • Footnote 4: changed 'Delay' to 'The output delay.' • Footnote 5: deleted 'before qualification.' Changed from 'This parameter is supplied for reference and is not guaranteed by design and not tested' to 'This parameter is supplied for reference and is guaranteed by design and tested.' • Changed from 'This parameter is supplied for reference and is not guaranteed by design and not tested' to 'This parameter is supplied for reference and is guaranteed by design and tested.'
Table 19 Reset and Configuration Pin Timing: Footnote 1, deleted 'F_{SYS} = 132 MHz.'	
Table 20 JTAG Pin AC Electrical Characteristics:	
	Footnote 1, deleted: ' and CL = 30 pF with DSC = 0b10, SRC = 0b11,' changed 'functional' to 'Nexus.'
Table 21 Nexus Debug Port Timing.	
	Changed Spec 12, TCK Low to TDO Data Valid: Changed 'VDDE = 3.0 to 3.6 volts' maximum value in column 4 from 9 to 10. Now reads 'V_{DDE} = 3.0–3.6 V' with a max value of 10.
Table 22 Bus Operation Timing:	
	• External Bus Frequency in the table heading: Added footnote that reads: Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including frequency modulation (FM). 82 MHz parts allow for 80 MHz system clock + 2% FM; 114 MHz parts allow for 112 MHz system clock + 2% FM, and 132 MHz parts allow for 128 MHz system clock + 2% FM. • Spec 1: Changed the values in Min. columns: 40 MHz from 25 to 24.4; 56 MHz from 17.9 to 17.5 • Specs 7 and 8: Removed from external bus interface: $\overline{BDIP}$, $\overline{OE}$, $\overline{WE}/\overline{BE}$[0:1]; removed from the calibration bus interface CAL_$\overline{CS}$[0, 2:3], CAL_$\overline{WE}/\overline{BE}$[0:1]. • Deleted duplicate footnote: The EBTS = 0 timings are tested and valid at V_{DDE} = 2.25–3.6 V only, whereas EBTS = 1 timings are tested and valid at V_{DDE} = 1.6–3.6 V. • Added a footnote each for the DATA[0:31], TEA, and $\overline{WE}/\overline{BE}$[0:3] signals in the table: Due to pin limitations, the DATA[16:31], $\overline{TEA}$, and $\overline{WE}/\overline{BE}$[2:3] signals are not available on the 324 package.
Table 23 External Interrupt Timing:	
	• Footnote 1, changed 'V_{DDEH} = 4.5–5.5;' to 'V_{DDEH} = 4.5–5.25;' • Footnote 1: Deleted 'F_{SYS} = 132 MHz.', 'V_{DD} = 1.35–1.65 V', 'V_{DD33} and V_{DDSYN} = 3.0–3.6 V.' and ' and CL = 200 pF with SRC = 0b11.' • Deleted second figure after table 'External Interrupt Setup Timing.'
Table 24 eTPU Timing	
	• Footnote 1, changed 'V_{DDEH} = 4.5–5.5;' to 'V_{DDEH} = 4.5–5.25;' • Footnote 1: Deleted 'F_{SYS} = 132 MHz.', 'V_{DD} = 1.35–1.65 V','V_{DD33} and V_{DDSYN} = 3.0–3.6' and ' and CL = 200 pF with SRC = 0b11.' • Deleted second figure, '*eTPU Input/Output Timing*' after this table. • Added Footnote 2: 'This specification does not include the rise and fall times. When calculating the minimum eTPU pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).'

Table 33. Table and Figure Changes Between Rev. 2.0 and 3.0 (continued)

Location	Description of Changes
Table 25 eMIOS Timing:	
	• Deleted (MTS) from the heading, table, and footnotes. • Footnote 1, changed 'V_{DDEH} = 4.5–5.5;' to 'V_{DDEH} = 4.5–5.25;' • Footnote 1: Deleted 'F_{SYS} = 132 MHz', 'V_{DD} = 1.35–1.65 V', 'V_{DD33} and V_{DDSYN} = 3.0–3.6 V' and ' and CL = 200 pF with SRC = 0b11.' • Added Footnote 2: 'This specification does not include the rise and fall times. When calculating the minimum eMIOS pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).'
Figure 17 Added *eMIOS Timing* figure.	
Table 26 DSPI Timing:	
	• Footnote 1, changed 'V_{DDEH} = 4.5–5.5;' to 'V_{DDEH} = 4.5–5.25;' • Table Title: Added footnote that reads: Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including frequency modulation (FM). 82 MHz parts allow for 80 MHz system clock + 2% FM; 114 MHz parts allow for 112 MHz system clock + 2% FM, and 132 MHz parts allow for 128 MHz system clock + 2% FM. • Spec 1: SCK cycle time; Changed 80 MHz = 24.4, and 112 MHz = 17.5. • Footnote 1: Changed to read: 'All DSPI timing specifications use the fastest slew rate (SRC = 0b11) on pad type M or MH. DSPI signals using pad types of S or SH have an additional delay based on the slew rate.' Deleted 'V_{DD} = 1.35–1.65 V' and 'V_{DD33} and V_{DDSYN} = 3.0–3.6 V.
Table 27 EQADC SSI Timing Characteristics:	
	• Footnote 1, changed 'V_{DDEH} = 4.5–5.5;' to 'V_{DDEH} = 4.5–5.25;' • Deleted from table title '(Pads at 3.3 V or 5.0 V)' • Deleted 1st line in table 'CLOAD = 25 pF on all outputs. Pad drive strength set to maximum.' • Spec 1: FCK frequency -- removed. • Combined footnotes 1 and 2, and moved the new footnote to Spec 2. Moved old footnote 3 that is now footnote 2 to Spec 2. • Footnote 1, deleted 'V_{DD} = 1.35–1.65 V' and 'V_{DD33} and V_{DDSYN} = 3.0–3.6V.' Changed 'CL = 50 pF' to 'CL = 25 pF.' • Footnote 2: added 'cycle' after 'duty' to read: FCK duty cycle is not 50% when . . . .
Section 3.14, "Fast Ethernet AC Timing Specifications" : Figure 28, Figure 29, Figure 30, and Figure 31.	
	Removed the 'M' in the diagram labels that refer to the specification numbers.
Figure 32 *MPC5553 208 Package*: Deleted the version number and date.	
Figure 33 *MPC5553 324 Package*: Deleted the version number and date.	
Figure 34 and Figure 35 *MPC5553 416 Package*: Deleted the version number and date.	

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Document Number: MPC5553
Rev. 3.0
3 Jun 2008

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MPC551x and MPC5533 products in 208 MAPBGA packages; MPC5534 and MPC5553 products in 208 and 496 MAPBGA packages; MPC5554, MPC5565, MPC5566 and MPC5567 products in 496 MAPBGA packages