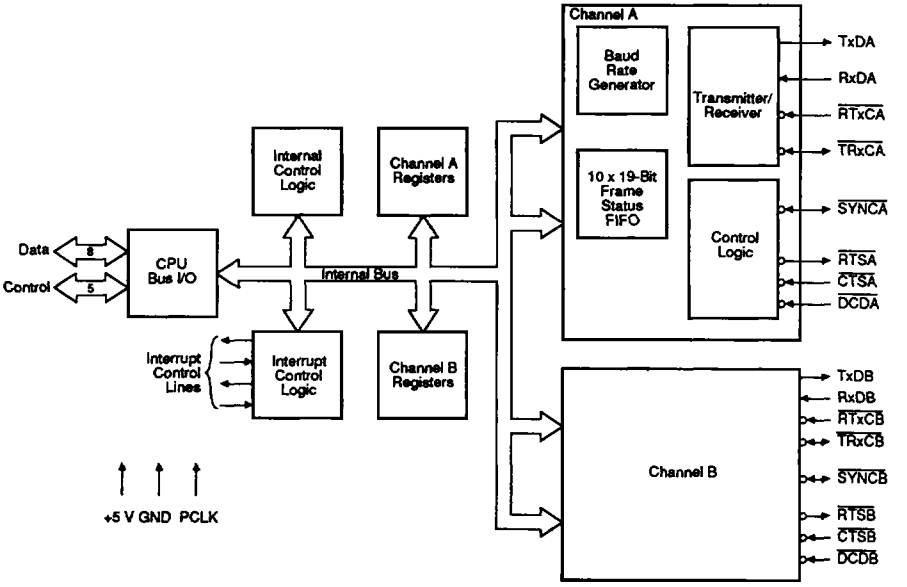
Z85C30

Enhanced Serial Communications Controller

DISTINCTIVE CHARACTERISTICS

- **Two independent full-duplex serial channels**
  Each channel has independent oscillator, baud-rate generator, and DPLL for clock recovery, dramatically reducing external components.
- **Programmable protocols**
  NRZ, NRZI, and FM data encoding/decoding supported under program control.
  - Max. Bit Rate (16 MHz)
    1) Externally clocked: 4 Mbps
    2) Self clocked:
       1 Mbps FM coding
       500 Kbps NRZI coding
- **Programmable Asynchronous Modes**
  - Programmable
    1) Stop bits
    2) Clock factor
    3) Character length (5- to 8-bit)
    4) Odd/even no parity
  - Break detection/generation
  - Error detection
    1) Framing
    2) Overrun
    3) Parity
- **Local Loopback and Auto Echo Modes**
- **Internal or external character synchronization**
- **Completely downward-compatible with the NMOS Z8530**
- **Programmable Synchronous Modes**
  SDLC/HDLC and SDLC Loop Modes supported with frame control, zero insertion and deletion, abort, and residue handling. CRC-16 and CCITT generators and checkers.
- **Compatible with non-multiplexed bus**
  The Z85C30 interfaces easily to most CPUs.
- **Enhanced SCC functions support DMA**
  - 14-bit byte counter
  - 10 x 19-bit SDLC/HDLC Frame Status FIFO
- **Low-power CMOS**

BLOCK DIAGRAM



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GENERAL DESCRIPTION

The Enhanced Serial Communications Controller (ESCC) is a dual-channel, multi-protocol data communications peripheral designed for use with 8- and 16-bit microprocessors. The ESCC functions as a serial-to-parallel, parallel-to-serial converter/controller. The ESCC can be software-configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions, including on-chip baud rate generators, digital phase-locked loops, and crystal oscillators, which dramatically reduce the need for external logic.

The ESCC handles asynchronous formats, SYNC byte-oriented protocols (such as IBM BISYNC), and SYNC bit-oriented protocols (such as HDLC and IBM SDLC). This versatile device supports virtually any serial data transfer application (cassette, diskette, tape drivers, etc.).

In addition, enhancements which allow the Z85C30 to be used more effectively in high-speed applications include:

- a 10 x 19-bit SDLC/HDLC frame status FIFO array
- a 14-bit SDLC/HDLC *frame byte counter*
- automatic SDLC/HDLC opening frame flag transmission
- TxD pin forced HIGH in SDLC NRZI mode after closing flag
- automatic SDLC/HDLC Tx underrun/EOM flag reset
- automatic SDLC/HDLC Tx CRC generator reset/preset
- $\overline{RTS}$ synchronization to closing SDLC/HDLC flag
- $\overline{DTR}/\overline{REQ}$ de-activation delay significantly reduced
- external PCLK to $\overline{RxC}$ or $\overline{TxC}$ synchronization requirement eliminated for PCLK divide-by-four operation

Other enhancements to improve the Z85C30 interface capabilities include:

- write data valid setup time to falling edge of $\overline{WR}$ requirement eliminated
- reduced $\overline{INT}$ response time
- reduced access recovery time (t_{RC}) to 3 PCLK best case (3 1/2 PCLK worst case)
- improved $\overline{Wait}$ timing
- write registers WR3, WR4, WR5, and WR10 made readable
- lower priority interrupt masking without $\overline{INTACK}$
- complete SDLC/HDLC CRC character reception

The device can generate and check CRC codes in any SYNC mode, and can be programmed to check data integrity in various modes. The ESCC also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

The ESCC is designed for non-multiplexed buses and is easily interfaced with most CPUs, such as 8080, Z80®, 6800, 68000, and MULTIBUS.†

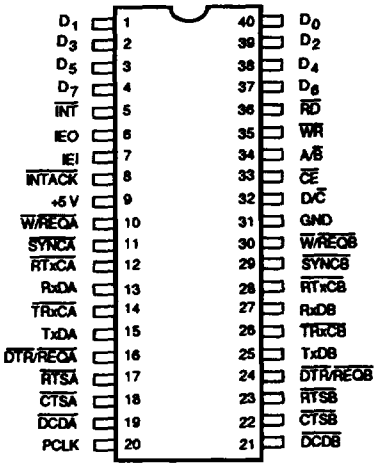
RELATED AMD PRODUCTS

Part No.	Description
Am7960	Coded Data Transceiver
80186	Highly Integrated 16-Bit Microprocessor
80286	High-Performance 16-Bit Microprocessor
Am9517A	DMA Controller

Z80 is a registerd trademark of Zilog, Inc.
†MULTIBUS is a trademark of Intel, Corp.

CONNECTION DIAGRAMS
Top View

DIPs



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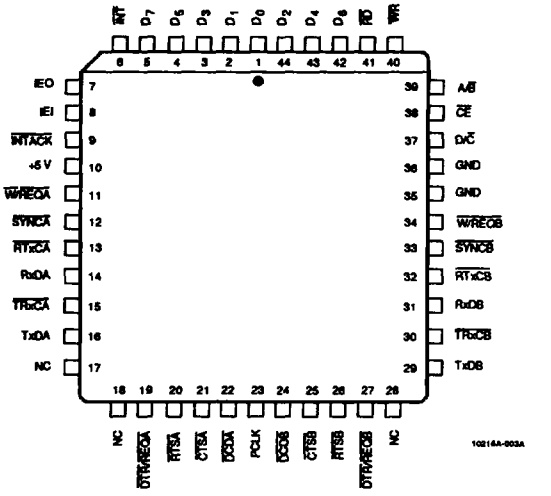
PLCC



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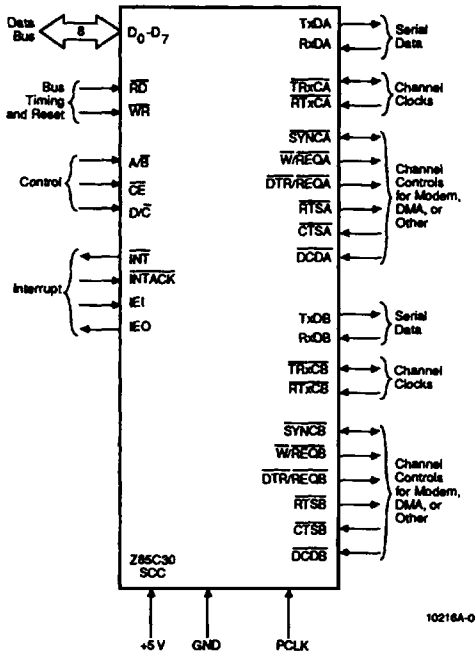
Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



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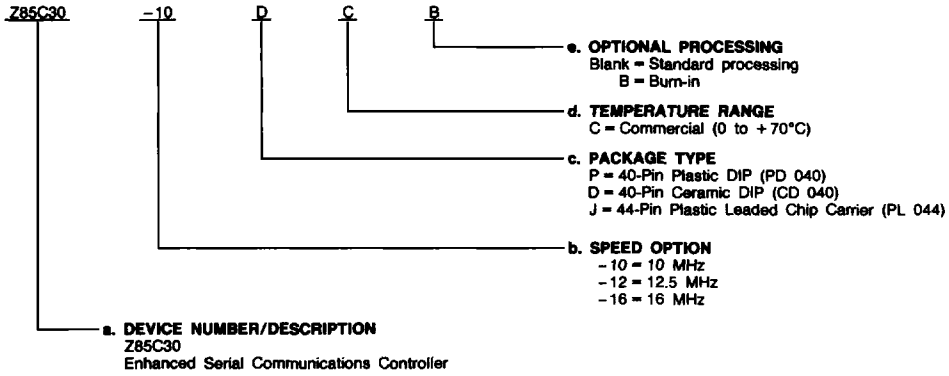
ORDERING INFORMATION

Commodity Products

AMD commodity products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
Z85C30-10	PC, DC, DCB, JC
Z85C30-12	
Z85C30-16	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.