

2SJ451

Silicon P Channel MOS FET

REJ03G0864-0400

Rev.4.00

Sep 07, 2007

Description

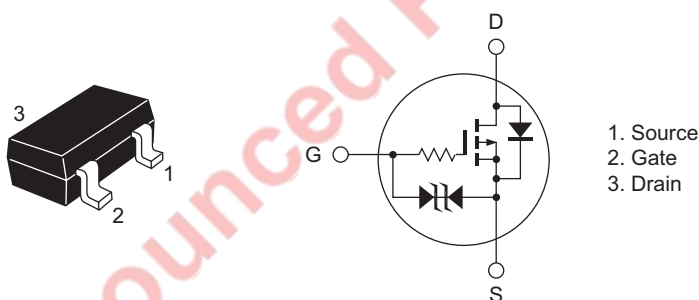
Low frequency power switching

Features

- Low on-resistance.
- Low drive power
- 2.5 V gate drive device.
- Small package (MPAK).

Outline

RENESAS Package code: PLSP0003ZB-A
(Package name: MPAK)



Note: Marking is "ZK-".

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V_{DS}	-20	V
Gate to source voltage	V_{GS}	± 20	V
Drain current	I_D	-0.2	A
Drain peak current	$I_{D(pulse)}$ ^{Note 1}	-0.4	A
Channel dissipation	P_{ch}	150	mW
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

Note: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$

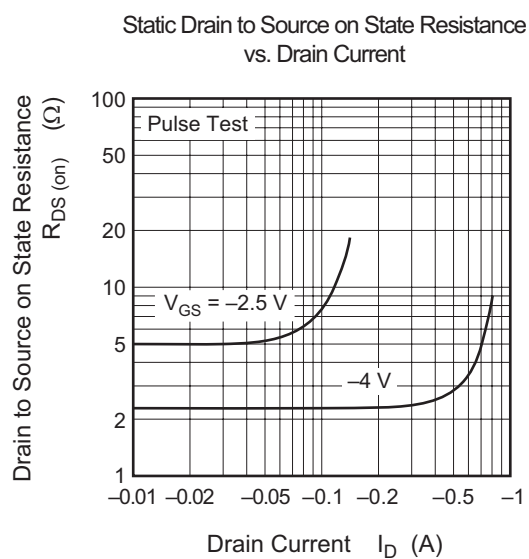
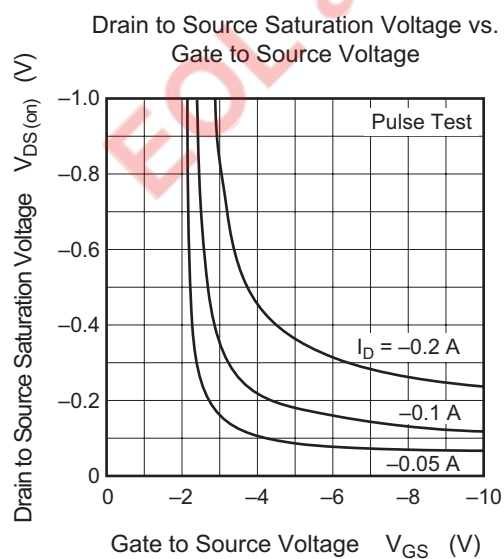
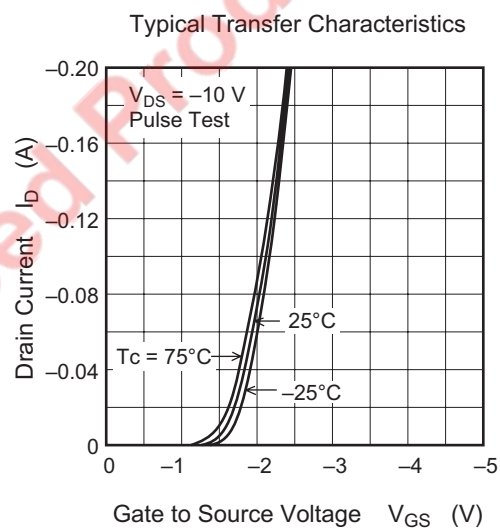
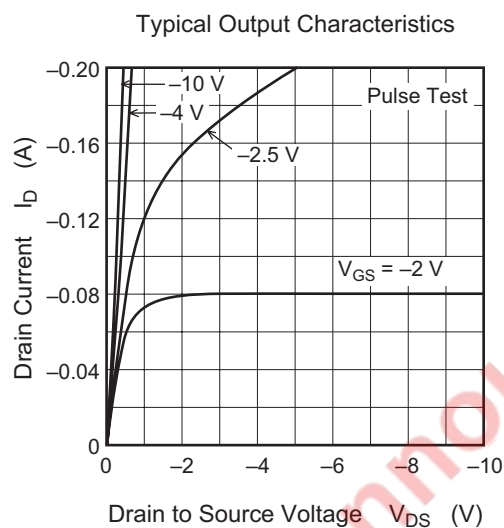
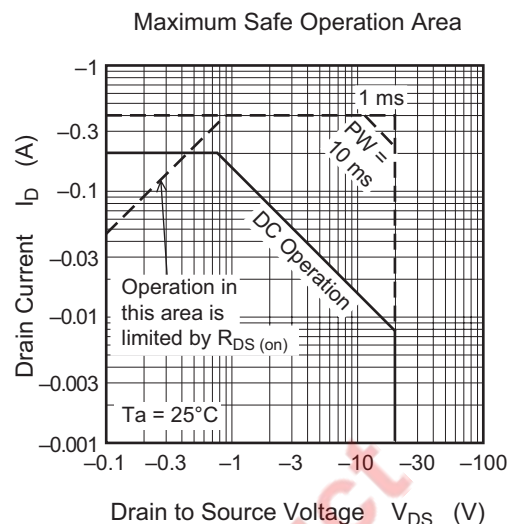
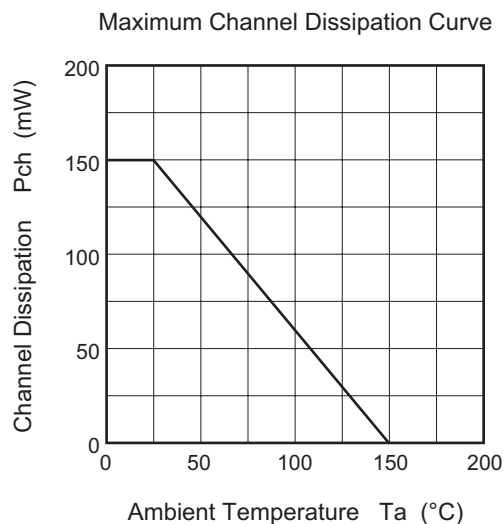
Electrical Characteristics

(Ta = 25°C)

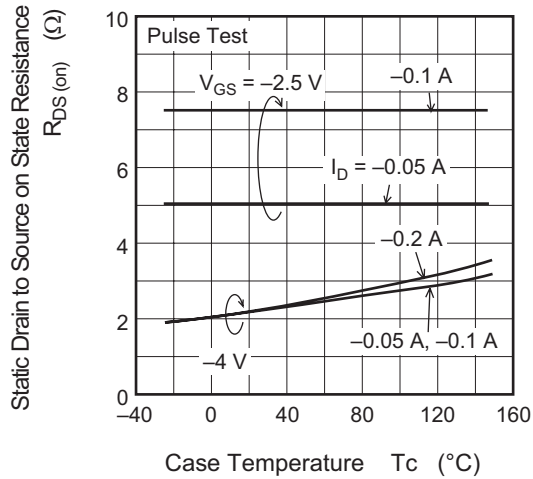
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR) DSS}$	-20	—	—	V	$I_D = -100 \mu A$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR) GSS}$	± 20	—	—	V	$I_G = \pm 100 \mu A$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-1.0	μA	$V_{DS} = -16 V$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 2.0	μA	$V_{GS} = \pm 16 V$, $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS (off)}$	-0.5	—	-1.5	V	$I_D = -10 \mu A$, $V_{DS} = -5 V$
Static drain to source on state resistance	$R_{DS (on) 1}$	—	2.3	3.5	Ω	$I_D = -100 mA$, $V_{GS} = -4 V$ ^{Note 2}
	$R_{DS (on) 2}$	—	5.0	9.0	Ω	$I_D = -40 mA$, $V_{GS} = -2.5 V$ ^{Note 2}
Forward transfer admittance	$ y_{fs} $	0.13	0.23	—	S	$I_D = -100 mA$, $V_{DS} = -10 V$ ^{Note 2}
Input capacitance	C_{iss}	—	2.4	—	pF	$V_{DS} = -10 V$ $V_{GS} = 0$ $f = 1 MHz$
Output capacitance	C_{oss}	—	31	—	pF	
Reverse transfer capacitance	C_{rss}	—	0.6	—	pF	
Turn-on delay time	$t_{d (on)}$	—	170	—	ns	$I_D = -0.1 A$ $V_{GS} = -10 V$ $R_L = 100 \Omega$
Rise time	t_r	—	680	—	ns	
Turn-off delay time	$t_{d (off)}$	—	3.0	—	μs	
Fall time	t_f	—	2.8	—	μs	

Note: 2. Pulse test

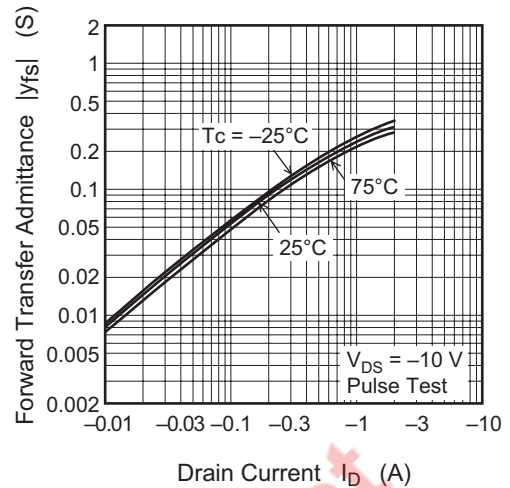
Main Characteristics



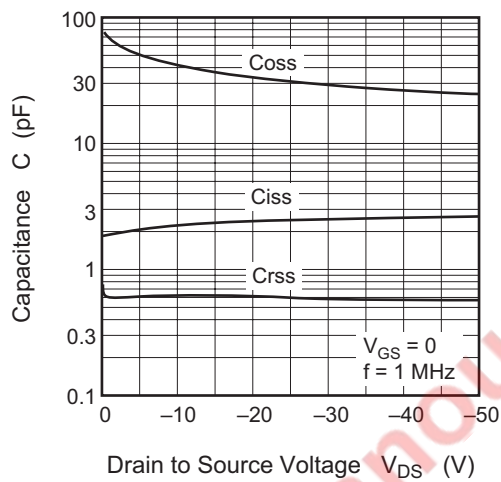
Static Drain to Source on State Resistance vs. Temperature



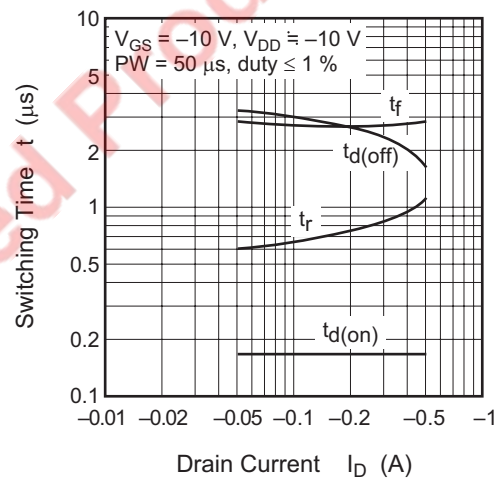
Forward Transfer Admittance vs. Drain Current



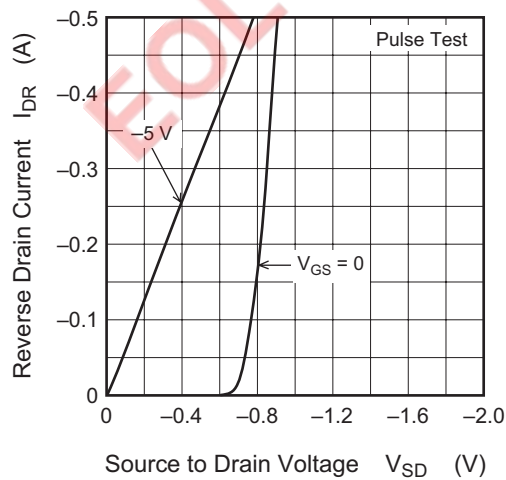
Typical Capacitance vs. Drain to Source Voltage



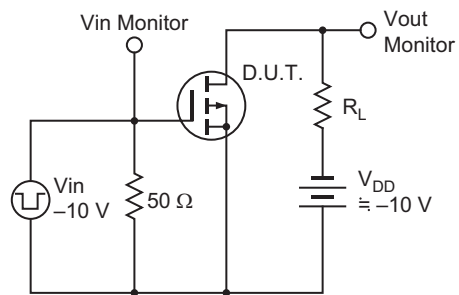
Switching Characteristics



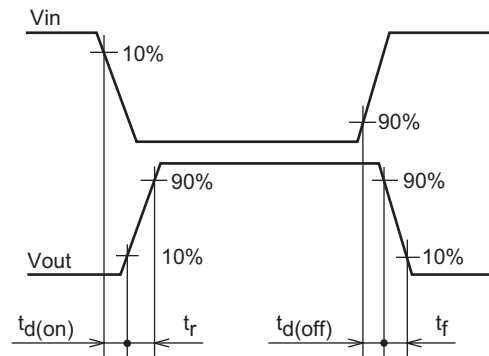
Reverse Drain Current vs. Source to Drain Voltage



Switching Time Test Circuit



Waveform



EOL announced Product

Notes:

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