

2SK2570

Silicon N Channel MOS FET Low Frequency Power Switching

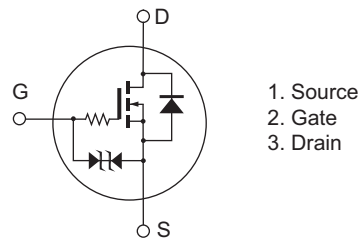
REJ03G1019-0200
(Previous: ADE-208-574)
Rev.2.00
Sep 07, 2005

Features

- Low on-resistance
 $R_{DS(on)} = 0.8 \Omega$ typ. ($V_{GS} = 4 \text{ V}$, $I_D = 100 \text{ mA}$)
- 2.5 V gate drive devices.
- Small package (MPAK)

Outline

RENESAS Package code: PLSP0003ZB-A
(Package name: MPAK)



Note: Marking is "ZL—"

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	20	V
Gate to source voltage	V_{GSS}	± 10	V
Drain current	I_D	0.2	A
Drain peak current	$I_{D(pulse)}^{*1}$	0.4	A
Channel dissipation	Pch	150	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

Note: 1. PW ≤ 10 μs, duty cycle ≤ 1 %

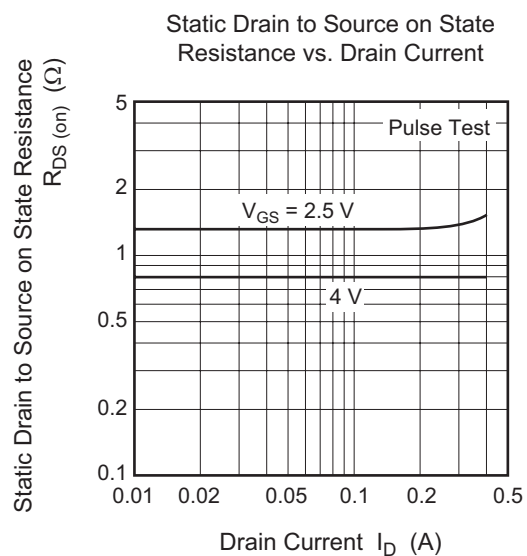
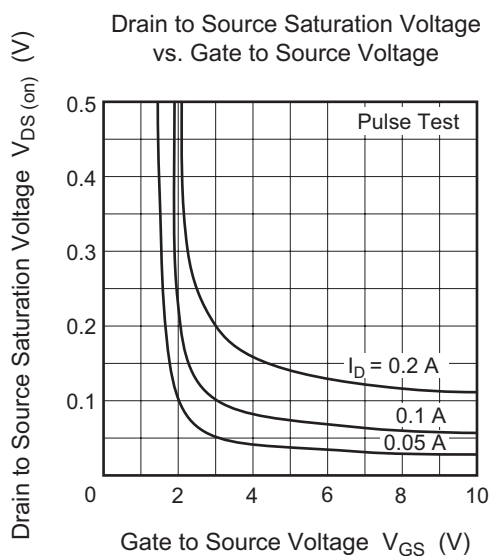
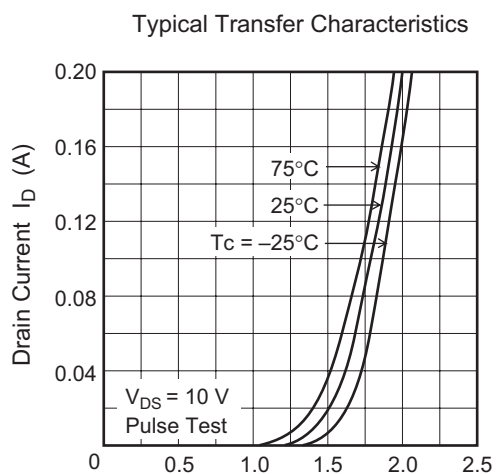
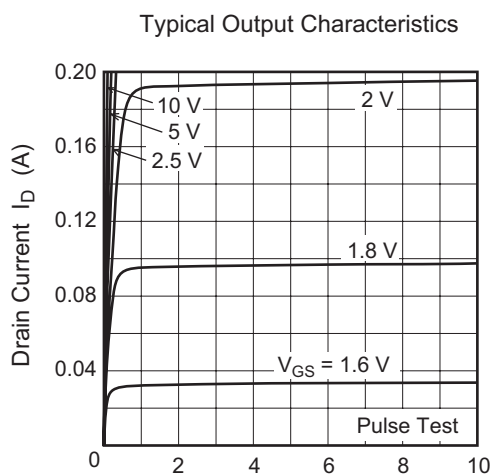
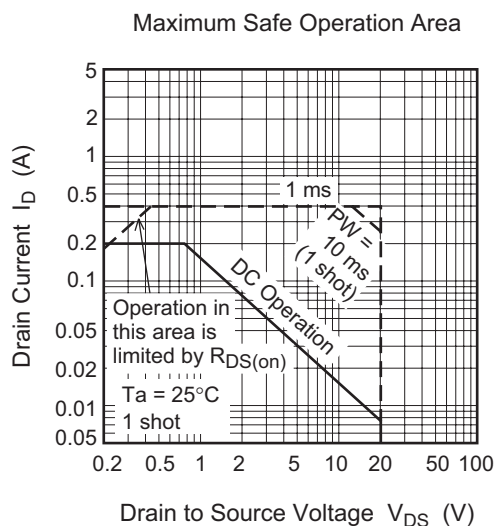
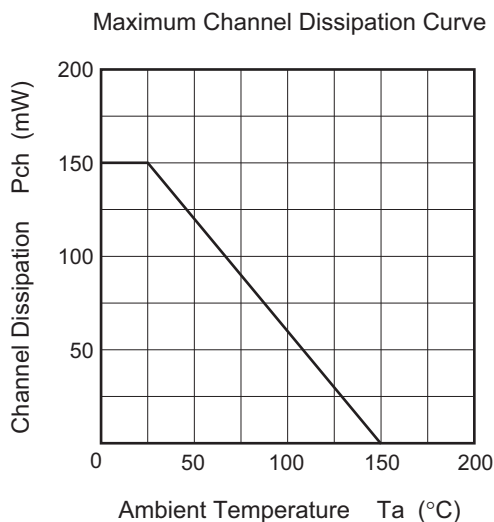
Electrical Characteristics

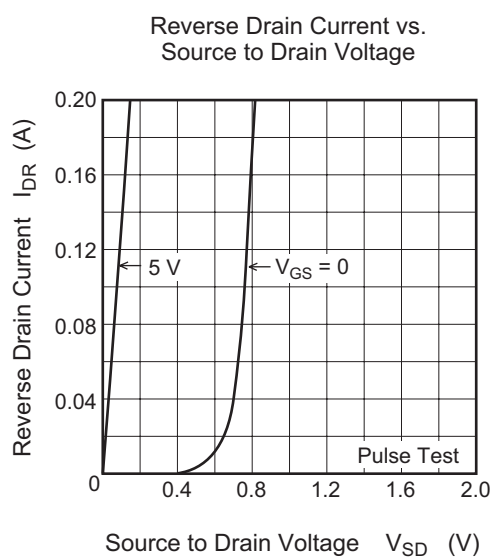
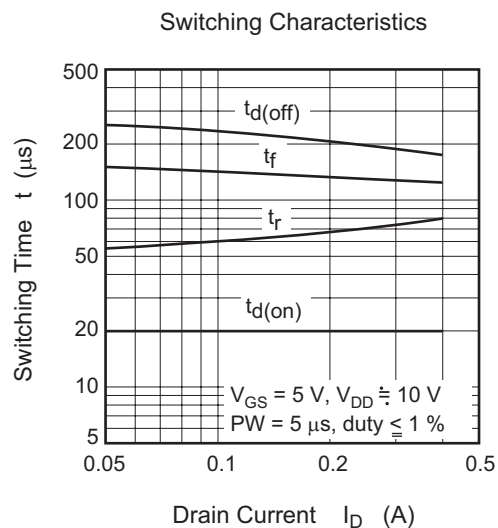
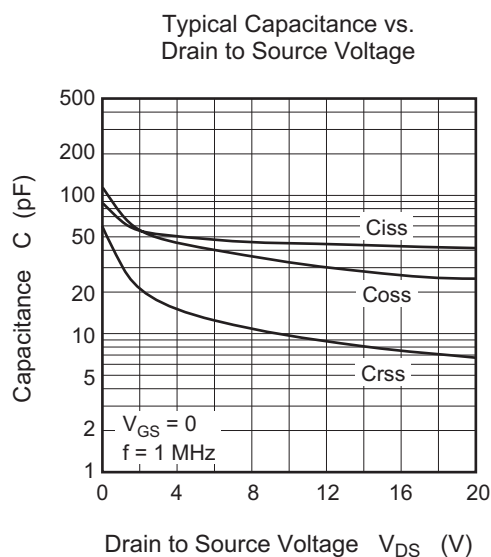
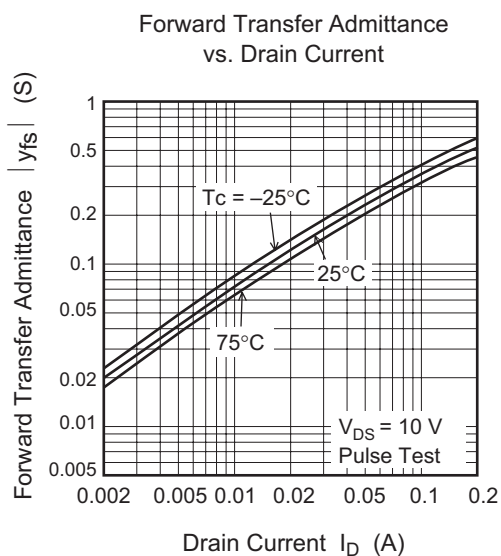
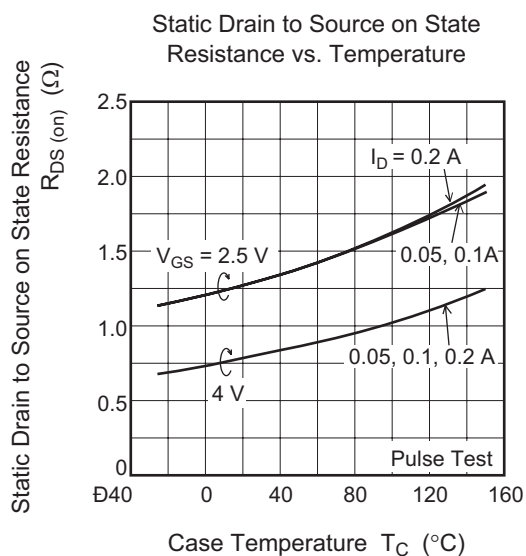
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	20	—	—	V	$I_D = 10 \mu A, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 10	—	—	V	$I_G = \pm 100 \mu A, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1.0	μA	$V_{DS} = 20 V, V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 5.0	μA	$V_{GS} = \pm 6.5 V, V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	0.5	—	1.5	V	$I_D = 10 \mu A, V_{DS} = 5 V$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.8	1.1	Ω	$I_D = 100 mA, V_{GS} = 4 V^{*2}$
		—	1.3	2.2	Ω	$I_D = 40 mA, V_{GS} = 2.5 V^{*2}$
Forward transfer admittance	$ y_{fs} $	0.22	0.35	—	S	$I_D = 100 mA, V_{DS} = 10 V^{*2}$
Input capacitance	C_{iss}	—	45	—	pF	$V_{DS} = 10 V, V_{GS} = 0,$ $f = 1 MHz$
Output capacitance	C_{oss}	—	33	—	pF	
Reverse transfer capacitance	C_{rss}	—	9.6	—	pF	
Turn-on delay time	$t_{d(on)}$	—	20	—	ns	$V_{GS} = 5 V, I_D = 100 mA,$ $R_L = 100 \Omega$
Rise time	t_r	—	60	—	ns	
Turn-off delay time	$t_{d(off)}$	—	240	—	ns	
Fall time	t_f	—	140	—	ns	

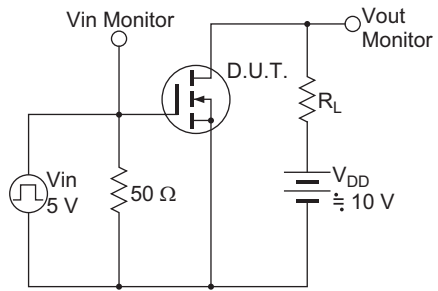
Notes: 2. Pulse test

Main Characteristics

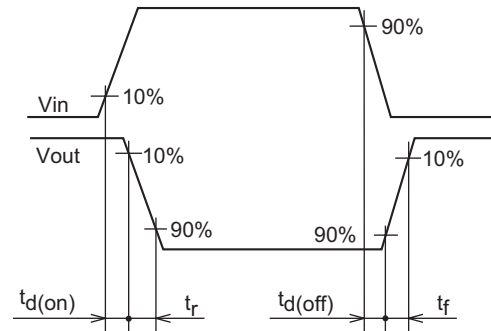




Switching Time Test Circuit



Waveform



Package Dimensions

JEITA Package Code	RENESAS Code	Package Name	MASS[Typ.]
SC-59A	PLSP0003ZB-A	MPAK(T) / MPAK(T)/V, MPAK / MPAKV	0.011g

Technical drawing of the SC-59A package showing top, side, and cross-section views. Dimensions include D, A, e, HE, E, b, A2, A1, S, b, b1, c1, c, and A-A Section. The side view shows a bent lead with dimensions Q, c, L, L1, LP, A3, e, and e1. The cross-section A-A shows dimensions b, b1, c1, and c.

A-A Section

Pattern of terminal position areas

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	1.0	—	1.3
A ₁	0	—	0.1
A ₂	1.0	1.1	1.2
A ₃	—	0.25	—
b	0.35	0.42	0.5
b ₁	—	0.4	—
c	0.1	0.13	0.15
c ₁	—	0.11	—
D	2.7	—	3.1
E	1.35	1.5	1.65
e	—	0.95	—
HE	2.2	2.8	3.0
L	0.35	—	0.75
L ₁	0.15	—	0.55
L _P	0.25	—	0.65
x	—	—	0.05
b ₂	—	—	0.55
e ₁	—	1.95	—
l ₁	—	—	1.05
Q	—	0.3	—

Ordering Information

Part Name	Quantity	Shipping Container
2SK2570ZL-TL-E	3000 pcs	Taping
2SK2570ZL-TR-E	3000 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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