# Eight-Output, 200-MHz Zero Delay Buffer

## Features

- **50-MHz to 200-MHz operating range**
- **650-ps Total Timing Budget™ (TTB™) window**
- **Multiple configurations (see *Table 2*)**
- **Eight low-skew outputs**
  - **Output-output skew < 200 ps**
  - **Device-device skew < 500 ps**
- **Input-output skew < 250 ps**
- **Three-stateable outputs**
- **< 50-µA shutdown current**
- **Phase-locked loop (PLL) bypass mode (see *Table 1*)**
- **Spread Aware™**
- **16-pin TSSOP**
- **3.3V operation**
- **Commercial/Industrial temperature**

## Functional Description

The CY2308A is a high-performance 200-MHz zero delay buffer designed for high-speed clock distribution. The integrated PLL is designed for low jitter and optimized for noise rejection. These parameters are critical for reference clock distribution in systems using high-performance ASICs and microprocessors. The CY2308A PLL feedback is external and is required to be driven into the FBK pin using anyone of the outputs.

The device features a guaranteed maximum TTB window specifying all occurrences of output clocks with respect to the input reference clock across variations in output frequency, supply voltage, operating temperature, input edge rate, and process.

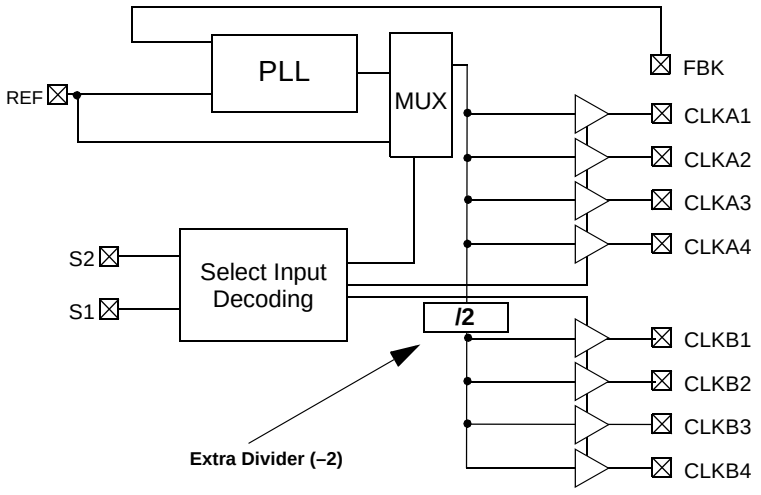
The CY2308A has two banks of four outputs each that can be controlled by the Select inputs as shown in *Table 1*. If all output clocks are not required, Bank B can be three-stated. The select inputs also allow the input clock to be directly applied to the output for chip and system testing purposes.

The CY2308A PLL enters a power-down state when there are no rising edges on the REF input. In this mode, all outputs are three-stated and the PLL is turned off, resulting in less than 50 µA of current draw. The PLL shuts down in two additional cases, as shown in *Table 1*.

The CY2308A is available in five different configurations, as shown in *Table 2*. The CY2308A–1 is the base part with the output frequencies equal to the reference if there is no divider in the feedback path. The CY2308A–1H is the high-drive version of the –1 with faster rise and fall times.

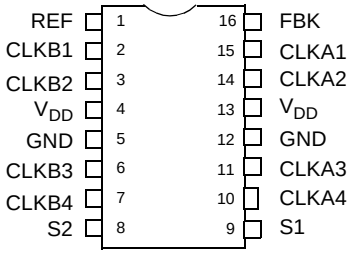
The CY2308A–2 allows the user to obtain 1X / ½X frequencies on each output bank. The exact configuration and output frequencies depends on which output drives FBK.

## Block Diagram




## Pin Configuration

**TSSOP**
**Top View**



## Pin Description

| Pin | Signal | Description |
|---|---|---|
| 1 | REF | Input reference frequency, 5V-tolerant input |
| 2 | CLKB1[2] | Clock output, Bank B |
| 3 | CLKB2[2] | Clock output, Bank B |
| 4 | $V_{DD}$ | 3.3V supply |
| 5 | GND | Ground |
| 6 | CLKB3[2] | Clock output, Bank B |
| 7 | CLKB4[2] | Clock output, Bank B |
| 8 | S2[1] | Select input, 5V-tolerant input |
| 9 | S1[1] | Select input, 5V-tolerant input |
| 10 | CLKA4[2] | Clock output, Bank A |
| 11 | CLKA3[2] | Clock output, Bank A |
| 12 | GND | Ground |
| 13 | $V_{DD}$ | 3.3V supply |
| 14 | CLKA2[2] | Clock output, Bank A |
| 15 | CLKA1[2] | Clock output, Bank A |
| 16 | FBK | PLL feedback input |

**Table 1. Select Input Decoding**

| S2 | S1 | CLOCK A1–A4 | CLOCK B1–B4 | Output Source | PLL Shutdown |
|---|---|---|---|---|---|
| 0 | 0 | Three-state | Three-state | PLL | Y |
| 0 | 1 | Driven | Three-state | PLL | N |
| 1 | 0 | Driven | Driven | Reference | Y |
| 1 | 1 | Driven | Driven | PLL | N |

**Table 2. Available CY2308A Configurations**

| Device | Feedback From | Bank A Frequency | Bank B Frequency |
|---|---|---|---|
| CY2308A–1 | Bank A or Bank B | Reference | Reference |
| CY2308A–1H | Bank A or Bank B | Reference | Reference |
| CY2308A–2 | Bank A | Reference | Reference/2 |
| CY2308A–2 | Bank B | Reference X2 | Reference |

**Notes:**
1. Weak pull-up.
2. Weak pull-down.

## Maximum Ratings

Supply Voltage to Ground Potential ..... –0.5V to +7.0V

DC Input Voltage
(Except Ref, S1, S2) .....–0.5V to $V_{DD}$ + 0.5V

DC Input Voltage (REF, S1, S2).....–0.5 to 7V

Storage Temperature .....–65°C to +150°C

Junction Temperature..... 125°C

Junction-to-Ambient Thermal Resistance

16-pin TSSOP ..... 115°C/W

Static Discharge Voltage
(per MIL-STD-883, Method 3015) .....> 2000V

**Table 3. Operating Conditions for CY2308AZC–XX Commercial Temperature Devices**

| Parameter | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 3.135 | 3.465 | V |
| $T_A$ | Operating Temperature (Ambient Temperature) | 0 | 70 | °C |
| $C_{IN}$ | Input Capacitance | | 7 | pF |
| $t_{PU}$ | Power-up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic) | 0.05 | 500 | ms |

**Table 4. Electrical Characteristics for CY2308AZC–XX Commercial Temperature Devices**

| Parameter | Description | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{IL}$ | Input LOW Voltage | CMOS Levels, 30% of $V_{DD}$ | | 0.25 | $V_{DD}$ |
| $V_{IH}$ | Input HIGH Voltage | CMOS Levels, 70% of $V_{DD}$ | 0.7 | | $V_{DD}$ |
| $I_{IL}$ | Input LOW Current | $V_{IN}$ = 0V | | 50.0 | µA |
| $I_{IH}$ | Input HIGH Current | $V_{IN}$ = $V_{DD}$ | | 10.0 | µA |
| $I_{OL}$ | Output LOW Current[3] (–1, –2) | $V_{OL}$ = 0.5V | 12 | | mA |
| | (–1H) | | 18 | | |
| $I_{OH}$ | Output HIGH Current[3] (–1, –2) | $V_{OH}$ = $V_{DD}$ – 0.5V | | –12 | mA |
| | (–1H) | | | –18 | |
| $I_{DDS}$ | Power-down Supply Current | REF = 0V, S1 = $V_{DD}$, S2 = $V_{DD}$ | | 50 | µA |
| $I_{DD}$ | Supply Current | Unloaded outputs @ 200 MHz | | 115 | mA |
| | | Loaded outputs @ 200 MHz, $C_L$ = 10 pF | | 145 | |

**Table 5. Switching Characteristics for CY2308AZC–XX Commercial Temperature Devices**[4]

| Parameter | Name | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| | Reference Frequency | | 50 | | 200 | MHz |
| | Reference Edge Rate | 30% to 70% of $V_{DD}$ | 0.5 | | 4 | V/ns |
| | Reference Duty Cycle | | 25 | | 75 | % |
| $t_1$ | Output Frequency | $C_L$ = 10 pF | 50 | | 200 | MHz |
| | | $C_L$ = 15 pF | 50 | | 140 | MHz |
| | Duty Cycle[3] = $t_2 \div t_1$ | Measured at $V_{DD}/2$ | 45.0 | 50.0 | 55.0 | % |
| $t_3$ | Rising Edge Rate[3] (–1, –2) | 20% to 80% of $V_{DD}$, $C_L$ = 15 pF | 0.8 | | 4 | V/ns |
| | Rising Edge Rate[3] (–1H) | 20% to 80% of $V_{DD}$, $C_L$ = 15 pF | 1 | | 4 | V/ns |
| $t_4$ | Falling Edge Rate[3] (–1, –2) | 80% to 20% of $V_{DD}$, $C_L$ = 15 pF | 0.8 | | 4 | V/ns |
| | Falling Edge Rate[3] (–1H) | 80% to 20% of $V_{DD}$, $C_L$ = 15 pF | 1 | | 4 | V/ns |
| $t_{TB}$ | TTB window, Bank A and B Same Frequency[5] | Outputs @ 200 MHz, Tracking Skew Not Included | | | 650 | ps |
| | TTB window, Bank A and B Different Frequency[5] | | | | 850 | |

**Notes:**

3. Parameter is guaranteed by design and characterization. Not 100% tested in production.
4. All parameters are specified with loaded outputs.
5. $t_{TB}$ is the window between the earliest and the latest output clocks with respect to the input reference clock across variations in output frequency, supply voltage, operating temperature, input clock edge rate, and process. The measurements are taken with the AC test load specified and include output-output skew, cycle-cycle jitter, and dynamic phase error. $t_{TB}$ will be equal to or smaller than the maximum specified value at a given output frequency.

**Table 5. Switching Characteristics for CY2308AZC–XX Commercial Temperature Devices[4]** (continued)

| Parameter | Name | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_5$ | Output-to-Output Skew[3] | All Outputs Equally Loaded | | | 200 | ps |
| $t_6$ | Input-to-Output Skew (Static Phase Error)[3] | Measured at $V_{DD}/2$, REF to FBK | | | 250 | ps |
| $t_7$ | Device-to-Device Skew[3] | Measured at $V_{DD}/2$ | | | 500 | ps |
| $t_J$ | Cycle-to-Cycle Jitter,[3] Bank A and B Same Frequency | Loaded Outputs | | | 200 | ps |
| | | | | | 35 | $ps_{RMS}$ |
| | Cycle-to-Cycle Jitter,[3] Bank A and B Different Frequency | Loaded Outputs | | | 400 | ps |
| | | | | | 70 | $ps_{RMS}$ |
| $t_{LOCK}$ | PLL Lock Time[3] | Stable Power Supply, Valid Clock at REF | | | 1.0 | ms |

**Table 6. Operating Conditions for CY2308AZI–XX Industrial Temperature Devices**

| Parameter | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 3.135 | 3.465 | V |
| $T_A$ | Operating Temperature (Ambient Temperature) | –40 | 85 | °C |
| $C_{IN}$ | Input Capacitance | | 7 | pF |
| $t_{PU}$ | Power-up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic) | 0.05 | 500 | ms |

**Table 7. Electrical Characteristics for CY2308AZI-XX Industrial Temperature Devices**

| Parameter | Description | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{IL}$ | Input LOW Voltage | CMOS Levels, 30% of $V_{DD}$ | | 0.25 | $V_{DD}$ |
| $V_{IH}$ | Input HIGH Voltage | CMOS Levels, 70% of $V_{DD}$ | 0.7 | | $V_{DD}$ |
| $I_{IL}$ | Input LOW Current | $V_{IN}$ = 0V | | 50.0 | µA |
| $I_{IH}$ | Input HIGH Current | $V_{IN} = V_{DD}$ | | 10.0 | µA |
| $I_{OL}$ | Output LOW Current[3] (–1, –2) | $V_{OL}$ = 0.5V | 10 | | mA |
| | (–1H) | | 15 | | |
| $I_{OH}$ | Output HIGH Current[3] (–1, –2) | $V_{OH} = V_{DD} – 0.5V$ | | –10 | mA |
| | (–1H) | | | –15 | |
| $I_{DDS}$ | Power-down Supply Current | REF = 0V, S1 = $V_{DD}$, S2 = $V_{DD}$ | | 50 | µA |
| $I_{DD}$ | Supply Current | Unloaded outputs @ 133 MHz | | 80.0 | mA |
| | | Loaded outputs @ 133 MHz, $C_L$ = 10 pF | | 110.0 | |

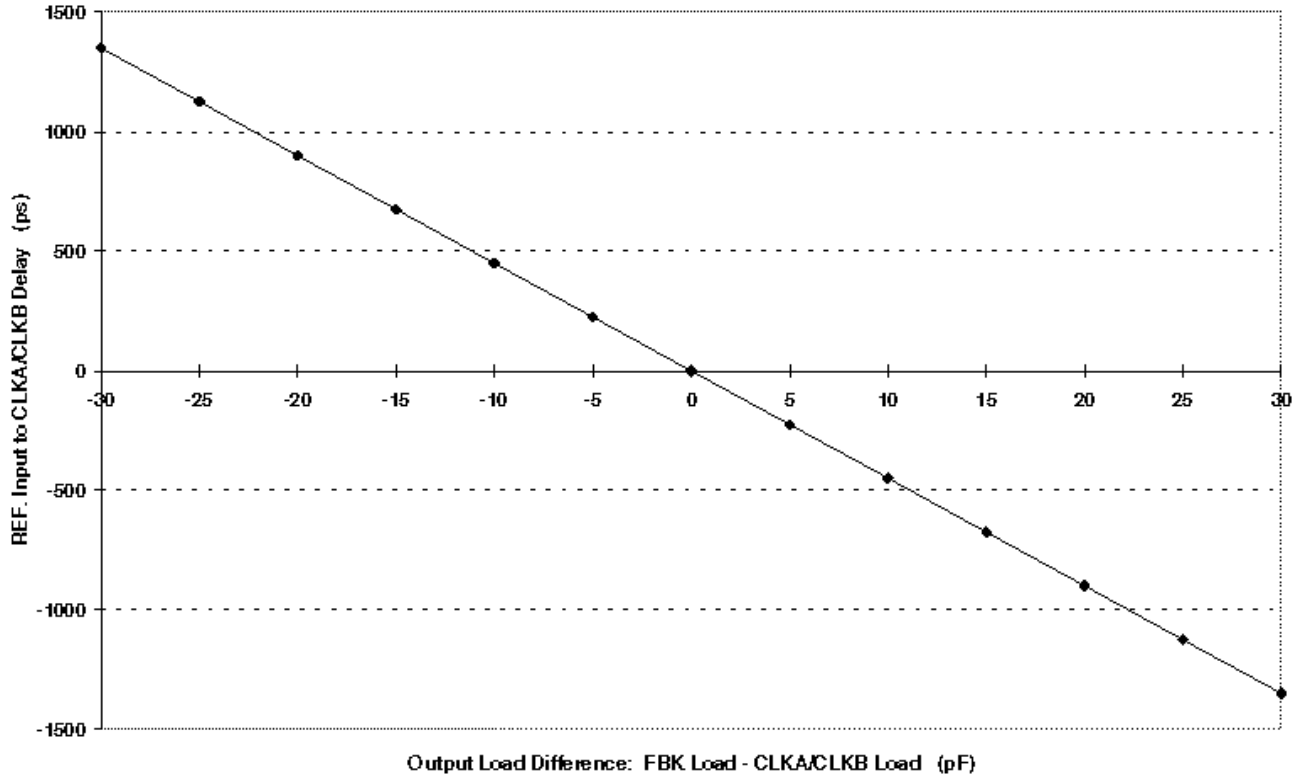
**Table 8. Switching Characteristics for CY2308AZI–XX Industrial Temperature Devices[4]**

| Parameter | Name | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| | Reference Frequency | | 50 | | 133 | MHz |
| | Reference Edge Rate | 30% to 70% of $V_{DD}$ | 0.5 | | 4 | V/ns |
| | Reference Duty Cycle | | 25 | | 75 | % |
| $t_1$ | Output Frequency | $C_L$ = 10 pF | 50 | | 133 | MHz |
| | Duty Cycle[3] = $t_2 \div t_1$ | Measured at $V_{DD}/2$ | 40.0 | 50.0 | 60.0 | % |
| $t_3$ | Rising Edge Rate[3] (–1, –2) | 20% to 80% of $V_{DD}$, $C_L$ = 15 pF | 0.5 | | 3 | V/ns |
| | Rising Edge Rate[3] (–1H) | 20% to 80% of $V_{DD}$, $C_L$ = 15 pF | 0.8 | | 4 | V/ns |
| $t_4$ | Falling Edge Rate[3] (–1, –2) | 80% to 20% of $V_{DD}$, $C_L$ = 15 pF | 0.5 | | 3 | V/ns |
| | Falling Edge Rate[3] (–1H) | 80% to 20% of $V_{DD}$, $C_L$ = 15 pF | 0.8 | | 4 | V/ns |

**Table 8. Switching Characteristics for CY2308AZI–XX Industrial Temperature Devices**[4] (continued)

| Parameter | Name | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{TB}$ | Total Timing Budget window, Bank A and B Same Frequency[5] | Outputs @ 133 MHz, Tracking Skew Not Included | | | 650 | ps |
| | Total Timing Budget window, Bank A and B Different Frequency[5] | | | | 850 | |
| $t_5$ | Output-to-Output Skew[3] | All Outputs Equally Loaded | | | 200 | ps |
| $t_6$ | Input-to-Output Skew (Static Phase Error)[3] | Measured at $V_{DD}/2$, REF to FBK | | | 250 | ps |
| $t_7$ | Device-to-Device Skew[3] | Measured at $V_{DD}/2$ | | | 500 | ps |
| $t_J$ | Cycle-to-Cycle Jitter[3], Bank A and B Same Frequency | Loaded Outputs | | | 200 | ps |
| | | | | | 35 | $ps_{RMS}$ |
| | Cycle-to-Cycle Jitter[3], Bank A and B Different Frequency | Loaded Outputs | | | 400 | ps |
| | | | | | 70 | $ps_{RMS}$ |
| $t_{LOCK}$ | PLL Lock Time[3] | Stable Power Supply, Valid Clock at REF | | | 1.0 | ms |

**REF. Input to CLKA/CLKB Delay vs. Difference in Loading Between FBK Pin and CLKA/CLKB Pins**




## Zero Delay and Skew Control

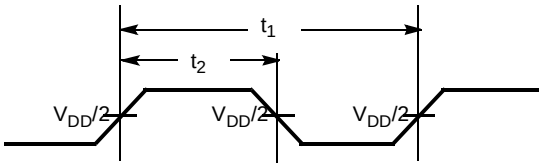
To close the feedback loop of the CY2308A, the FBK can be driven from any of the eight available output pins. The output driving the FBK will be driving a total load of 7 pF plus any additional load that it drives. The relative loading of this output (with respect to the remaining outputs) can adjust the input-output delay. See *REF Input to CLK Delay vs. Loading Difference*.

For applications requiring zero input-output delay, all outputs including the one providing feedback should be equally loaded. If input-output delay adjustments are required, use the above graph to calculate loading differences between the feedback output and remaining outputs.

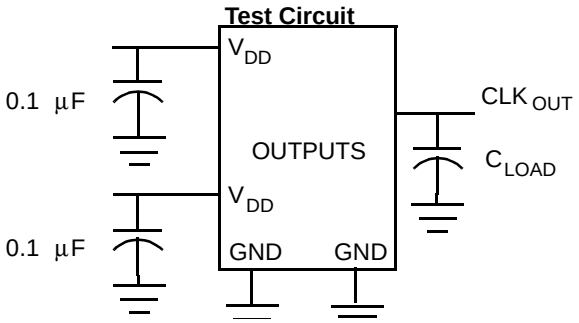
For zero output-output skew, be sure to load outputs equally. For further information on using CY2308A, refer to the application note *CY2308: Zero Delay Buffer*.

## Test Circuits

**Duty Cycle Timing**

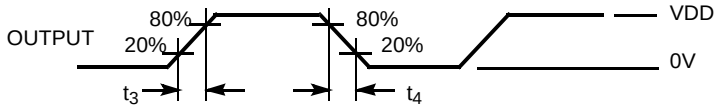



**Test Circuit**

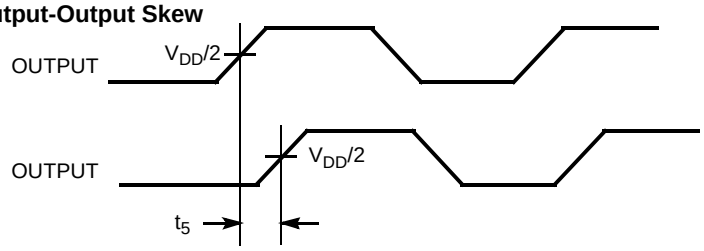



## Switching Waveforms

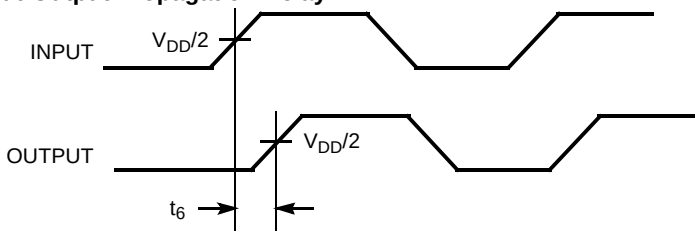
**All Outputs Rise/Fall Time**



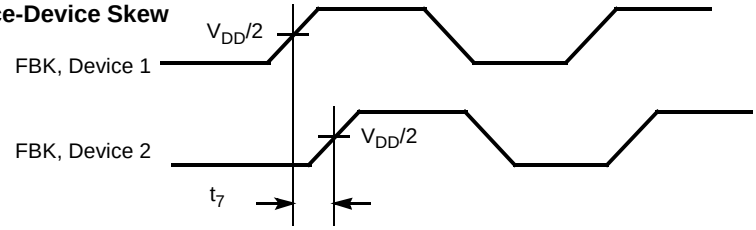

**Output-Output Skew**




**Input-Output Propagation Delay**




**Device-Device Skew**




## Ordering Information

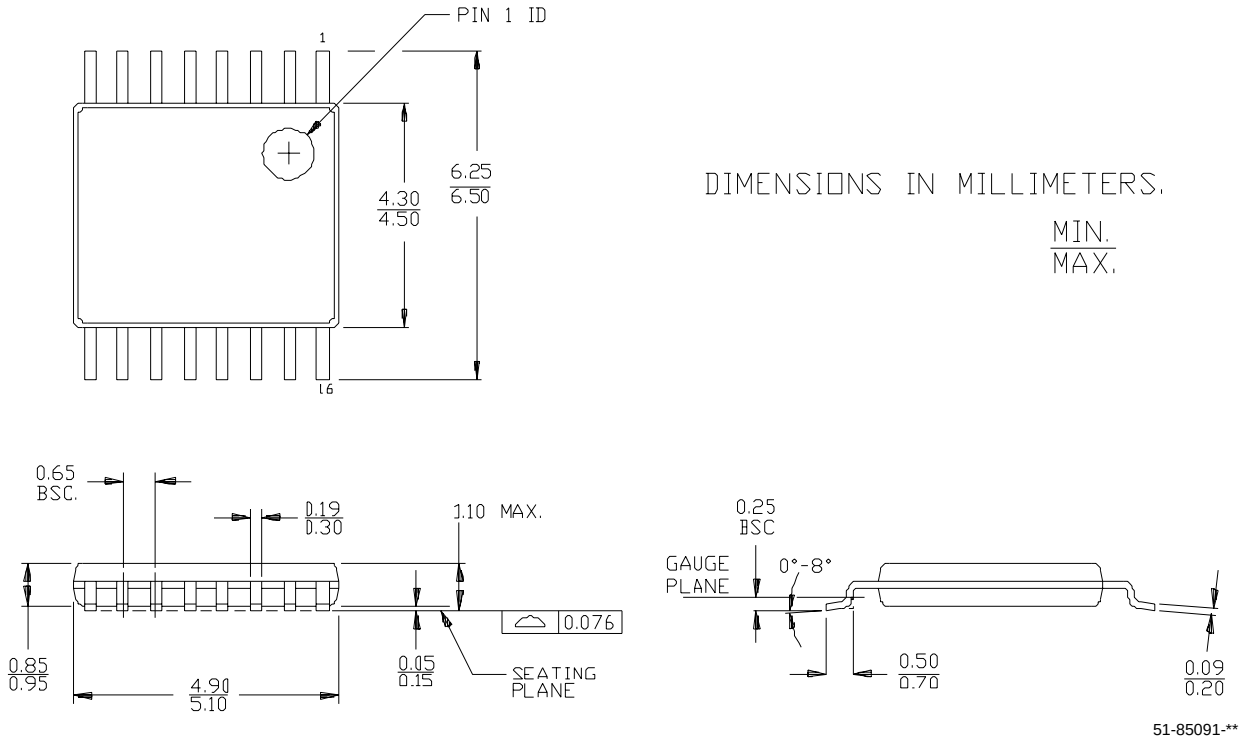
| Ordering Code | Package Type | Operating Range |
|---|---|---|
| CY2308AZC-1 | 16-pin 4.4-mm TSSOP | Commercial, 0°C to 70°C |
| CY2308AZC–1T | 16-pin 4.4-mm TSSOP – Tape and Reel | Commercial, 0°C to 70°C |
| CY2308AZC–1H | 16-pin 4.4-mm TSSOP | Commercial, 0°C to 70°C |
| CY2308AZC–1HT | 16-pin 4.4-mm TSSOP – Tape and Reel | Commercial, 0°C to 70°C |
| CY2308AZC–2 | 16-pin 4.4-mm TSSOP | Commercial, 0°C to 70°C |
| CY2308AZC–2T | 16-pin 4.4-mm TSSOP – Tape and Reel | Commercial, 0°C to 70°C |
| CY2308AZI-1 | 16-pin 4.4-mm TSSOP | Industrial, –40°C to 85°C |
| CY2308AZI-1T | 16-pin 4.4-mm TSSOP – Tape and Reel | Industrial, –40°C to 85°C |

## Ordering Information (continued)

| Ordering Code | Package Type | Operating Range |
|---|---|---|
| CY2308AZI–1H | 16-pin 4.4-mm TSSOP | Industrial, –40°C to 85°C |
| CY2308AZI–1HT | 16-pin 4.4-mm TSSOP – Tape and Reel | Industrial, –40°C to 85°C |
| CY2308AZI-2 | 16-pin 4.4-mm TSSOP | Industrial, –40°C to 85°C |
| CY2308AZI-2T | 16-pin 4.4-mm TSSOP – Tape and Reel | Industrial, –40°C to 85°C |

## Package Diagram

**16-Lead Thin Shrunk Small Outline Package (4.40 MM Body) Z16**

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## Document History Page

| Document Title: CY2308A Eight-Output, 200-MHz Zero Delay Buffer<br>Document Number: 38-07377 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 112938 | 04/02/02 | CTK | New Data Sheet |
| *A | 114685 | 07/17/02 | HWT | Change freq. of operation to 50 MHz–200 MHz<br>Eliminate specification related to 30-pF load |
| *B | 121892 | 12/14/02 | RBI | Power-up requirements added to Operating Conditions information |
| *C | 124597 | 03/06/03 | RGL | Changed $V_{IL}$ max value in Commercial Temp. Device from 0.3V to 0.25V<br>Changed $I_{DD}$ max values in Commercial Temp. Device from 75 and 150 to 115 and 145 mA, respectively<br>Changed $V_{IL}$ max value in Industrial Temp Device from 0.3V to 0.25V<br>Changed $I_{DD}$ max value in Industrial Temp Device from 60 and 120 mA to 80 and 110 mA<br>Removed Preliminary (final data sheet) |