National Semiconductor

ADVANCE INFORMATION

GAL16Z8 In-System re-Programmable (isp) Generic Array Logic

General Description

The NSC GAL®16Z8 is a revolutionary programmable logic device featuring 5V only in-system reprogrammability and real time, in-system diagnostic capabilties. This is made possible by on-chip circuitry which generates and shapes the necessary high voltage internal programming control signals. Using NSC UlltraMOS® technology, this device provides true bipolar performance at significantly reduced power levels.

The 24-pin GAL16Z8 is architecturally and parametrically identical to the 20-pin GAL16V8, but includes 4 extra pins to control in-system programming. These extra pins are: data clock (DCLK), serial data in (SDI), serial data out (SDO), and mode control (MODE). These pins are not associated with normal logic functions and are used only during programming. Additionally, this 4-pin interface allows an unlimited number of devices to be cascaded to form a serial programming and diagnostics loop.

Advanced features that simplify programming and reduce test time, coupled with E²CMOS™ reprogrammable cells, enable complete AC, DC, programmability, and functionality testing of each GAL16Z8 during manufacturing and allows National Semiconductor to guarantee 100% performance to all specifications.

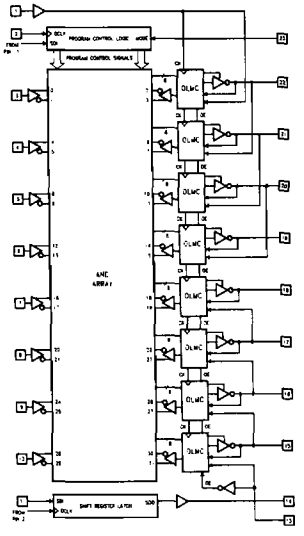
Features

- In-system reconfigurable—5V only programming
  - — Change logic "On the Fly" (in less than 1s) Nonvolatile electrically erasable technology
- Diagnositics mode for controllability and observability of system logic
- High performance E²CMOS technology
  - — High speed: 25 ns max propagation delay
  - — Low power: 90 mA max active
- Eight output logic macrocells
  - — Maximum flexibility for complex logic designs
  - — Also emulates 20-pin PAL® devices with full function/fuse map/parametric compatibility
- Preload and power-up reset of all registers
  - — 100% functional testability
- Space saving 24-pin, 300-mil DIP
- Minimum 10,000 erase/write cycles
- Data retention exceeds 20 years
- Electronic signature for identification
- Applications include:
  - — Reconfigurable interfaces
  - — Copy protection and security schemes
  - — erasable hardware
  - — password systems
  - — proprietary hardware/software interlocks

PAL Replacement by Device Type

"Small-PAL" Mode				"Registered-PAL" Mode			"Medium-PAL" Mode
10L8	12L6	14L4	16L2	16R8	16R6	16R4	16L8
10H8	12H6	14H4	16H2	16RP8	16RP6	16RP4	16H8
10P8	12P6	14P4	16P2				16P8

Block Diagram—GAL16Z8



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Overview

The GAL16Z8 device has three basic modes of operation: NORMAL, DIAGNOSTIC and PROGRAM. These three modes are controlled by the system designer through the use of a sophisticated on-chip state machine.

In addition, the GAL16Z8 has been optimized so that the use of 2 or more devices on a board requires the same amount of control overhead as a single device would. This Serial Loop approach applies to the DIAGNOSTIC and PROGRAM operation modes of the device.

The balance of this document will perform a general review of the operation of the GAL16Z8 in its various modes and will explain the use of these control pins.

Mode Control and Operation

The signals used to control this device are the same for both the DIAGNOSTIC and PROGRAM modes. During NORMAL mode, the control pins serve no function other than to control the transition to another mode. The shared control pin approach allows for a simple multi-mode operation with minimal system or board overhead.

The four control signals are TTL level signals; MODE, DCLK, SDI and SDO. These signals are used to transition from mode to mode and through each of the five states as shown in *Figure 1*. MODE is used only to control the on-chip state machine. DCLK is used for mode control and for the orderly clocking of data into the 16Z8 from the SDI (serial data in) pin as well as out of the device through the SDO (serial data out) pin. SDI is also used for state machine control.

The current state cannot be explicitly observed, however, an "escape" sequence ("HL") to the NORMAL mode is always available to start the process fresh. Caution should be used when using this escape path as the pattern in the device may not be valid if an erase or reprogramming operation was in progress.

Diagnostic Mode

From the NORMAL mode, the device transitions to the DIAGNOSTIC:Preload state (mode:state). In this mode, the values in the Macrocell registers can be interrogated or "pre-"loaded for diagnostic testing of the system. Advanced system design requires full control and observability of all registers on a board.

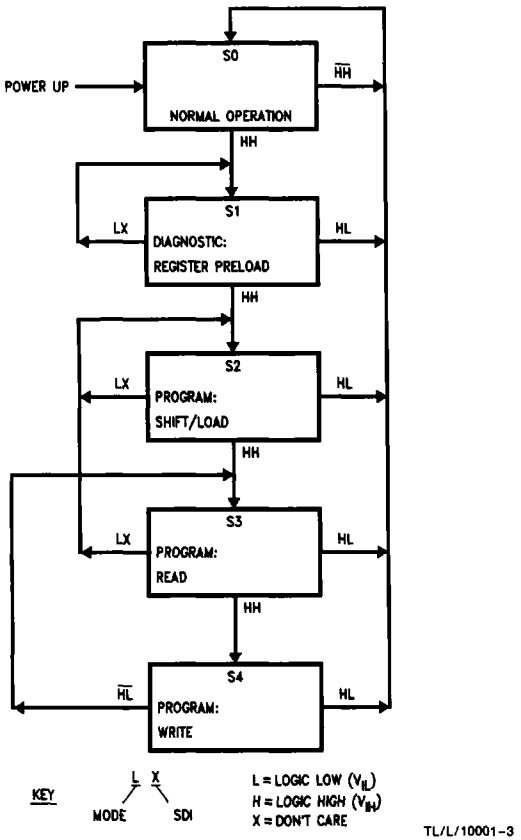

FIGURE 1. On-Chip State Machine

Diagnostic Mode (Continued)

Upon entry to the DIAGNOSTIC:Preload state, the data on the device output pins (15-22) is latched and held to its 1, 0 or TRI-STATE® condition. This is important as the DIAGNOSTIC:Preload state configures a serial loop from the SDI pin through each of the registers to the SDO pin. Data is shifted across all of the registers during diagnostics *(Figure 2)*. The latching of the current output data insures that the system is not influenced by the changing register contents until such time as the DIAGNOSTIC:Preload state is exited.

The access to the macrocell data is through the SDI and SDO pins. While in the DIAGNOSTIC:Preload state, the value in each register is serially shifted out through SDO with each pulse of the DCLK pin. Similarly, new data can be preloaded into the registers through the SDI pin.

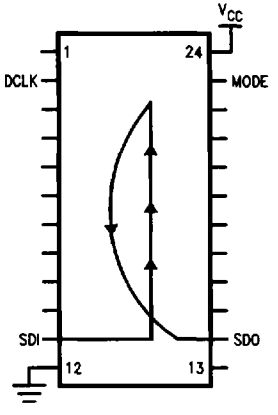

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FIGURE 2. Diagnostic/Program Pinout

The number of registers in a 16Z8 is a function of the configuration of each macrocell. The length of the serial path, and therefore the number of bits of data shifted in or out of the device, is a function of the number of macrocells which are configured to have registers.

Program Mode

The PROGRAM mode can only be entered from the DIAGNOSTIC:Preload state. When this transition is made, the value of the user programmable TRI-STATE Bit (TSB) is examined to determine the data condition that is held on the device output pins 15–22. The data can either remain latched to 1-0-Z as in the DIAGNOSTIC mode or the data can be forced to high impedance. Again, this feature allows complete control of the system during programming.

The PROGRAM mode consists of three states of the on-chip state machine: SHIFT, READ and WRITE. Proper sequencing of these states is necessary to program and verify the device. Programming and verification is accomplished using a Serial Register Latch (SRL) to program or verify a row of data at a time.

PROGRAM:SHIFT

During the PROGRAM:Shift state, the 88-bit SRL is serially loaded with 82 bits of data and 6 bits of row address for each row to be programmed. The architecture and Electronic Signature of the 16Z8 are also programmed in the same manner. DCLK is used to shift data into SDI for the loading process.

PROGRAM:READ

Verification of data in the array is accomplished in the PROGRAM:Read state. Exiting the PROGRAM:Read state to the PROGRAM:Shift state causes the contents of the array row to be copied to the SRL. This data can be shifted out as outlined above. Programming the Security Cell prevents valid data from being loaded into the SRL. This feature is provided to prevent subsequent copying of the cell patterns.

PROGRAM:WRITE

The actual programming cycle occurs in the PROGRAM:Write state. The data to be programmed is loaded into the SRL in the PROGRAM:Shift state prior to executing the write cycle. It is the responsibility of the system control logic to assure that the device stays in the PROGRAM:Write state for a sufficient time to program the E^2 cells, approximately 10 ms. The PROGRAM:Write is then exited to the PROGRAM:Read state for verification of the data.

The 16Z8 is completely erased by addressing an "erase" row address using the same process outlined above. It is necessary to bulk-erase the device prior to rewriting any pattern into the device as each row write cycle does not include an automatic erase of that row.

The entire programming process takes less than ½ second. The bulk erase is 10 ms, and each of the 36 programmable rows can be loaded, programmed and verified in approximately 10.5 ms for a total time of 0.39 seconds. During this time, the device output pins are latched or in the high impedance condition and the 16Z8 is not responding to changes on its input pins. The system must accommodate this programming time.

Serial Diagnostic/Program Loop Operation

Figure 3 shows a typical GAL16Z8 system. Notice that several devices have been cascaded together to form a serial programming loop. This arrangement allows the simultaneous transfer of programming and diagnostic data through every In-System re-Programmable GAL device in the system with no additional control logic necessary. When controlling multiple devices in such a loop, the basic diagnostic and programming algorithms remain unchanged. However, there are some additional considerations.

In a serial programming loop, the SDO of the first device is connected to the SDI of the second; the SDO of the second to the SDI of the third, and so on. DCLK and MODE are common for every device. With such an arrangement, devices in the loop are always in the same state, but the data being shifted into their respective SRLs may be different. Note that, before data reaches the SDI input of any given device, it must first pass through the 88-bit SRL of every device ahead of it in the loop. The SRL is asynchronously bypassed (SDO = SDI) whenever MODE = 1 allowing SDI to function as both a data and mode control pin.

In a serial diagnostic loop, the length of the loop is a function of the number of OLMC registers being used. On the other hand, in a serial programming loop, data transfers always occur in multiples of 88 bits, as the data must pass through the SRL of other devices in the loop.

Because all devices in a loop are always in the same state, reprogramming just one out of "n" devices would seem to be a problem. This, however, is not the case, as several options exist. The most obvious solution is to simply reprogram all of the devices, even if the new pattern is the same as the old. The system "down" time is effectively the same since all the devices reprogram in parallel.

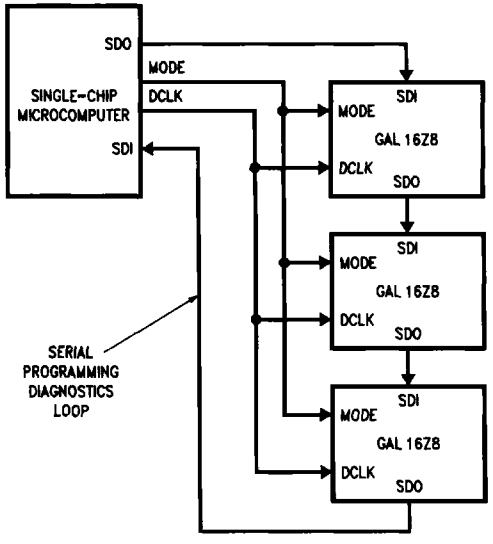

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FIGURE 3. Typical GAL16Z8 System