4. ELECTRICAL CHARACTERISTICS

4.1 HD64180R0 ELECTRICAL CHARACTERISTICS

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage	V_{CC}	$-0.3 \sim +7.0$	V
Input Voltage	V_{in}	$-0.3 \sim V_{CC}+0.3$	V
Operating Temperature	T_{opr}	$-20 \sim +75$	°C
Storage Temperature	T_{stg}	$-55 \sim +150$	°C

[NOTE] Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect reliability of LSI.

■ DC CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, Ta = −20 ~ +75°C, unless otherwise noted.)

Symbol	Item	Condition	min	typ	max	Unit
V_{IH1}	Input "H" Voltage $\overline{RESET}$, EXTAL, $\overline{NMI}$		$V_{CC}-0.6$	–	$V_{CC}+0.3$	V
V_{IH2}	Input "H" Voltage Except $\overline{RESET}$, EXTAL, $\overline{NMI}$		2.0	–	$V_{CC}+0.3$	V
V_{IL1}	Input "L" Voltage $\overline{RESET}$, EXTAL, $\overline{NMI}$		−0.3	–	0.6	V
V_{IL2}	Input "L" Voltage Except $\overline{RESET}$, EXTAL, $\overline{NMI}$		−0.3	–	0.8	V
V_{OH}	Output "H" Voltage All Outputs	$I_{OH} = -200\mu A$	2.4	–	–	V
		$I_{OH} = -20\mu A$	$V_{CC}-1.2$	–	–	
V_{OL}	Output "L" Voltage All Outputs	I_{OL} = 1.6 mA	–	–	0.45	V
I_{IL}	Input Leakage Current All Inputs Except XTAL, EXTAL	$Vin = 0.5 \sim V_{CC}-0.5$	–	–	1.0	μA
I_{TL}	Three State Leakage Current	$Vin = 0.5 \sim V_{CC}-0.5$	–	–	1.0	μA
I_{CC}*	Power Dissipation (Normal Operation)	f=4 MHz	–	10	20	mA
		f=6 MHz	–	15	30	
	Power Dissipation (SYSTEM STOP mode)	f=4 MHz	–	2.5	5.0	mA
		f=6 MHz	–	3.8	7.5	
Cp	Pin Capacitance	Vin=0V, f=1 MHz Ta=25°C	–	–	12	pF

* $V_{IHmin} = V_{CC}-1.0V$, $V_{ILmax} = 0.8V$ (all output terminals are at no load.)

■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, Ta = −20 ~ +75°C, unless otherwise noted.)

Symbol	Item	HD64A180R0			HD64B180R0			Unit
		min	typ	max	min	typ	max	
t_{cyc}	Clock Cycle Time	250	–	2000	162	–	2000	ns
t_{CHW}	Clock "H" Pulse Width	110	–	–	57	–	–	ns
t_{CLW}	Clock "L" Pulse Width	100	–	–	57	–	–	ns
t_{cf}	Clock Fall Time	–	–	25	–	–	25	ns
t_{cr}	Clock Rise Time	–	–	20	–	–	20	ns
t_{AD}	Address Delay Time	–	–	110 130*	–	–	105 125*	ns
t_{AS}	Address Set-up Time ($\overline{ME}$ or $\overline{IOE}$ ↓)	45 30**	–	–	10 −15**	–	–	ns
t_{MED1}	$\overline{ME}$ Delay Time 1	–	–	85	–	–	75	ns
t_{RDD1}	$\overline{RD}$ Delay Time 1	–	–	85	–	–	75	ns
t_{LD1}	$\overline{LIR}$ Delay Time 1	–	–	105 120***	–	–	100 115***	ns
t_{AH}	Address Hold Time ($\overline{ME}$, $\overline{IOE}$, $\overline{RD}$ or $\overline{WR}$ ↑)	80	–	–	35	–	–	ns
t_{MED2}	$\overline{ME}$ Delay Time 2	–	–	85	–	–	75	ns
t_{RDD2}	$\overline{RD}$ Delay Time 2	–	–	85	–	–	75	ns
t_{LD2}	$\overline{LIR}$ Delay Time 2	–	–	105	–	–	100	ns
t_{DRS}	Data Read Set-up Time	50	–	–	45	–	–	ns
t_{DRH}	Data Read Hold Time	0	–	–	0	–	–	ns
t_{STD1}	ST Delay Time 1	–	–	110	–	–	100	ns
t_{STD2}	ST Delay Time 2	–	–	110	–	–	100	ns
t_{WS}	$\overline{WAIT}$ Set-up Time	80	–	–	40	–	–	ns
t_{WH}	$\overline{WAIT}$ Hold Time	70	–	–	40	–	–	ns

(to be continued)

NOTE) Each symbols shows the value at the following conditions.

*1. Just after RESET (Restart address = 00000H)
2. At the beginning of SLEEP mode or SYSTEM STOP mode (Starting address = 7FFFFH)
3. After BUS RELEASE mode

**1. Just after RESET (Restart address = 00000H)
2. After BUS RELEASE mode

***1. Just after RESET (Restart address = 00000H)

Symbol	Item	HD64A180R0			HD64B180R0			Unit
		min	typ	max	min	typ	max	
t_{WDZ}	Write Data Floating Delay Time	–	–	100	–	–	95	ns
t_{WRD1}	$\overline{WR}$ Delay Time 1	–	–	90	–	–	80	ns
t_{WDD}	Write Data Delay Time	–	–	110	–	–	90	ns
t_{WDS}	Write Data Set-up Time ($\overline{WR}$ ↓)	60	–	–	40	–	–	ns
t_{WRD2}	$\overline{WR}$ Delay Time 2	–	–	90	–	–	80	ns
t_{WRP}	$\overline{WR}$ Pulse Width	220	–	–	135	–	–	ns
t_{WDH}	Write Data Hold Time ($\overline{WR}$ ↑)	60	–	–	40	–	–	ns
t_{IOD1}	$\overline{IOE}$ Delay Time 1	–	–	85	–	–	75	ns
t_{IOD2}	$\overline{IOE}$ Delay Time 2	–	–	85	–	–	75	ns
t_{IOD3}	$\overline{IOE}$ Delay Time 3 ($\overline{LIR}$ ↓)	540	–	–	340	–	–	ns
t_{INTS}	$\overline{INT}$ Set-up Time (ϕ ↓)	80	–	–	70	–	–	ns
t_{INTH}	$\overline{INT}$ Hold Time (ϕ ↓)	70	–	–	60	–	–	ns
t_{NMIW}	$\overline{NMI}$ Pulse Width	120	–	–	120	–	–	ns
t_{BRS}	$\overline{BUSREQ}$ Set-up Time (ϕ ↓)	80	–	–	70	–	–	ns
t_{BRH}	$\overline{BUSREQ}$ Hold Time (ϕ ↓)	70	–	–	60	–	–	ns
t_{BAD1}	$\overline{BUSACK}$ Delay Time 1	–	–	100	–	–	95	ns
t_{BAD2}	$\overline{BUSACK}$ Delay Time 2	–	–	100	–	–	95	ns
t_{BZD}	Bus Floating Delay Time	–	–	130	–	–	125	ns
t_{MEWH}	$\overline{ME}$ Pulse Width (HIGH)	200	–	–	110	–	–	ns
t_{MEWL}	$\overline{ME}$ Pulse Width (LOW)	210	–	–	125	–	–	ns

(to be continued)

Symbol	Item	HD64A180R0			HD64B180R0			Unit
		min	typ	max	min	typ	max	
t_{RFD1}	$\overline{REF}$ Delay Time 1	–	–	110	–	–	100	ns
t_{RFD2}	$\overline{REF}$ Delay Time 2	–	–	110	–	–	100	ns
t_{HAD1}	$\overline{HALT}$ Delay Time 1	–	–	110	–	–	100	ns
t_{HAD2}	$\overline{HALT}$ Delay Time 2	–	–	110	–	–	100	ns
t_{DRQS}	$\overline{DREQi}$ Set-up Time	80	–	–	70	–	–	ns
t_{DRQH}	$\overline{DREQi}$ Hold Time	70	–	–	60	–	–	ns
t_{TED1}	$\overline{TENDi}$ Delay Time 1	–	–	85	–	–	70	ns
t_{TED2}	$\overline{TENDi}$ Delay Time 2	–	–	85	–	–	70	ns
t_{ED1}	Enable Delay Time 1	–	–	100	–	–	95	ns
t_{ED2}	Enable Delay Time 2	–	–	100	–	–	95	ns
t_{TOD}	Timer Output Delay Time	–	–	300	–	–	300	ns
t_{STDI}	CSI/O Transmit Data Delay Time (Internal Clock Operation)	–	–	200	–	–	200	ns
t_{STDE}	CSI/O Transmit Data Delay Time (External Clock Operation)	–	–	7.5 tcyc +300	–	–	7.5 tcyc +300	ns
t_{SRSI}	CSI/O Receive Data Set-up time (Internal Clock Operation)	1	–	–	1	–	–	tcyc
t_{SRHI}	CSI/O Receive Data Hold Time (Internal Clock Operation)	1	–	–	1	–	–	tcyc
t_{SRSE}	CSI/O Receive Data Set-up Time (External Clock Operation)	1	–	–	1	–	–	tcyc
t_{SRHE}	CSI/O Receive Data Hold Time (External Clock Operation)	1	–	–	1	–	–	tcyc
t_{RES}	$\overline{RESET}$ Set-up Time	120	–	–	120	–	–	ns
t_{REH}	$\overline{RESET}$ Hold Time	80	–	–	80	–	–	ns
t_{OSC}	Oscillator Stabilization Time	–	–	20	–	–	20	ms
t_{EXr}	External Clock Rise Time (EXTAL)	–	–	25	–	–	25	ns
t_{EXf}	External Clock Fall Time (EXTAL)	–	–	25	–	–	25	ns
t_{Rr}	$\overline{RESET}$ Rise Time	–	–	50	–	–	50	ms
t_{Rf}	$\overline{RESET}$ Fall Time	–	–	50	–	–	50	ms
t_{Ir}	Input Rise Time (except EXTAL, $\overline{RESET}$)	–	–	100	–	–	100	ns
t_{If}	Input Fall Time (except EXTAL, $\overline{RESET}$)	–	–	100	–	–	100	ns

4.2 HD64180R1 AND HD64180Z ELECTRICAL CHARACTERISTICS

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage	V_{CC}	$-0.3 \sim +7.0$	V
Input Voltage	V_{in}	$-0.3 \sim V_{CC}+0.3$	V
Operating Temperature	T_{opr}	$-20 \sim +75$	°C
Storage Temperature	T_{stg}	$-55 \sim +150$	°C

[NOTE] Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect reliability of LSI.

■ DC CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, Ta = −20 ~ +75°C, unless otherwise noted.)

Symbol	Item	Condition	min	typ	max	Unit
V_{IH1}	Input "H" Voltage $\overline{RESET}$, EXTAL, $\overline{NMI}$		$V_{CC}-0.6$	–	$V_{CC}+0.3$	V
V_{IH2}	Input "H" Voltage Except $\overline{RESET}$, EXTAL, $\overline{NMI}$		2.0	–	$V_{CC}+0.3$	V
V_{IL1}	Input "L" Voltage $\overline{RESET}$, EXTAL, $\overline{NMI}$		−0.3	–	0.6	V
V_{IL2}	Input "L" Voltage Except $\overline{RESET}$, EXTAL, $\overline{NMI}$		−0.3	–	0.8	V
V_{OH}	Output "H" Voltage All outputs	$I_{OH} = -200\mu A$	2.4	–	–	V
		$I_{OH} = -20\mu A$	$V_{CC}-1.2$	–	–	
V_{OL}	Output "L" Voltage All Outputs	I_{OL} = 2.2 mA	–	–	0.45	V
I_{IL}	Input Leakage Current All Inputs Except XTAL, EXTAL	Vin=0.5 ~ $V_{CC}-0.5$	–	–	1.0	μA
I_{TL}	Three State Leakage Current	Vin=0.5 ~ $V_{CC}-0.5$	–	–	1.0	μA
I_{CC}*	Power Dissipation* (Normal Operation)	f=4 MHz	–	10	20	mA
		f=6 MHz	–	15	30	
		f=8 MHz	–	20	40	
	Power Dissipation* (SYSTEM STOP mode)	f=4 MHz	–	2.5	5.0	
		f=6 MHz	–	3.8	7.5	
		f=8 MHz	–	5.0	10.0	
Cp	Pin Capacitance	Vin=0V, f=1 MHz Ta=25°C	–	–	12	pF

* $V_{IHmin} = V_{CC}-1.0V$, $V_{ILmax} = 0.8V$ (all output terminals are at no load.)

■ HD64180R1 AC CHARACTERISTICS

(V_{CC} = 5V ± 10%, V_{SS} = 0V, Ta = −20 ~ +75°C, unless otherwise noted.)

Symbol	Item	HD64180R1-4			HD64180R1-6			HD64180R1-8			Unit
		min	typ	max	min	typ	max	min	typ	max	
t_{cyc}	Clock Cycle Time	250	–	2000	162	–	2000	125	–	2000	ns
t_{CHW}	Clock "H" Pulse Width	110	–	–	65	–	–	50	–	–	ns
t_{CLW}	Clock "L" Pulse Width	110	–	–	65	–	–	50	–	–	ns
t_{cf}	Clock Fall Time	–	–	15	–	–	15	–	–	15	ns
t_{cr}	Clock Rise Time	–	–	15	–	–	15	–	–	15	ns
t_{AD}	Address Delay Time	–	–	110	–	–	90	–	–	80	ns
t_{AS}	Address Set-up Time ($\overline{ME}$ or $\overline{IOE}$ ↓)	50	–	–	30	–	–	20	–	–	ns
t_{MED1}	$\overline{ME}$ Delay Time 1	–	–	85	–	–	60	–	–	50	ns
t_{RDD1}	$\overline{RD}$ Delay Time 1	–	–	85	–	–	60	–	–	50	ns
t_{LD1}	$\overline{LIR}$ Delay Time 1	–	–	100	–	–	80	–	–	70*	ns
t_{AH}	Address Hold Time ($\overline{ME}$, $\overline{IOE}$, $\overline{RD}$ or $\overline{WR}$ ↑)	80	–	–	35	–	–	20	–	–	ns
t_{MED2}	$\overline{ME}$ Delay Time 2	–	–	85	–	–	60	–	–	50	ns
t_{RDD2}	$\overline{RD}$ Delay Time 2	–	–	85	–	–	60	–	–	50	ns
t_{LD2}	$\overline{LIR}$ Delay Time 2	–	–	100	–	–	80	–	–	70*	ns
t_{DRS}	Data Read Set-up Time	50	–	–	40	–	–	30	–	–	ns
t_{DRH}	Data Read Hold Time	0	–	–	0	–	–	0	–	–	ns
t_{STD1}	ST Delay Time 1	–	–	110	–	–	90	–	–	70	ns
t_{STD2}	ST Delay Time 2	–	–	110	–	–	90	–	–	70	ns
t_{WS}	$\overline{WAIT}$ Set-up Time	80	–	–	40	–	–	40	–	–	ns
t_{WH}	$\overline{WAIT}$ Hold Time	70	–	–	40	–	–	40	–	–	ns

(to be continued)

* For a loading capacitance of less than or equal to 40 picofarads and operating temperature from 0 to 50 degrees, substract 10 nanoseconds from the value given in the maximum columns.

Symbol	Item	HD64180R1-4			HD64180R1-6			HD64180R1-8			Unit
		min	typ	max	min	typ	max	min	typ	max	
t_{WDZ}	Write Data Floating Delay Time	–	–	100	–	–	95	–	–	70	ns
t_{WRD1}	$\overline{WR}$ Delay Time 1	–	–	90	–	–	65	–	–	60	ns
t_{WDD}	Write Data Delay Time	–	–	110	–	–	90	–	–	80	ns
t_{WDS}	Write Data Set-up Time ($\overline{WR}$ ↓)	60	–	–	40	–	–	20	–	–	ns
t_{WRD2}	$\overline{WR}$ Delay Time 2	–	–	90	–	–	80	–	–	60	ns
t_{WRP}	$\overline{WR}$ Pulse Width	280	–	–	170	–	–	130	–	–	ns
t_{WDH}	Write Data Hold Time ($\overline{WR}$ ↑)	60	–	–	40	–	–	15	–	–	ns
t_{IOD1}	$\overline{IOE}$ Delay Time 1	–	–	85	–	–	60	–	–	50	ns
t_{IOD2}	$\overline{IOE}$ Delay Time 2	–	–	85	–	–	60	–	–	50	ns
t_{IOD3}	$\overline{IOE}$ Delay Time 3 ($\overline{LIR}$ ↓)	540	–	–	340	–	–	250	–	–	ns
t_{INTS}	$\overline{INT}$ Set-up Time (ϕ ↓)	80	–	–	40	–	–	40	–	–	ns
t_{INTH}	$\overline{INT}$ Hold Time (ϕ ↓)	70	–	–	40	–	–	40	–	–	ns
t_{NMIW}	$\overline{NMI}$ Pulse Width	120	–	–	120	–	–	100	–	–	ns
t_{BRS}	$\overline{BUSREQ}$ Set-up Time (ϕ ↓)	80	–	–	40	–	–	40	–	–	ns
t_{BRH}	$\overline{BUSREQ}$ Hold Time (ϕ ↓)	70	–	–	40	–	–	40	–	–	ns
t_{BAD1}	$\overline{BUSACK}$ Delay Time 1	–	–	100	–	–	95	–	–	70	ns
t_{BAD2}	$\overline{BUSACK}$ Delay Time 2	–	–	100	–	–	95	–	–	70	ns
t_{BZD}	Bus Floating Delay Time	–	–	130	–	–	125	–	–	90	ns
t_{MEWH}	$\overline{ME}$ Pulse Width (HIGH)	200	–	–	110	–	–	90	–	–	ns
t_{MEWL}	$\overline{ME}$ Pulse Width (LOW)	210	–	–	125	–	–	100	–	–	ns

(to be continued)

(V_{CC} = 5V ±10% V_{SS} = 0V, Ta = −20 ~ +75°C, unless otherwise noted.)

Symbol	Item	HD64180R1-4			HD64180R1-6			HD64180R1-8			Unit
		min	typ	max	min	typ	max	min	typ	max	
t_{RFD1}	$\overline{REF}$ Delay Time 1	–	–	110	–	–	90	–	–	80	ns
t_{RFD2}	$\overline{REF}$ Delay Time 2	–	–	110	–	–	90	–	–	80	ns
t_{HAD1}	$\overline{HALT}$ Delay Time 1	–	–	110	–	–	90	–	–	80	ns
t_{HAD2}	$\overline{HALT}$ Delay Time 2	–	–	110	–	–	90	–	–	80	ns
t_{DRQS}	$\overline{DREQ}$i Set-up Time	80	–	–	40	–	–	40	–	–	ns
t_{DRQH}	$\overline{DREQ}$i Hold Time	70	–	–	40	–	–	40	–	–	ns
t_{TED1}	$\overline{TEND}$i Delay Time 1	–	–	85	–	–	70	–	–	60	ns
t_{TED2}	$\overline{TEND}$i Delay Time 2	–	–	85	–	–	70	–	–	60	ns
t_{ED1}	Enable Delay Time 1	–	–	100	–	–	95	–	–	70	ns
t_{ED2}	Enable Delay Time 2	–	–	100	–	–	95	–	–	70	ns
P_{WEH}	E Pulse Width (HIGH)	150	–	–	75	–	–	65	–	–	ns
P_{WEL}	E Pulse Width (LOW)	300	–	–	180	–	–	130	–	–	ns
t_{Er}	Enable Rise Time	–	–	25	–	–	20	–	–	20	ns
t_{Ef}	Enable Fall Time	–	–	25	–	–	20	–	–	20	ns
t_{TOD}	Timer Output Delay Time	–	–	300	–	–	300	–	–	200	ns
t_{STDI}	CSI/O Transmit Data Delay Time (Internal Clock Operation)	–	–	200	–	–	200	–	–	200	ns
t_{STDE}	CSI/O Transmit Data Delay Time (External Clock Operation)	–	–	7.5 tcyc +300	–	–	7.5 tcyc +300	–	–	7.5 tcyc +200	ns
t_{SRSI}	CSI/O Receive Data Set-up time (Internal Clock Operation)	1	–	–	1	–	–	1	–	–	tcyc
t_{SRHI}	CSI/O Receive Data Hold Time (Internal Clock Operation)	1	–	–	1	–	–	1	–	–	tcyc
t_{SRSE}	CSI/O Receive Data Set-up Time (External Clock Operation)	1	–	–	1	–	–	1	–	–	tcyc
t_{SRHE}	CSI/O Receive Data Hold Time (External Clock Operation)	1	–	–	1	–	–	1	–	–	tcyc
t_{RES}	$\overline{RESET}$ Set-up Time	120	–	–	120	–	–	100	–	–	ns
t_{REH}	$\overline{RESET}$ Hold Time	80	–	–	80	–	–	70	–	–	ns
t_{OSC}	Oscillator Stabilization Time	–	–	20	–	–	20	–	–	20	ms
t_{EXr}	External Clock Rise Time (EXTAL)	–	–	25	–	–	25	–	–	25	ns
t_{EXf}	External Clock Fall Time (EXTAL)	–	–	25	–	–	25	–	–	25	ns
t_{Rr}	$\overline{RESET}$ Rise Time	–	–	50	–	–	50	–	–	50	ms
t_{Rf}	$\overline{RESET}$ Fall Time	–	–	50	–	–	50	–	–	50	ms
t_{Ir}	Input Rise Time (except EXTAL, RESET)	–	–	100	–	–	100	–	–	100	ns
t_{If}	Input Fall Time (except EXTAL, RESET)	–	–	100	–	–	100	–	–	100	ns

■HD64180Z AC Characteristics

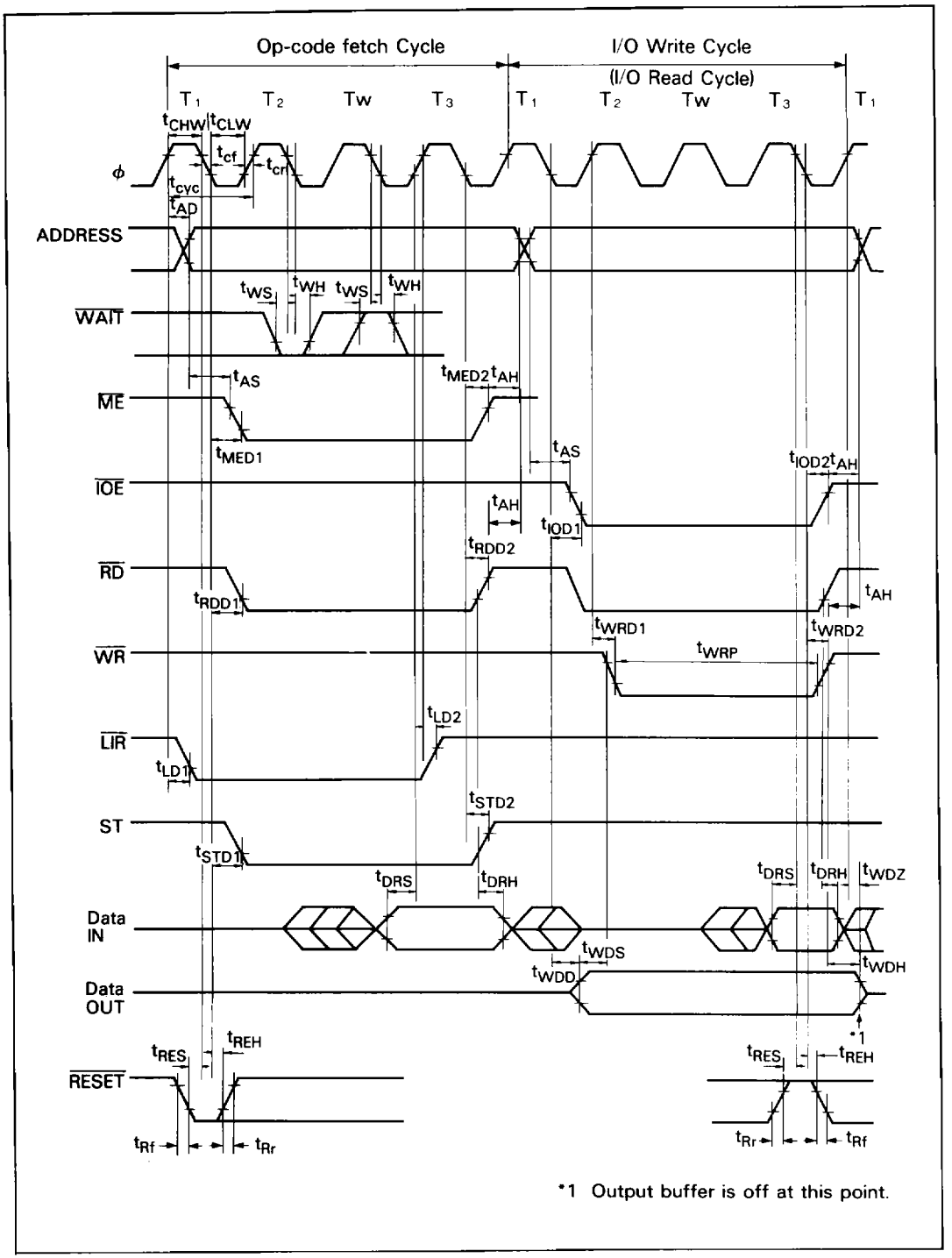
(V_{CC} = 5V ± 10%, V_{SS} = 0V, Ta = −20 to +75°C, unless otherwise noted.)

Symbol	Item		HD64180Z-4		HD64180Z-6		HD64180Z-8		Unit
			min	max	min	max	min	max	
t_{cyc}	Clock Cycle Time		250	2000	162	2000	125	2000	ns
t_{CHW}	Clock "H" Pulse Width		110	—	65	—	50	—	ns
t_{CLW}	Clock "L" Pulse Width		110	—	65	—	50	—	ns
t_{cf}	Clock Fall Time		—	15	—	15	—	15	ns
t_{cr}	Clock Rise Time		—	15	—	15	—	15	ns
t_{AD}	Address Delay Time		—	110	—	90	—	80	ns
t_{AS}	Address Set-up Time ($\overline{ME}$ or $\overline{IOE}$ ↓)		50	—	30	—	20	—	ns
t_{MED1}	$\overline{ME}$ Delay Time 1		—	85	—	60	—	50	ns
t_{RDD1}	$\overline{RD}$ Delay Time 1	$\overline{IOC}$= 1	—	85	—	60	—	50	ns
		$\overline{IOC}$= 0	—	85	—	65	—	60	
t_{LD1}	$\overline{LIR}$ Delay Time 1		—	100	—	80	—	70*	ns
t_{AH}	Address Hold Time 1 ($\overline{ME}$, $\overline{IOE}$, $\overline{RD}$ or $\overline{WR}$ ↑)		80	—	35	—	20	—	ns
t_{MED2}	$\overline{ME}$ Delay Time 2		—	85	—	60	—	50	ns
t_{RDD2}	$\overline{RD}$ Delay Time 2		—	85	—	60	—	50	ns
t_{LD2}	$\overline{LIR}$ Delay Time 2		—	100	—	80	—	70*	ns
t_{DRS}	Data Read Set-up Time		50	—	40	—	30	—	ns
t_{DRH}	Data Read Hold Time		0	—	0	—	0	—	ns
t_{STD1}	ST Delay Time 1		—	110	—	90	—	70	ns
t_{STD2}	ST Delay Time 2		—	110	—	90	—	70	ns
t_{WS}	$\overline{WAIT}$ Set-up Time		80	—	40	—	40	—	ns
t_{WH}	$\overline{WAIT}$ Hold Time		70	—	40	—	40	—	ns
t_{WDZ}	Write Data Floating Delay Time		—	100	—	95	—	70	ns
t_{WRD1}	$\overline{WR}$ Delay Time 1		—	90	—	65	—	60	ns
t_{WDD}	Write Data Delay Time		—	110	—	90	—	80	ns
t_{WDS}	Write Data Set-up Time ($\overline{WR}$ ↓)		60	—	40	—	20	—	ns
t_{WRD2}	$\overline{WR}$ Delay Time 2		—	90	—	80	—	60	ns
t_{WRP}	$\overline{WR}$ Pulse Width		280	—	170	—	130	—	ns

* For a loading capacitance of less than or equal to 40 picofarads and operating temperature from 0 to 50 degrees, substract 10 nanoseconds from the value given in the maximum columns.

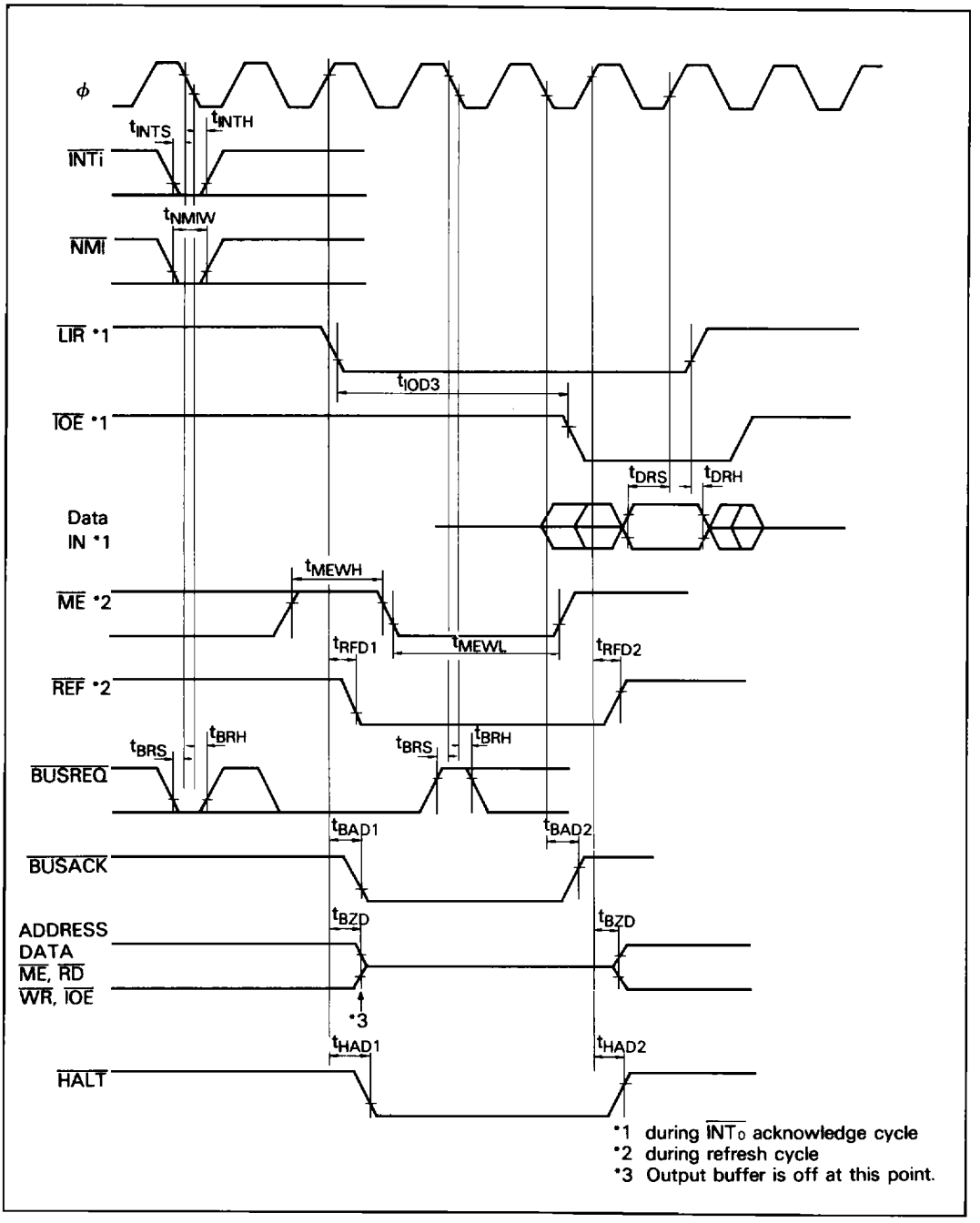
Symbol	Item		HD64180Z-4		HD64180Z-6		HD64180Z-8		Unit
			min	max	min	max	min	max	
t_{WDH}	Write Data Hold Time ($\overline{WR}$ ↑)		60	—	40	—	15	—	ns
t_{IOD1}	$\overline{IOE}$ Delay Time 1	$\overline{IOC}$= 1	—	85	—	60	—	50	ns
		$\overline{IOC}$= 0	—	85	—	65	—	60	
t_{IOD2}	$\overline{IOE}$ Delay Time 2		—	85	—	60	—	50	ns
t_{IOD3}	$\overline{IOE}$ Delay Time 3 ($\overline{LIR}$ ↓)		540	—	340	—	250	—	ns
t_{INTS}	$\overline{INT}$ Set-up Time (ϕ ↓)		80	—	40	—	40	—	ns
t_{INTH}	$\overline{INT}$ Hold Time (ϕ ↓)		70	—	40	—	40	—	ns
t_{NMIW}	$\overline{NMI}$ Pulse Width		120	—	120	—	100	—	ns
t_{BRS}	$\overline{BUSREQ}$ Set-up Time (ϕ ↓)		80	—	40	—	40	—	ns
t_{BRH}	$\overline{BUSREQ}$ Hold Time (ϕ ↓)		70	—	40	—	40	—	ns
t_{BAD1}	$\overline{BUSACK}$ Delay Time 1		—	100	—	95	—	70	ns
t_{BAD2}	$\overline{BUSACK}$ Delay Time 2		—	100	—	95	—	70	ns
t_{BZD}	Bus Floating Delay Time		—	130	—	125	—	90	ns
t_{MEWH}	$\overline{ME}$ Pulse Width (HIGH)		200	—	110	—	90	—	ns
t_{MEWL}	$\overline{ME}$ Pulse Width (LOW)		210	—	125	—	100	—	ns
t_{RFD1}	$\overline{REF}$ Delay Time 1		—	110	—	90	—	80	ns
t_{RFD2}	$\overline{REF}$ Delay Time 2		—	110	—	90	—	80	ns
t_{HAD1}	$\overline{HALT}$ Delay Time 1		—	110	—	90	—	80	ns
t_{HAD2}	$\overline{HALT}$ Delay Time 2		—	110	—	90	—	80	ns
t_{DRQS}	$\overline{DREQi}$ Set-up Time		80	—	40	—	40	—	ns
t_{DRQH}	$\overline{DREQi}$ Hold Time		70	—	40	—	40	—	ns
t_{TED1}	$\overline{TENDi}$ Delay Time 1		—	85	—	70	—	60	ns
t_{TED2}	$\overline{TENDi}$ Delay Time 2		—	85	—	70	—	60	ns
t_{ED1}	Enable Delay Time 1		—	100	—	95	—	70	ns
t_{ED2}	Enable Delay Time 2		—	100	—	95	—	70	ns
P_{WEH}	E Pulse Width (HIGH)		150	—	75	—	65	—	ns
P_{WEL}	E Pulse Width (LOW)		300	—	180	—	130	—	ns

Symbol	Item	HD64180Z-4		HD64180Z-6		HD64180Z-8		Unit
		min	max	min	max	min	max	
t_{Er}	Enable Rise Time	—	25	—	20	—	20	ns
t_{Ef}	Enable Fall Time	—	25	—	20	—	20	ns
t_{TOD}	Timer Output Delay Time	—	300	—	300	—	200	ns
t_{STDI}	CSI/O Transmit Data Delay Time (Internal Clock Operation)	—	200	—	200	—	200	ns
t_{STDE}	CSI/O Transmit Data Delay Time (External Clock Operation)	—	7.5tcyc +300	—	7.5tcyc +300	—	7.5tcyc +200	ns
t_{SRSI}	CSI/O Receive Data Set-up Time (Internal Clock Operation)	1	—	1	—	1	—	tcyc
t_{SRHI}	CSI/O Receive Data Hold Time (Internal Clock Operation)	1	—	1	—	1	—	tcyc
t_{SRSE}	CSI/O Receive Data Set-up Time (External Clock Operation)	1	—	1	—	1	—	tcyc
t_{SRHE}	CSI/O Receive Data Hold Time (External Clock Operation)	1	—	1	—	1	—	tcyc
t_{RES}	$\overline{\text{RESET}}$ Set-up Time	120	—	120	—	100	—	ns
t_{REH}	$\overline{\text{RESET}}$ Hold Time	80	—	80	—	70	—	ns
t_{OSC}	Oscillator Stabilization Time	—	20	—	20	—	20	ms
t_{EXr}	External Clock Rise Time (EXTAL)	—	25	—	25	—	25	ns
t_{EXf}	External Clock Fall Time (EXTAL)	—	25	—	25	—	25	ns
t_{Rr}	$\overline{\text{RESET}}$ Rise Time	—	50	—	50	—	50	ms
t_{Rf}	$\overline{\text{RESET}}$ Fall Time	—	50	—	50	—	50	ms
t_{Ir}	Input Rise Time (except EXTAL, $\overline{\text{RESET}}$)	—	100	—	100	—	100	ns
t_{If}	Input Fall Time (except EXTAL, $\overline{\text{RESET}}$)	—	100	—	100	—	100	ns

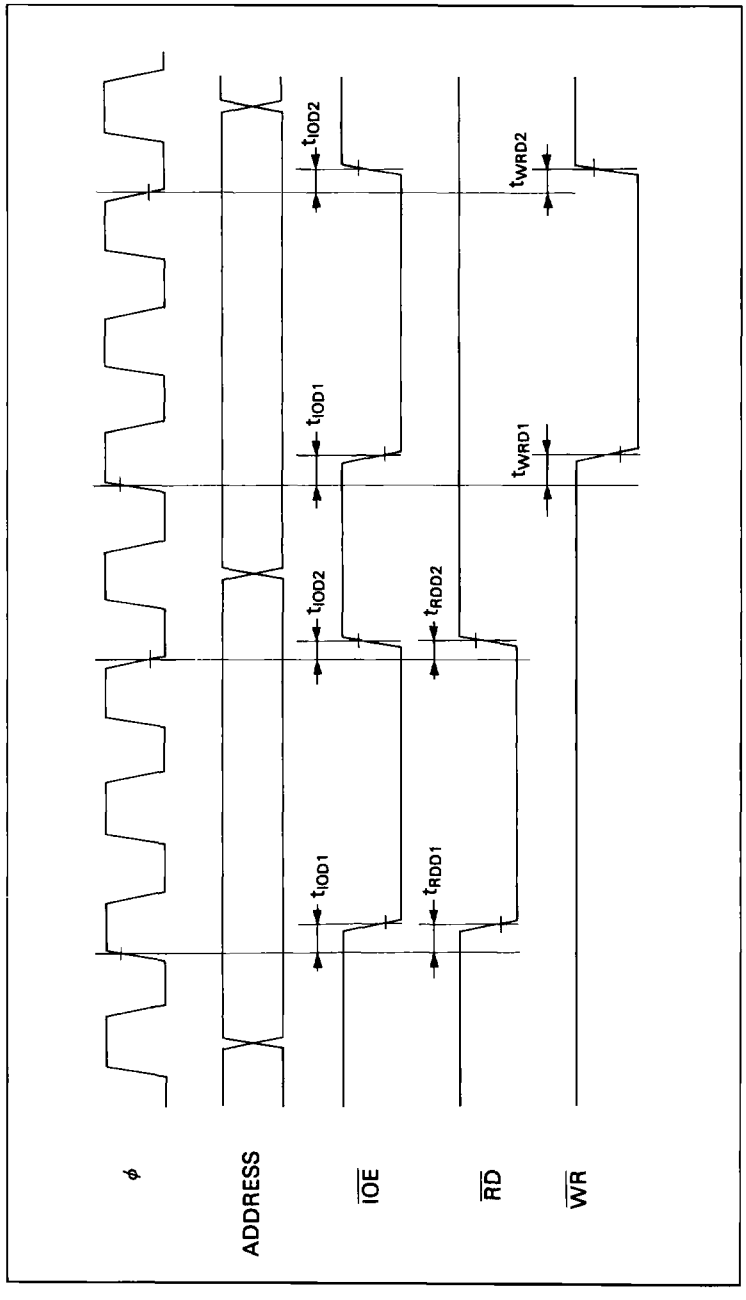


*1 Output buffer is off at this point.

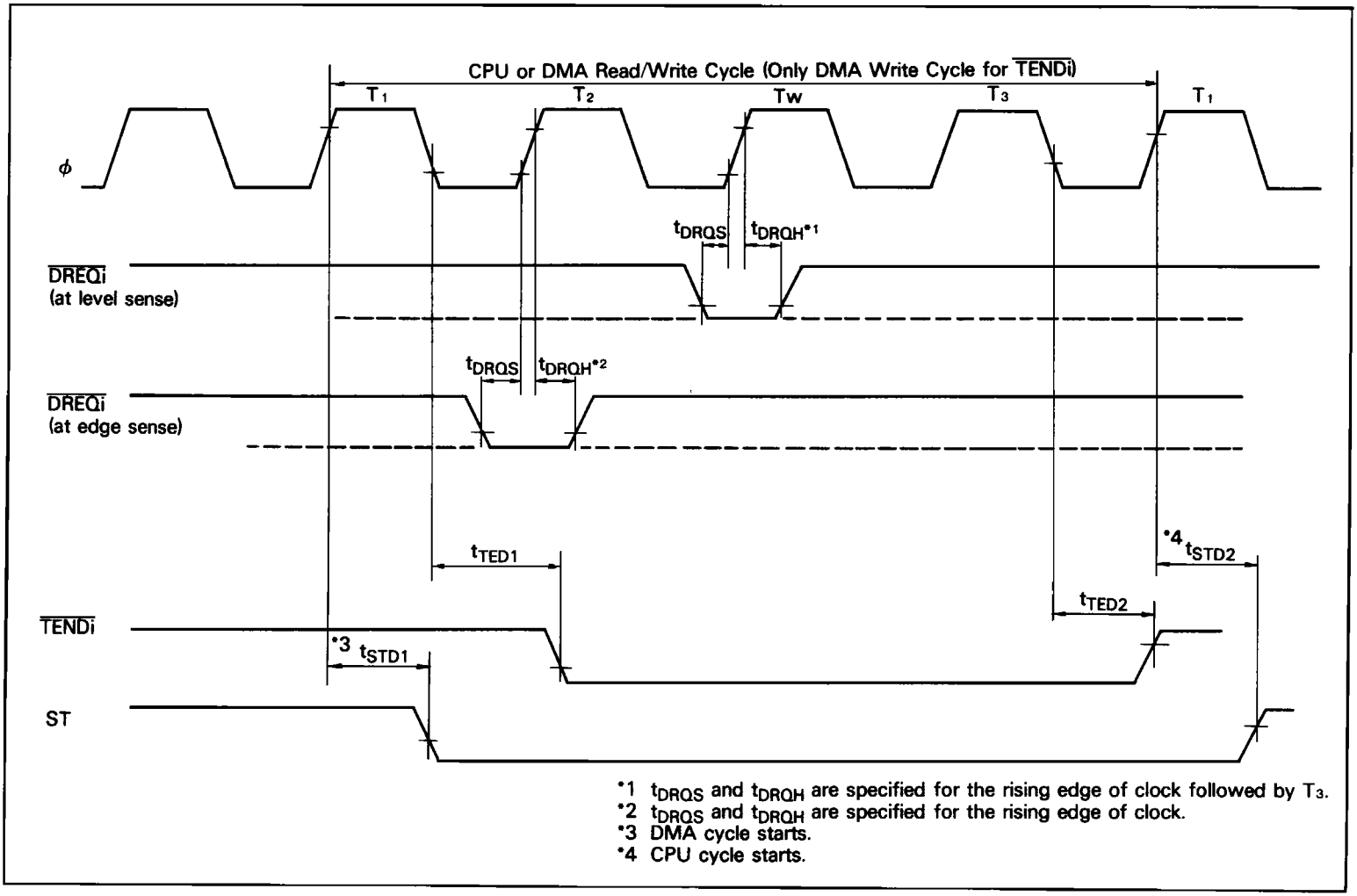
CPU Timing { **Op-code fetch Cycle** / **I/O Write Cycle** / **I/O Read Cycle** }



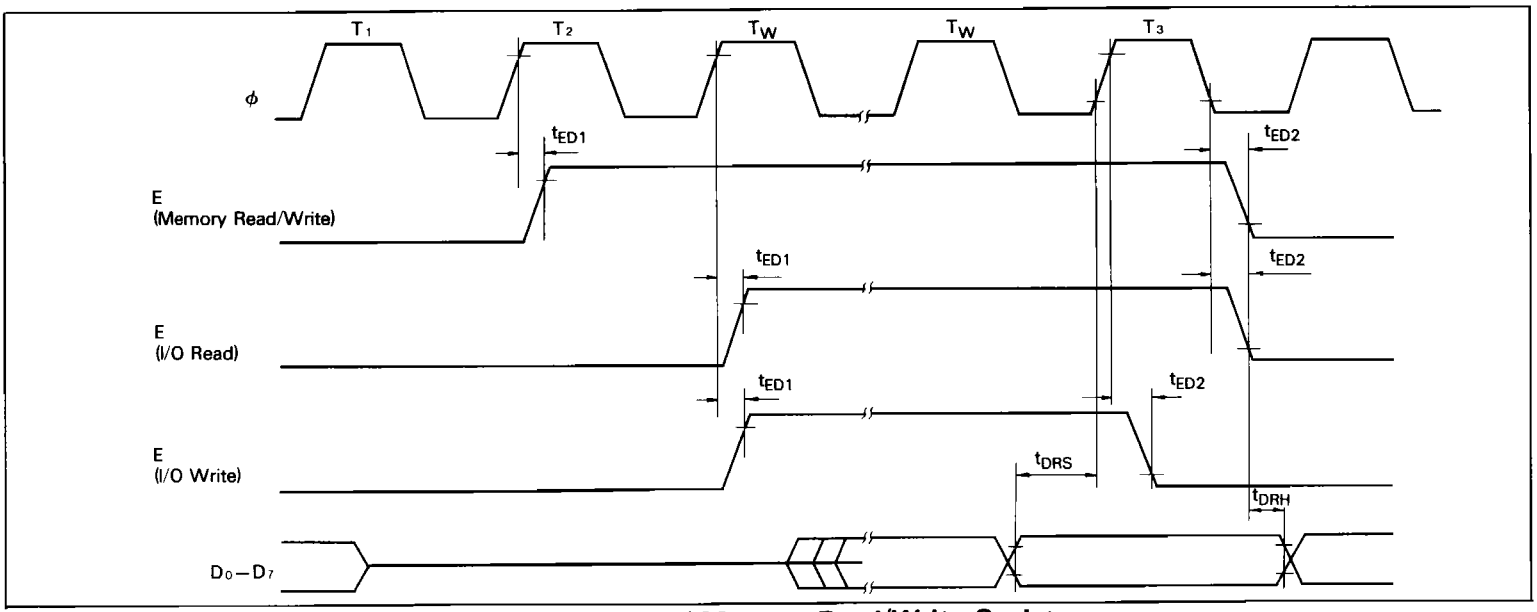
CPU Timing { **INT0 Acknowledge cycle**
Refresh Cycle
BUS RELEASE Mode
HALT Mode
SLEEP Mode
SYSTEM STOP Mode }



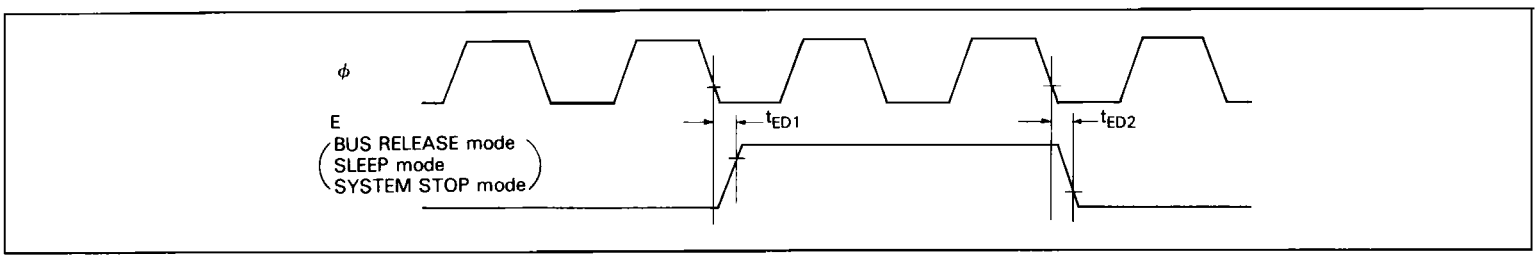
CPU Timing ($\overline{IOC}$=0)



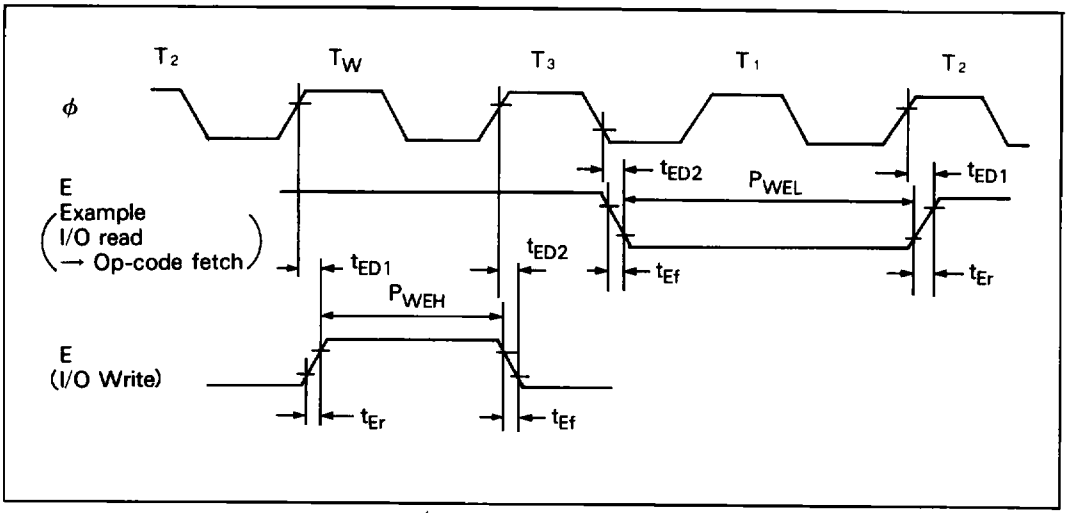
DMA Control Signals



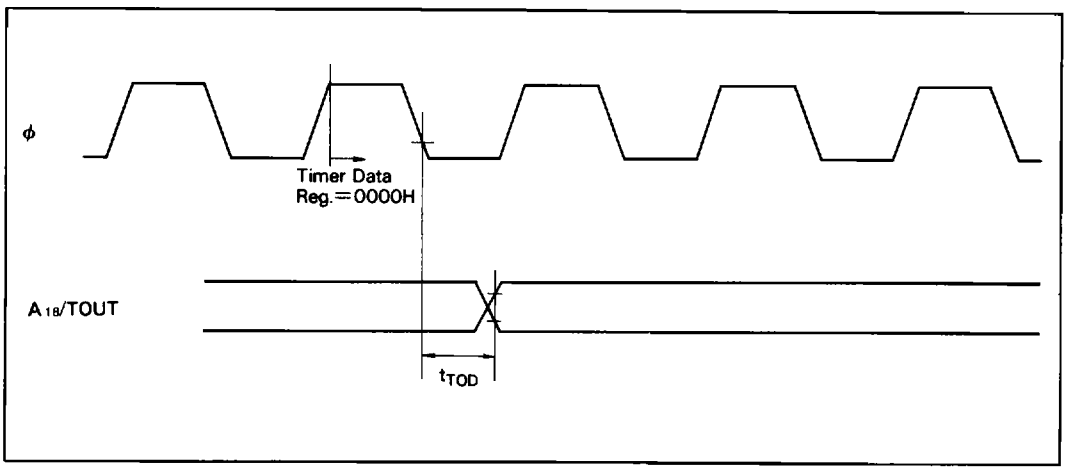
E Clock Timing { **Memory Read/Write Cycle** / **I/O Read/Write Cycle** }



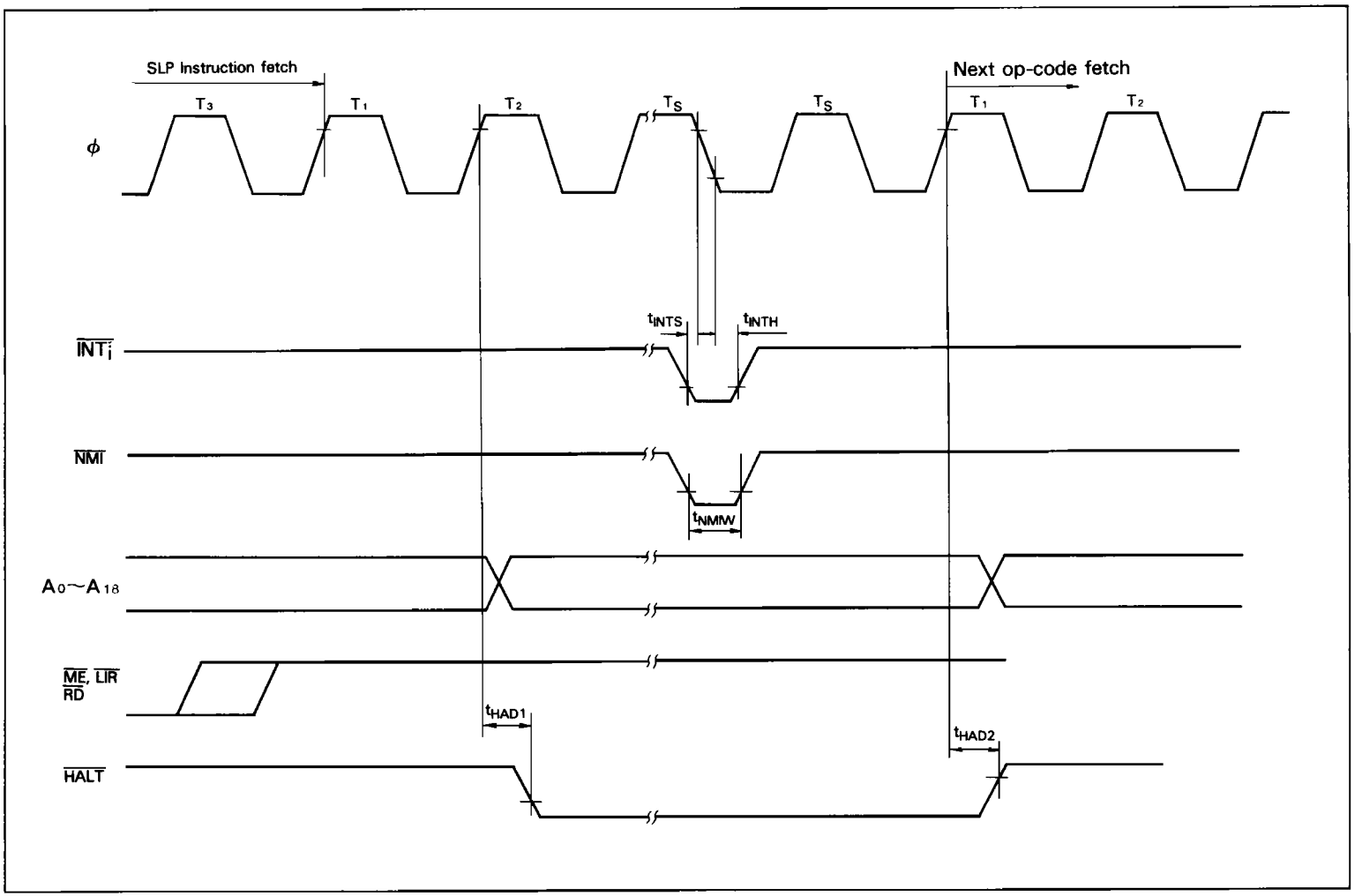
E Clock Timing { **BUS RELEASE Mode** / **SLEEP Mode** / **SYSTEM STOP Mode** }



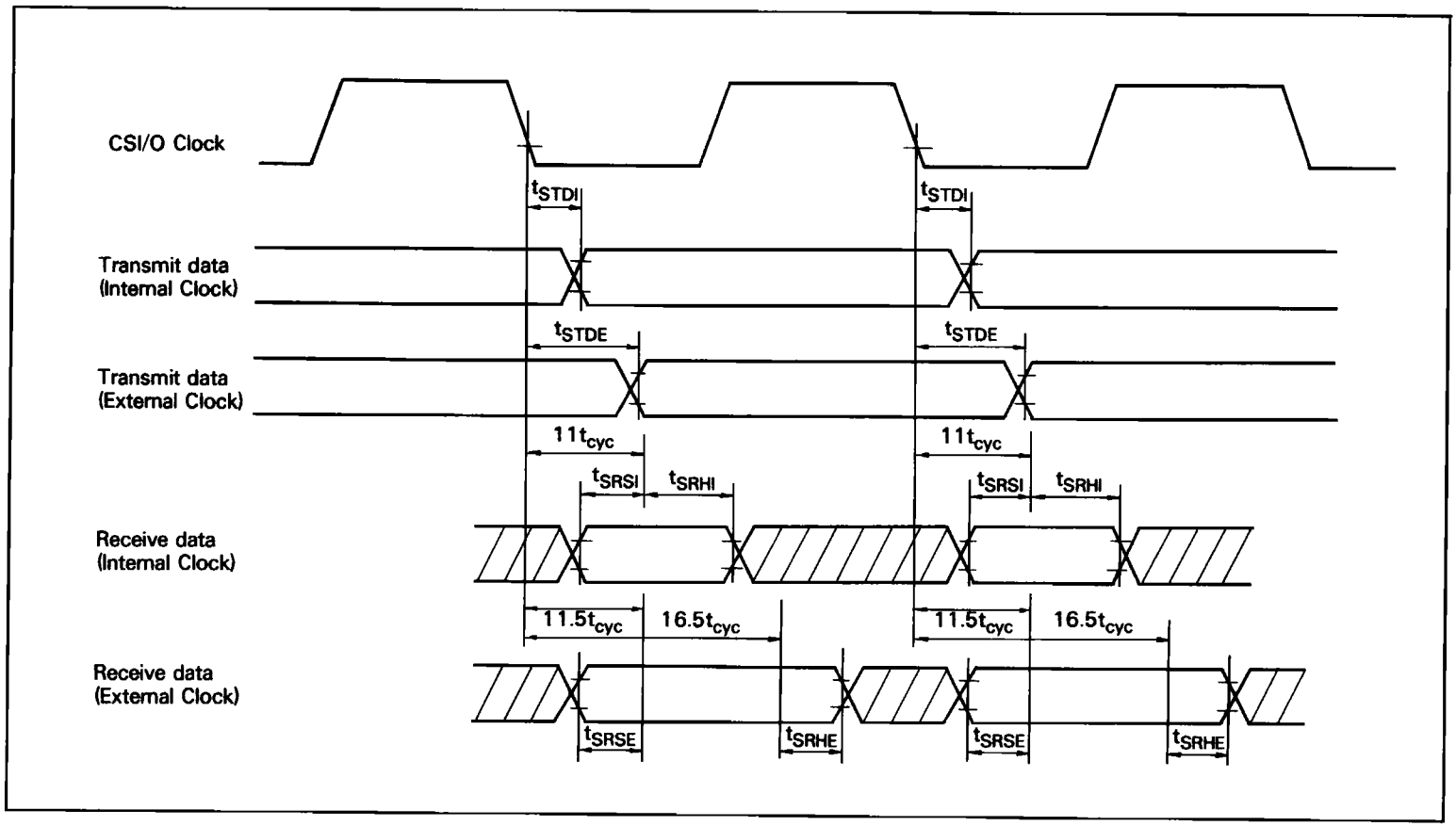
E Clock Timing (**Minimum timing example of P_{WEL} and P_{WEH}**)



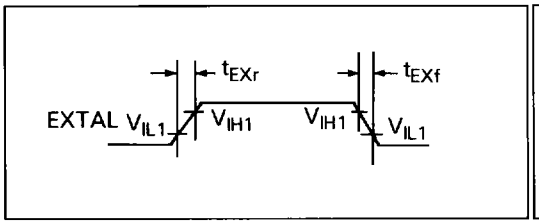
Timer Output Timing



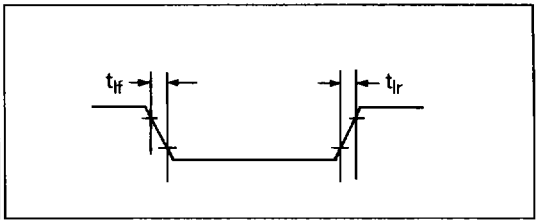
SLP Execution Cycle



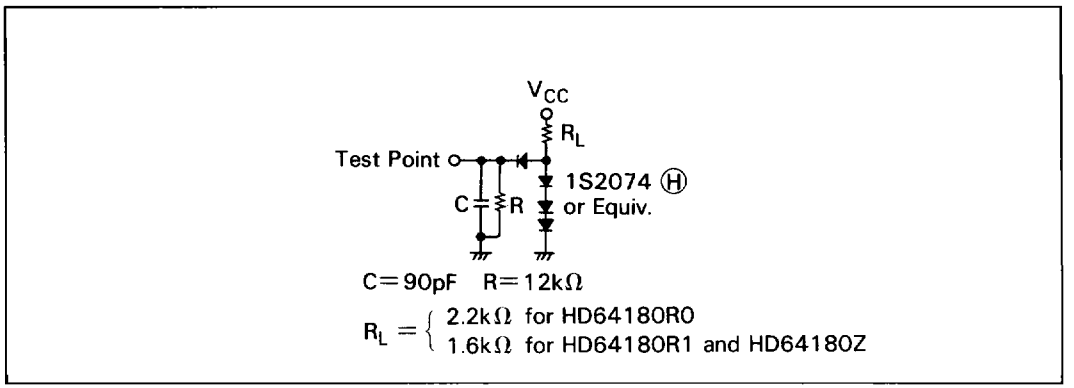
CSI/O Receive/Transmit Timing



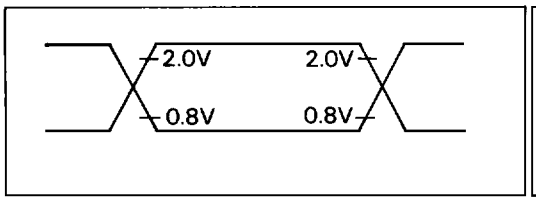
External Clock Rise Time and Fall Time



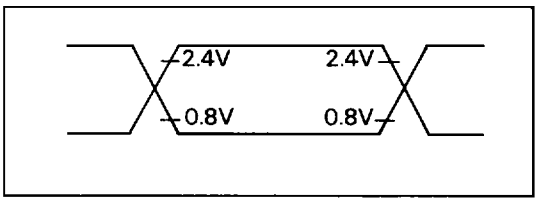
Input Rise Time and Fall Time (Except EXTAL, $\overline{\text{RESET}}$)



Bus Timing Test Load (TTL Load)



Reference Level (Input)



Reference Level (Output)