HYUNDAI

8Mx72 bits
PC100 SDRAM SO DIMM

based on 8Mx8 SDRAM with LVTTL, 4 banks & 4K Refresh

HYM7V75A801B Z-Series

Preliminary

DESCRIPTION

The Hyundai HYM7V75A801B Z-Series are 4Mx72bits ECC Synchronous DRAM Modules composed of nine 8Mx8bit CMOS Synchronous DRAMs in 400mil 54pin TSOP-II package and 2Kbit EEPROM in 8pin TSSOP package on a 144pin glass-epoxy printed circuit board. A 0.22uF and a 0.0022uF decoupling capacitors per each SDRAM are mounted on the PCB.

The HYM7V75A801B Z-Series are Small Outline Dual In-line Memory Modules suitable for easy interchange and addition of 64Mbytes memory. The HYM7V75A801B Z-Series are offering fully synchronous operation referenced to a positive edge of the clock. All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high bandwidth.

FEATURES

- 144pin SDRAM SO DIMM
- Serial Presence Detect with EEPROM
- 1.50" (38.10mm) Height PCB with Double Sided components
- Single 3.3 ± 0.3V power supply
- All devices pins are compatible with LVTTL interface
- Data mask function by DQM
- SDRAM devices : internal four banks operation
- Auto refresh and self refresh
- 4096 refresh cycles / 64ms
- Programmable Burst Length and Burst Type

  -. 1, 2, 4, 8, or Full Page for Sequential Burst
  -. 1, 2, 4 or 8 for Interleave Burst
- Programmable /CAS Latency : 2, 3 Clocks

ORDERING INFORMATION

PART NO.	MAX. FREQUENCY	INTERNAL BANK	REF.	POWER	SDRAM PACKAGE	PLATING
HYM7V75A801BTZG-75	133MHz	4 Banks	4K	Normal	TSOP-II	Gold
HYM7V75A801BTZG-8	125MHz					
HYM7V75A801BTZG-10P	100MHz					
HYM7V75A801BTZG-10S	100MHz					
HYM7V75A801BLTZG-75	133MHz			Low Power		
HYM7V75A801BLTZG-8	125MHz					
HYM7V75A801BLTZG-10P	100MHz					
HYM7V75A801BLTZG-10S	100MHz					

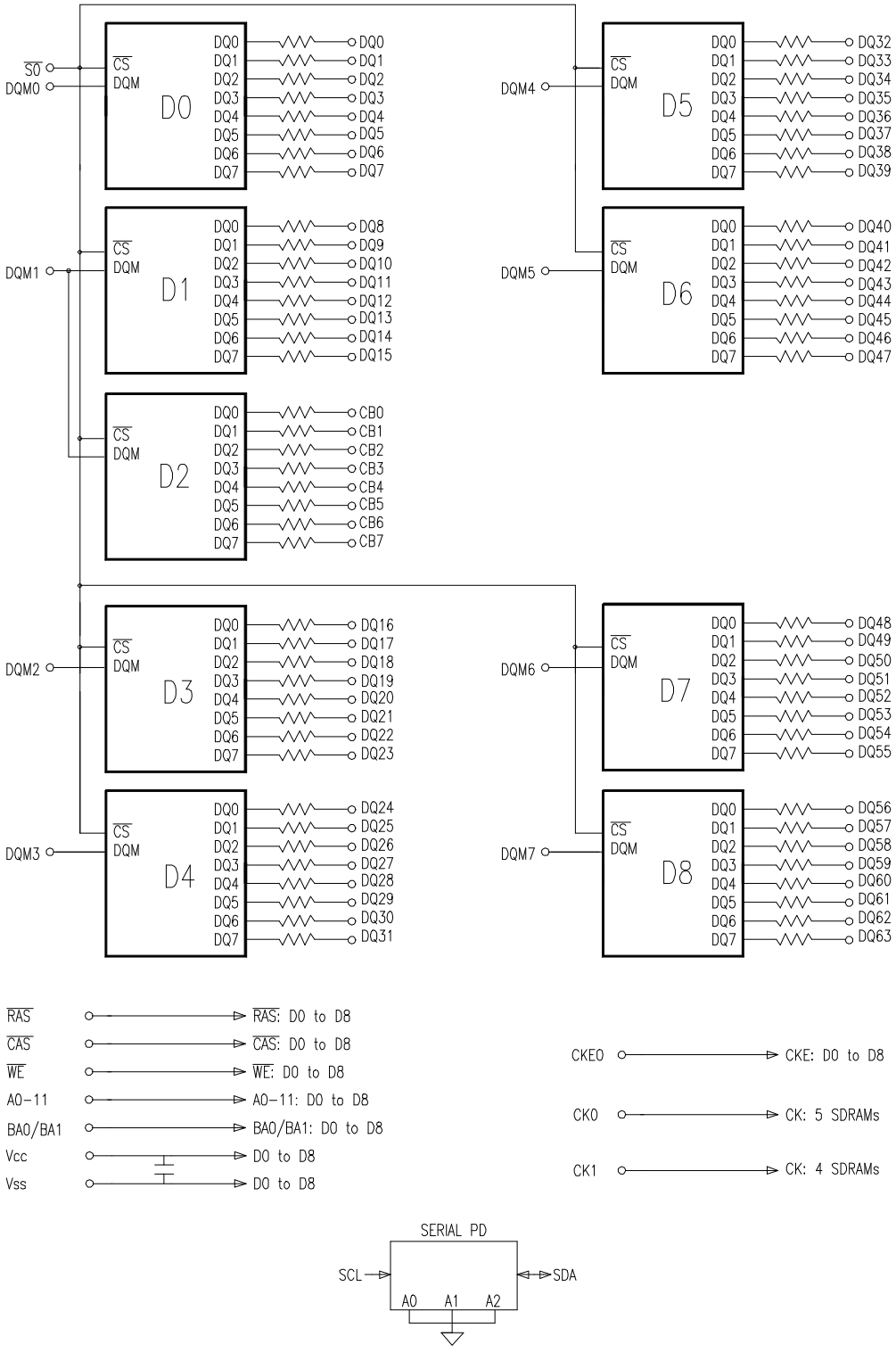
PIN DESCRIPTION

PIN NAME	DESCRIPTION	
CK0, CK1	Clock Inputs	The System Clock Input. All other inputs are registered to the SDRAM on the rising edge of CLK.
CKE0	Clock Enable	Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh.
/S0	Chip Select	Enables or disables all inputs except CK, CKE and DQM.
BA0, BA1	SDRAM Bank Address	Select bank to be activated during /RAS activity. Select bank to be read/written during /CAS activity
A0~A11	Address Inputs	Row address : RA0~RA11, Column address : CA0~CA7 Auto-precharge flag : A10
/RAS	Row Address Strobe	/RAS define the operation. Refer to the function truth table for details.
/CAS	Column Address Strobe	/CAS define the operation. Refer to the function truth table for details.
/WE	Write Enable	/WE define the operation. Refer to the function truth table for details.
DQM0~DQM7	Data Input/Output Mask	Controls output buffers in read mode and masks input data in write mode.
DQ0~DQ63	Data Input/Output	Multiplexed data input/output pins
CB0~CB7	ECC Data Input/Output	Error Checking and Correction Bits
VCC	Power Supply (3.3V)	Power supply for internal circuits and input/output buffers
VSS	Ground	Ground
SCL	SPD Clock Input	Serial Presence Detect Clock Input
SDA	SPD Data Input/Output	Serial Presence Detect Data input/output
NC	No Connect	No Connect or Don't Use

PIN ASSIGNMENTS

FRONT SIDE		BACK SIDE		FRONT SIDE		BACK SIDE	
PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME
1	VSS	2	VSS	71	NC	72	NC
3	DQ0	4	DQ32	73	NC	74	CK1
5	DQ1	6	DQ33	75	VSS	76	VSS
7	DQ2	8	DQ34	77	CB2	78	CB6
9	DQ3	10	DQ35	79	CB3	80	CB7
11	VCC	12	VCC	81	VCC	82	VCC
13	DQ4	14	DQ36	83	DQ16	84	DQ48
15	DQ5	16	DQ37	85	DQ17	86	DQ49
17	DQ6	18	DQ38	87	DQ18	88	DQ50
19	DQ7	20	DQ39	89	DQ19	90	DQ51
21	VSS	22	VSS	91	VSS	92	VSS
23	DQM0	24	DQM4	93	DQ20	94	DQ52
25	DQM1	26	DQM5	95	DQ21	96	DQ53
27	VCC	28	VCC	97	DQ22	98	DQ54
29	A0	30	A3	99	DQ23	100	DQ55
31	A1	32	A4	101	VCC	102	VCC
33	A2	34	A5	103	A6	104	A7
35	VSS	36	VSS	105	A8	106	BA0
37	DQ8	38	DQ40	107	VSS	108	VSS
39	DQ9	40	DQ41	109	A9	110	BA1
41	DQ10	42	DQ42	111	A10/AP	112	A11
43	DQ11	44	DQ43	113	VCC	114	VCC
45	VCC	46	VCC	115	DQM2	116	DQM6
47	DQ12	48	DQ44	117	DQM3	118	DQM7
49	DQ13	50	DQ45	119	VSS	120	VSS
51	DQ14	52	DQ46	121	DQ24	122	DQ56
53	DQ15	54	DQ47	123	DQ25	124	DQ57
55	VSS	56	VSS	125	DQ26	126	DQ58
57	CB0	58	CB4	127	DQ27	128	DQ59
59	CB1	60	CB5	129	VCC	130	VCC
Voltage Key				131	DQ28	132	DQ60
				133	DQ29	134	DQ61
61	CK0	62	CKE0	135	DQ30	136	DQ62
63	VCC	64	VCC	137	DQ31	138	DQ63
65	/RAS	66	/CAS	139	VSS	140	VSS
67	/WE	68	NC	141	SDA	142	SCL
69	/S0	70	NC	143	VCC	144	VCC

BLOCK DIAGRAM



Note : The serial resistor values of DQs are 10 Ohms.

SERIAL PRESENCE DETECT

BYTE NUMBER	FUNCTION DESCRIBED	FUNCTION -75	-8	-10P	-10S	VALUE -75	-8	-10P	-10S	NOTE
BYTE0	# of Bytes Written into Serial Memory at Module Manufacturer	128 Bytes				80h				
BYTE1	Total # of Bytes of SPD Memory Device	256 Bytes				08h				
BYTE2	Fundamental Memory Type	SDRAM				04h				
BYTE3	# of Row Addresses on This Assembly	12				0Ch				1
BYTE4	# of Column Addresses on This Assembly	9				09h				
BYTE5	# of Module Banks on This Assembly	1 Bank				01h				
BYTE6	Data Width of This Assembly	72 Bits				48h				
BYTE7	Data Width of This Assembly (Continued)	-				00h				
BYTE8	Voltage Interface Standard of This Assembly	LVTTL				01h				
BYTE9	SDRAM Cycle Time @ /CAS Latency=3	7.5ns	8ns	10ns	10ns	75h	80h	A0h	A0h	
BYTE10	Access Time from Clock @ /CAS Latency=3	5.4ns	6ns	6ns	6ns	54h	60h	60h	60h	
BYTE11	DIMM Configuration Type	ECC				02h				
BYTE12	Refresh Rate/Type	15.625µs / Self Refresh Supported				80h				
BYTE13	Primary SDRAM Width	x8				08h				
BYTE14	Error Checking SDRAM Width	x8				08h				
BYTE15	Minimum Clock Delay Back to Back Random Column Address	tCCD = 1 CLK				01h				
BYTE16	Burst Lengths Supported	1,2,4,8,Full Page				8Fh				2
BYTE17	# of Banks on Each SDRAM Device	4 Banks				04h				
BYTE18	SDRAM Device Attributes, CAS # Latency	/CAS Latency=2,3				06h				
BYTE19	SDRAM Device Attributes, CS # Latency	/CS Latency=0				01h				
BYTE20	SDRAM Device Attributes, Write Latency	/WE Latency=0				01h				
BYTE21	SDRAM Module Attributes	Neither Buffered nor Registered				00h				
BYTE22	SDRAM Device Attributes, General	+/-10% voltage tolerance, Burst Read Single bit Write, Precharge All, Auto Precharge, Early RAS Precharge				0Eh				
BYTE23	SDRAM Cycle Time @ /CAS Latency=2	10ns	10ns	10ns	12ns	A0h	A0h	A0h	C0h	
BYTE24	Access Time from Clock @ /CAS Latency=2	6ns	6ns	6ns	6ns	60h	60h	60h	60h	
BYTE25	SDRAM Cycle Time @ /CAS Latency=1	-	-	-	-	00h	00h	00h	00h	
BYTE26	Access Time from Clock @ /CAS Latency=1	-	-	-	-	00h	00h	00h	00h	
BYTE27	Minimum Row Precharge Time (tRP)	23ns (22.5)	20ns	20ns	20ns	17h	14h	14h	14h	
BYTE28	Minimum Row Active to Row Active Delay (tRRD)	15ns	16ns	20ns	20ns	0Fh	10h	14h	14h	
BYTE29	Minimum /RAS to /CAS Delay (tRCD)	23ns (22.5)	20ns	20ns	20ns	17h	14h	14h	14h	
BYTE30	Minimum /RAS Pulse width (tRAS)	45ns	48ns	50ns	50ns	2Dh	30h	32h	32h	
BYTE31	Module Bank Density	64MB				10h				
BYTE32	Command and Address Signal Input Setup Time	1.5ns	2ns	2ns	2ns	15h	20h	20h	20h	
BYTE33	Command and Address Signal Input Hold Time	0.8ns	1ns	1ns	1ns	08h	10h	10h	10h	
BYTE34	Data Signal Input Setup Time	1.5ns	2ns	2ns	2ns	15h	20h	20h	20h	
BYTE35	Data Signal Input Hold Time	0.8ns	1ns	1ns	1ns	08h	10h	10h	10h	
BYTE36 –61	Superset Information (may be used in future)	-				00h				
BYTE62	SPD Revision	Intel SPD 1.2A				12h				3, 8
BYTE63	Checksum for Bytes 0~62	-				B6h	F1h	17h	37h	
BYTE64	Manufacturer JEDEC ID Code	Hyundai JEDEC ID				ADh				
BYTE65 ~71	....Manufacturer JEDEC ID Code	Unused				FFh				
BYTE72	Manufacturing Location	HEI (Korea) HEA (United States) HEU (Europe)				01h 02h 03h				

Continued

BYTE NUMBER	FUNCTION DESCRIBED	FUNCTION -75	-8	-10P	-10S	VALUE -75	-8	-10P	-10S	NOTE
BYTE73	Manufacturer's Part Number (Component)	7 (SDRAM)				37h				4, 5
BYTE74	Manufacturer's Part Number (Voltage Interface)	V (3.3V, LVTTL)				56h				4, 5
BYTE75	Manufacturer's Part Number (Data Width)	7				37h				4, 5
BYTE76	....Manufacturer's Part Number (Data Width)	5				35h				4, 5
BYTE77	Manufacturer's Part Number (ECC)	A				41h				4, 5
BYTE78	Manufacturer's Part Number (Memory Depth)	8				38h				4, 5
BYTE79	Manufacturer's Part Number (Refresh)	0 (4K Refresh)				30h				4, 5
BYTE80	Manufacturer's Part Number (Internal Banks)	1 (4 Banks)				31h				4, 5
BYTE81	Manufacturer's Part Number (Generation)	B				42h				4, 5
BYTE82	Manufacturer's Part Number (Package Type)	T (TSOPII)				54h				4, 5
BYTE83	Manufacturer's Part Number (Module Type)	Z (x8 based SO DIMM)				5Ah				4, 5
BYTE84	Manufacturer's Part Number (Plating Type)	G (Gold)				47h				4, 5
BYTE85	Manufacturer's Part Number (Hyphen)	- (Hyphen)				2Dh				4, 5
BYTE86	Manufacturer's Part Number (Min. Cycle Time)	7	8	1	1	37h	38h	31h	31h	4, 5
BYTE87	....Manufacturer's Part Number (Min. Cycle Time)	5	Blank	0	0	35h	20h	30h	30h	4, 5
BYTE88	....Manufacturer's Part Number (Min. Cycle Time)	Blank	Blank	P	S	20h	20h	50h	53h	4, 5
BYTE89 ~90	Manufacturer's Part Number	Blanks				20h				4, 5
BYTE91	Revision Code (for Component)	Process Code				-				4, 6
BYTE92	....Revision Code (for PCB)	Process Code				-				4, 6
BYTE93	Manufacturing Date	Work Week				-				3, 6
BYTE94	....Manufacturing Date	Year				-				3, 6
BYTE95 ~98	Assembly Serial Number	Serial Number				-				6
BYTE99 ~125	Manufacturer Specific Data (may be used in future)	None				00h				
BYTE126	System Frequency Support	100MHz				64h				8
BYTE127	Intel Specification Details for 100MHz Support	Refer to Note7				C7h	C7h	C7h	C5h	7, 8
BYTE128 ~256	Unused Storage Locations	-				00h				

Note: 1. The bank address is excluded.
2. 1,2,4,8 for Interleave Burst Type
3. BCD adopted.
4. ASCII adopted.
5. Basically HYUNDAI writes Part No. except for ` HYM ` in Byte 73-90 to use the limited 18 bytes from byte 73 to 90 efficiently.
6. Not fixed but dependent.
7. CLK0, CK1 connected on the DIMM, TBD junction temp, CL2(3) support, Intel defined Concurrent Auto Precharge support
8. Refer to Intel SPD Specification Rev.1.2A.

BYTE82~89 for L-Part (HYM7V75A801BLTZG)

BYTE NUMBER	FUNCTION DESCRIBED	FUNCTION -75	-8	-10P	-10S	VALUE -75	-8	-10P	-10S	NOTE
BYTE82	Manufacturer's Part Number (Power)	L (Low Power)				4Ch				4, 5
BYTE83	Manufacturer's Part Number (Package Type)	T (TSOPII)				54h				4, 5
BYTE84	Manufacturer's Part Number (Module Type)	Z (x8 based SO DIMM)				5Ah				4, 5
BYTE85	Manufacturer's Part Number (Plating Type)	G (Gold)				47h				4, 5
BYTE86	Manufacturer's Part Number (Hyphen)	- (Hyphen)				2Dh				4, 5
BYTE87	Manufacturer's Part Number (Min. Cycle Time)	7	8	1	1	37h	38h	31h	31h	4, 5
BYTE88	....Manufacturer's Part Number (Min. Cycle Time)	5	Blank	0	0	35h	20h	30h	30h	4, 5
BYTE89	....Manufacturer's Part Number (Min. Cycle Time)	Blank	Blank	P	S	20h	20h	50h	53h	4, 5

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Ambient Temperature	TA	0 ~ 70	°C
Storage Temperature	TSTG	-55 ~ 125	°C
Voltage on any Pin relative to VSS	VIN, VOUT	-1.0 ~ 4.6	V
Voltage on VDD relative to VSS	VDD, VDDQ	-1.0 ~ 4.6	V
Short Circuit Output Current	IOS	50	MA
Power Dissipation	PD	9	W
Soldering Temperature · Time	TSOLDER	260 · 10	°C · Sec

Note : Operation at above absolute maximum can adversely affect device reliability.

DC OPERATING CONDITION

(TA = 0 to 70°C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT	NOTE
Power Supply Voltage	VCC	3.0	3.3	3.6	V	1
Input High Voltage	VIH	2.0	3.0	VCC + 2.0	V	1, 2
Input Low Voltage	VIL	VSS – 2.0	0	0.8	V	1, 3

Note : 1. All voltage are referenced to VSS = 0V.
2. VIH (max) is acceptable 5.6V AC pulse width with ≤ 3ns of duration.
3. VIL (min) is acceptable –2.0V AC pulse width with ≤ 3ns of duration.

AC OPERATING CONDITION

(TA = 0 to 70°C, VDD = 3.3 ± 0.3V, VSS = 0V)

PARAMETER	SYMBOL	VALUE	UNIT
AC Input High / Low Level Voltage	VIH / VIL	2.4 / o.4	V
Input Timing Measurement Reference Level Voltage	Vtrip	1.4	V
Input Rise / Fall Time	tR / tF	1	ns
Output Timing Measurement Reference Level Voltage	Voutref	1.4	V
Output Load Capacitance for Access Time Measurement	CL	*Note	pF

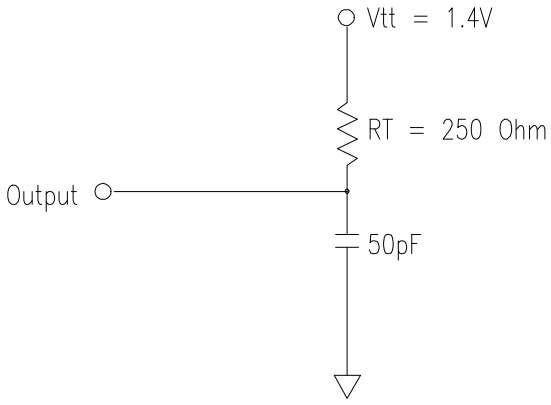
Note : *. Output load to measure access time is equivalent to two TTL gates and one capacitor (50pF).
For details, refer to AC/DC output circuit.

CAPACITANCE

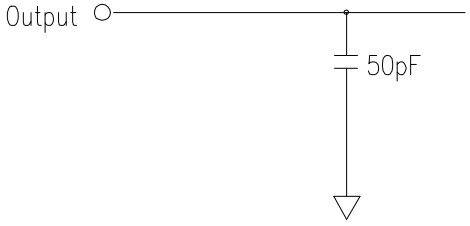
(TA = 25°C, f = 1MHz)

PARAMETER	PIN	SYMBOL	MIN	MAX	TYP.	UNIT
Input Capacitance	CK0, CK1	CIN1	-	50	-	pF
	CKE0	CIN2	-	65	-	pF
	/S0	CIN3	-	65	-	pF
	A0~A11, BA0, BA1	CIN4	-	65	-	pF
	/RAS, /CAS, /WE	CIN5	-	65	-	pF
	DQM0~DQM7	CIN6	-	20	-	pF
Data Input/Output Capacitance	DQ0~DQ63, CB0~CB7	CI/O	-	18	-	pF

OUTPUT LOAD CIRCUIT



DC Output Load Circuit



AC Output Load Circuit

DC CHARACTERISTICS I

(TA = 0 to 70°C, VDD = 3.3 ± 0.3V)

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTE
Input Leakage Current	ILI	-9	9	uA	1
Output Leakage Current	ILO	-1	1	uA	2
Output High Voltage	VOH	2.4	-	V	IOH = -4mA
Output Low Voltage	VOL	-	0.4	V	IOL = +4mA

Note : 1. VIN = 0 to 3.6V. All other pins are not tested under VIN = 0V.
2. DOUT is disabled. VOUT = 0 to 3.6V.

DC CHARACTERISTICS II

(TA = 0 to 70°C, VDD = 3.3 ± 0.3V, VSS = 0V)

PARAMETER	SYMBOL	TEST CONDITION		SPEED				UNIT	NOTE
				-75	-8	-10P	-10S		
Operating Current	IDD1	Burst Length = 1, One bank active tRC ≥ tRC(min), IOL = 0mA		810	720	630	630	mA	1
Precharge Standby Current in Power Down Mode	IDD2P	CKE ≤ VIL(max), tCK = min		18				mA	
	IDD2PS	CKE ≤ VIL(max), tCK = ∞		18				mA	
Precharge Standby Current in Non Power Down Mode	IDD2N	CKE ≥ VIH(min), /CS ≥ VIH(min), tCK = min Input signals are changed one time during 2clks. All other pins ≥ VDD – 0.2V or ≤ 0.2V		135				mA	
	IDD2NS	CKE ≥ VIH(max), tCK = ∞ Input signals are stable.		135				mA	
Active Standby Current in Power Down Mode	IDD3P	CKE ≤ VIL(max), tCK = min		45				mA	
	IDD3PS	CKE ≤ VIL(max), tCK = ∞		45				mA	
Active Standby Current in Non Power Down Mode	IDD3N	CKE ≥ VIH(min), /CS ≥ VIH(min), tCK = min Input signals are changed one time during 2clks. All other pins ≥ VDD – 0.2V or ≤ 0.2V		270				mA	
	IDD3NS	CKE ≥ VIH(max), tCK = ∞ Input signals are stable.		270				mA	
Burst Mode Operating Current	IDD4	tCK ≥ tCK(min), IOL = 0mA All banks active	CL = 3	1080	990	810	810	mA	1
			CL = 2	810	810	810	810		
Auto Refresh Current	IDD5	tRRC ≥ tRRC(min), All banks active		1800	1800	1620	1620	mA	2
Self Refresh Current	IDD6	CKE ≤ 0.2V		18				mA	
				4.5				mA	3

Note : 1. IDD1 and IDD4 depend on output loading and cycle rates. Specified values are measured with the output open.
2. Min. of tRRC (Refresh /RAS cycle time) is shown at AC CHARACTERISTICS II.
3. L-part (HYM7V75A801BLTZG)

AC CHARACTERISTICS I

(AC operating conditions unless otherwise noted)

PARAMETER		SYMBOL	-75		-8		-10P		-10S		UNIT	NOTE
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
System Clock Cycle Time	/CAS Latency = 3	tCK3	7.5	1000	8	1000	10	1000	10	1000	ns	
	/CAS Latency = 2	tCK2	10		10		10		12			
Clock High Pulse Width		tCHW	2.5	-	3	-	3	-	3	-	ns	I
Clock Low Pulse Width		tCLW	2.5	-	3	-	3	-	3	-	ns	I
Access Time from Clock	/CAS Latency = 3	tAC3	-	5.4	-	6	-	6	-	6	ns	2
	/CAS Latency = 2	tAC2	-	6	-	6	-	6	-	6		
Data-Out Hold Time		tOH	2.7	-	3	-	3	-	3	-	ns	
Data-Input Setup Time		tDS	1.5	-	2	-	2	-	2	-	ns	1
Data-Input Hold Time		tDH	0.8	-	1	-	1	-	1	-	ns	1
Address Setup Time		tDS	1.5	-	2	-	2	-	2	-	ns	1
Address Hold Time		tDH	0.8	-	1	-	1	-	1	-	ns	1
CKE Setup Time		tDS	1.5	-	2	-	2	-	2	-	ns	1
CKE Hold Time		tDH	0.8	-	1	-	1	-	1	-	ns	1
Command Setup Time		tDS	1.5	-	2	-	2	-	2	-	ns	1
Command Hold Time		tDH	0.8	-	1	-	1	-	1	-	ns	1
CLK to Data Output in Low-Z time		tOLZ	1	-	1	-	1	-	1	-	ns	
CLK to Data Output in High-Z time	/CAS Latency = 3	tOHZ3	2.7	5.4	3	6	3	6	3	6	ns	
	/CAS Latency = 2	tOHZ2	3	6	3	6	3	6	3	6		

Note : 1. Assume tR / tF (input rise and fall time) is 1ns.
2. Access times to be measured with input signals of 1v/ns edge rate.

AC CHARACTERISTICS II

PARAMETER		SYMBOL	-75		-8		-10P		-10S		UNIT	NOTE
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
/RAS Cycle Time	Operation	tRC	67.5	-	70	-	70	-	70	-	ns	
	Auto Refresh	tRRC	67.5		70		70		70			
/RAS to /CAS Delay		tRCD	22.5	-	20	-	20	-	20	-	ns	
/RAS Active Time		tRAS	45	100K	48	100K	50	100K	50	100K	ns	
/RAS Precharge Time		tRP	22.5	-	20	-	20	-	20	-	ns	
/RAS to /RAS Bank Active Delay		tRRD	15	-	16	-	20	-	20	-	ns	
/CAS to /CAS Delay		tCCD	1	-	1	-	1	-	1	-	CLK	
Write Command to Data-in Delay		tWTL	0	-	0	-	0	-	0	-	CLK	
Data-in to Precharge Command		tDPL	2	-	1	-	1	-	1	-	CLK	
Data-in to Active Command		tDAL	5	-	4	-	3	-	3	-	CLK	
DQM to Data-out Hi-Z		tDQZ	2	-	2	-	2	-	2	-	CLK	
DQM to Data-in Mask		tDQM	0	-	0	-	0	-	0	-	CLK	
MRS to New Command		tMRD	2	-	2	-	2	-	2	-	CLK	
Precharge to Data Output Hi-Z	/CAS Latency = 3	tPROZ3	3	-	3	-	3	-	3	-	CLK	
	/CAS Latency = 2	tPROZ2	2	-	2	-	2	-	2	-		
Power Down Exit Time		tPDE	1	-	1	-	1	-	1	-	CLK	
Self Refresh Exit Time		tSRE	1	-	1	-	1	-	1	-	CLK	1
Refresh Time		tREF	64	-	64	-	64	-	64	-	ms	

Note : 1. A new command can be given tRRC after self refresh exit.

OPERATING OPTION TABLE

HYM7V75A801BTZG-75 / HYM7V75A801BLTZG-75

	/CAS LATENCY	tRCD	tRAS	tRC	tRP	tAC	tOH
133MHz (7.5ns)	3CLKS	3CLKS	6CLKS	9CLKS	3CLKS	5.4ns	2.7ns
125MHz (8.0ns)	3CLKS	3CLKS	6CLKS	9CLKS	3CLKS	6ns	3ns
100MHz (10.0ns)	2CLKS	2CLKS	5CLKS	7CLKS	2CLKS	6ns	3ns
83MHz (12.0ns)	2CLKS	2CLKS	4CLKS	6CLKS	2CLKS	6ns	3ns
66MHz (15.0ns)	2CLKS	2CLKS	4CLKS	6CLKS	2CLKS	6ns	3ns

HYM7V75A801BTZG-8 / HYM7V75A801BLTZG-8

	/CAS LATENCY	tRCD	tRAS	tRC	tRP	tAC	tOH
125MHz (8.0ns)	3CLKS	3CLKS	6CLKS	9CLKS	3CLKS	6ns	3ns
100MHz (10.0ns)	2CLKS	2CLKS	5CLKS	7CLKS	2CLKS	6ns	3ns
83MHz (12.0ns)	2CLKS	2CLKS	4CLKS	6CLKS	2CLKS	6ns	3ns
66MHz (15.0ns)	2CLKS	2CLKS	4CLKS	6CLKS	2CLKS	6ns	3ns

HYM7V75A801BTZG-10P / HYM7V75A801BLTZG-10P

	/CAS LATENCY	tRCD	tRAS	tRC	tRP	tAC	tOH
100MHz (10.0ns)	2CLKS	2CLKS	5CLKS	7CLKS	2CLKS	6ns	3ns
83MHz (12.0ns)	2CLKS	2CLKS	5CLKS	7CLKS	2CLKS	6ns	3ns
66MHz (15.0ns)	2CLKS	2CLKS	4CLKS	6CLKS	2CLKS	6ns	3ns

HYM7V75A801BTZG-10S / HYM7V75A801BLTZG-10S

	/CAS LATENCY	tRCD	tRAS	tRC	tRP	tAC	tOH
100MHz (10.0ns)	3CLKS	2CLKS	5CLKS	7CLKS	2CLKS	6ns	3ns
83MHz (12.0ns)	2CLKS	2CLKS	5CLKS	7CLKS	2CLKS	6ns	3ns
66MHz (15.0ns)	2CLKS	2CLKS	4CLKS	6CLKS	2CLKS	6ns	3ns

COMMAND TRUTH TABLE

		CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	DQM	ADDR	A10/AP	BA	NOTE
Mode Register Set		H	X	L	L	L	L	X	OP code			
No Operation		H	X	H	X	X	X	X	X			
				L	H	H	H					
Bank Active		H	X	L	L	H	H	X	RA		V	
Read		H	X	L	H	L	H	X	CA	L	V	
Read with Autoprecharge										H		
Write		H	X	L	H	L	L	X	CA	L	V	
Write with Autoprecharge										H		
Precharge All Banks		H	X	L	L	H	L	X	X	H	X	
Precharge Selected Bank										L	V	
Burst Stop		H	X	L	H	H	L	X	X			
DQM		H	X					V	X			
Auto Refresh		H	H	L	L	L	H	X	X			
Self Refresh	Entry	H	L	L	L	L	H	X	X			
	Exit	L	H	H	X	X	X	X				1
				L	H	H	H					
Precharge Power Down	Entry	H	L	H	X	X	X	X	X			
				L	H	H	H					
	Exit	L	H	H	X	X	X	X				
				L	H	H	H					
Clock Suspend	Entry	H	L	H	X	X	X	X	X			
				L	V	V	V					
	Exit	L	H	X				X				

Note : 1. Existing Self Refresh occurs by asynchronously bringing CKE from low to high.
2. X = Don' t care, H = Logic High, L = logic Low, BA = Bank Address, CA = Column Address, OP code = Operand code, NOP = No operation

PACKAGE DIMENSIONS