Revision History

Revision .3 (March 1998)

Some Parameter values & Characteristics of comp. level are changed as below :

- Input leakage currents (Inputs) : ±5uA to ±1uA.
- Input leakage currents (I/O) : ±5uA to ±1.5uA.
- Cin to be measured at V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200mV.
- AC Operating Condition is changed as defined :
  V_{IH}(max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
  V_{IL}(min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
- I_{CC3}PS is changed 1mA to 2mA.

Revision .4 (March 1998)

- I_{CC2}N, I_{CC2}NS, I_{CC3}N & I_{CC3}NS in comp. level values are changed.

Revision .5 (June 1998)

- t_{SH} (-10 binning) is revised.

KMM366S803BTL SDRAM DIMM

8Mx64 SDRAM DIMM based on 8Mx8, 2Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM366S803BTL is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung KMM366S803BTL consists of eight CMOS 8M x 8 bit with 2banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.33uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The KMM366S803BTL is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
KMM366S803BTL-G0	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  Latency (Access from column address)
  Burst length (1, 2, 4, 8 & Full page)
  Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,000mil)**, double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	*CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	*BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	*CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	VSS	106	*CB5	134	NC	162	VSS
23	VSS	51	NC	79	*CLK2	107	VSS	135	NC	163	*CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	NC	109	NC	137	*CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

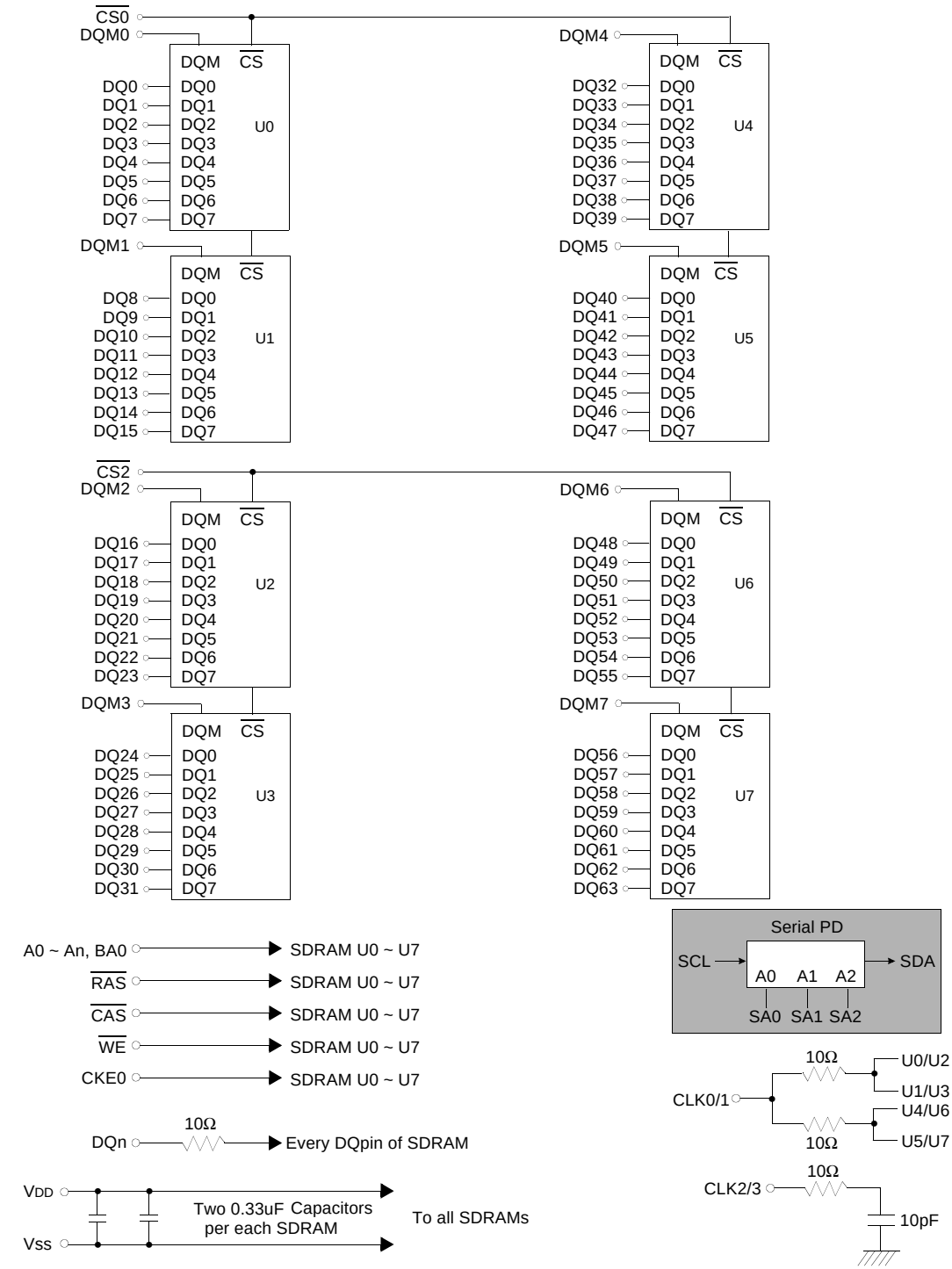
Pin Name	Function
A0 ~ A12	Address input (Multiplexed)
BA0	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK1	Clock input
CKE0	Clock enable input
CS0, CS2	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+t_{SS} prior to valid command.
A0 ~ A12	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, Column address : CA0 ~ CA8
BA0	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	8	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-8	-	8	uA	3
Input leakage current (I/O pins)	I_{IL}	-1.5	-	1.5	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A12, BA0)	C_{IN1}	40	60	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	40	60	pF
Input capacitance (CKE0)	C_{IN3}	35	55	pF
Input capacitance (CLK0 ~ CLK1)	C_{IN4}	25	35	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN5}	25	35	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	5	15	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	5	15	pF

MAXIMUM TRACE LENGTHS

Signal	Max lengths	Unit	Signal	Max lengths	Unit
A0 ~ A12	8.0	Inches	CKE0	5.5	Inches
BA0	8.0	Inches	$\overline{CS0}$, $\overline{CS2}$	4.0	Inches
$\overline{RAS}$	8.0	Inches	DQM0 ~ DQM7	3.0	Inches
$\overline{CAS}$	8.0	Inches	DQ0 ~ DQ63	2.0	Inches
$\overline{WE}$	8.0	Inches			

DC CHARACTERISTICS

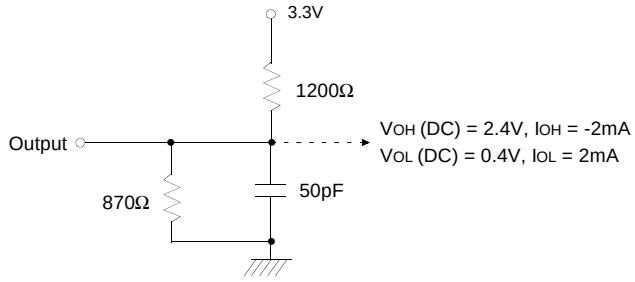
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version -0	Unit	Note
Operating current (One bank active)	I_{CC1}	Burst length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		720	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		8	mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		8		
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		160	mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		80		
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		16	mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		16		
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		240	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		160	mA	
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0 mA Page burst 2Banks activated t_{CCD} = 2CLKs	**3**	840	mA	1
			2	720		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		1,080	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V		8	mA	

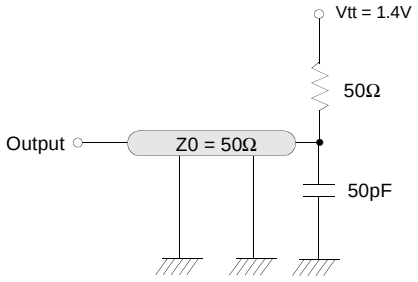
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version	Unit	Note
			-0		
Row active to row active delay		tRRD(min)	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	24	ns	1
Row precharge time		tRP(min)	24	ns	1
Row active time		tRAS(min)	50	ns	1
		tRAS(max)	100	us	
Row cycle time		tRC(min)	80	ns	1
Last data in to row precharge		tRDL(min)	12	ns	2
Last data in to new col. address delay		tCDL(min)	1	CLK	2
Last data in to burst stop		tBDL(min)	1	CLK	2
Col. address to col. address delay		tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3		2	ea	4
	CAS latency=2		1		

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-0		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	t_{CC}	10	1000	ns	1
	CAS latency=2		13			
CLK to valid output delay	CAS latency=3	t_{SAC}		7	ns	1,2
	CAS latency=2			7		
Output data hold time	CAS latency=3	t_{OH}	3		ns	1,2
	CAS latency=2		3			
CLK high pulse width		t_{CH}	3.5		ns	3
CLK low pulse width		t_{CL}	3.5		ns	3
Input setup time		t_{SS}	2.5		ns	3
Input hold time		t_{SH}	1		ns	3
CLK to output in Low-Z		t_{SLZ}	1		ns	2
CLK to output in Hi-Z	CAS latency=3	t_{SHZ}		7	ns	1
	CAS latency=2			7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM366S803BTL-G0 (Unit : Number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		80ns	50ns	24ns	20ns	24ns	10ns	10ns	12ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	2
83MHz (12.0ns)	2	7	5	2	2	2	1	1	1
75MHz (13.0ns)	2	7	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

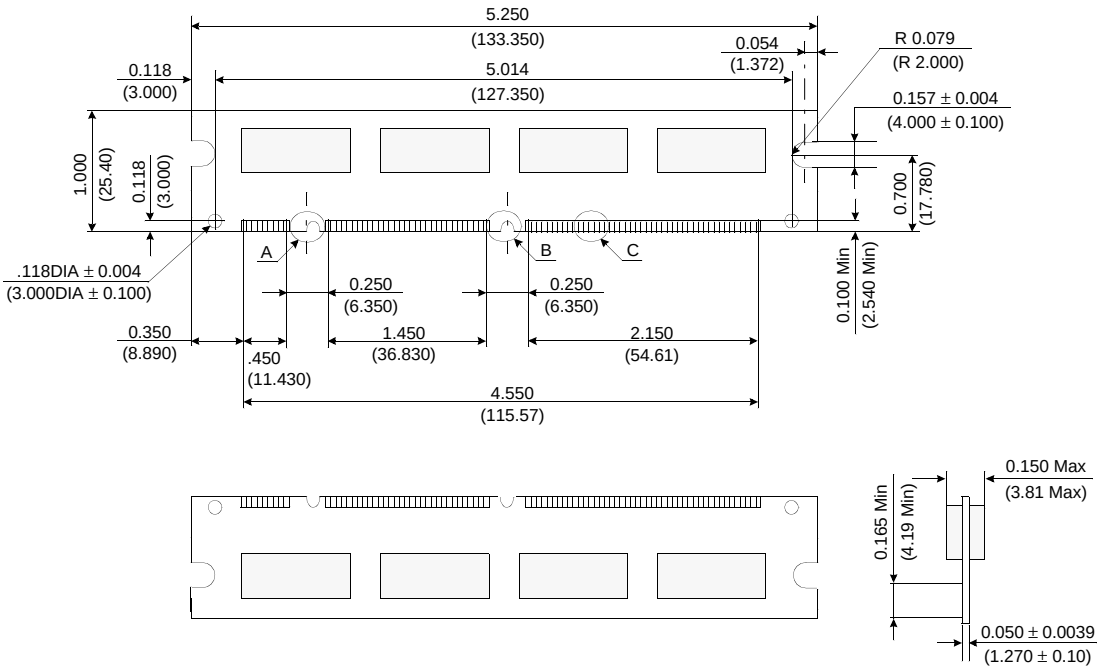
Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA_0	A_{10}/AP	A_{12} ~ A_{11}, A_9 ~ A_0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A_0 ~ A_8)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A_0 ~ A_8)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	Both banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

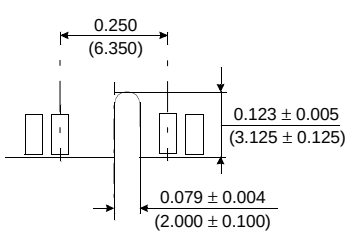
(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
A_0 ~ A_{12}, BA_0 : Program keys. (@ MRS)
2. MRS can be issued only at both banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at both banks precharge state.
4. BA_0 : Bank select address.
If "Low" at read, write, row active and precharge, bank A is selected.
If "High" at read, write, row active and precharge, bank B is selected.
If A_{10}/AP is "High" at row precharge, BA_0 is ignored and both banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0),
but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

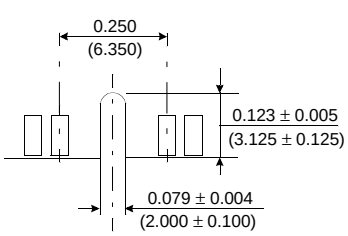
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

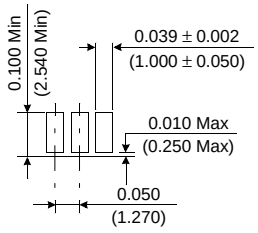




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : KM48S8020BT

KMM366S803BTL-G0

- Organization : 8Mx64
- Composition : 8Mx8 *8
- Used component part # : KM48S8020BT-G10
- # of banks in module : 1 bank
- # of banks in component : 2 banks
- Feature : 1,000mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported	Hex value	Note
		-0	-0	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	13	0Dh	1
4	# of column address on this assembly	9	09h	1
5	# of module banks on this assembly	1 bank	01h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	7ns	70h	2
11	DIMM configuraion type	Non Parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	2 banks	02h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	13ns	D0h	2
24	SDRAM access time from clock @CAS latency of 2	7ns	70h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	24ns	18h	
28	Minimum row active to row active delay (tRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	18h	
30	Minimum activate precharge time (=tRAS)	50ns	32h	
31	Module bank density	1 bank of 64MB	10h	
32~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	EBh	

Byte #	Function Described	Function Supported	Hex value	Note
		-0	-0	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Samsung memory)	K	4Bh	
74	Manufacturer part # (Samsung memory)	M	4Dh	
75	Manufacturer part # (Memory module)	M	4Dh	
76	Manufacturer part # (Memory type & edge connector)	3	33h	
77	Manufacturer part # (Data bits)	Blank	20h	
78	..... Manufacturer part # (Data bits)	6	36h	
79	..... Manufacturer part # (Data bits)	6	36h	
80	Manufacturer part # (Mode & operating voltage)	S	53h	
81	Manufacturer part # (Module density)	Blank	20h	
82	..... Manufacturer part # (Module density)	8	38h	
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	0	30h	
84	Manufacturer part # (Compositon component)	3	33h	
85	Manufacturer part # (Component revision)	B	42h	
86	Manufacturer part # (Package type)	T	54h	
87	Manufacturer part # (PCB revision)	L	4Ch	
88	Manufacturer part # (Hyphen)	" - "	2Dh	
89	Manufacturer part # (Power)	G	47h	
90	Manufacturer part # (Minimum cycle time)	0	30h	
91	Manufacturer revision code (For PCB)	L	4Ch	
92	..... Manufacturer revision code (For component)	B-die (3rd Gen.)	42h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	-	FFh	
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	-	FFh	

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year.
4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.