

DDR2 SDRAM VLP RDIMM

MT36HVS25672(P) – 2GB

MT36HVS51272(P) – 4GB

MT36HVZS51272(P) – 4GB

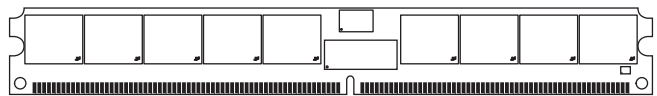
For component data sheets, refer to Micron's Web site: www.micron.com

Features

- 240-pin, very low profile registered dual in-line memory module (VLP RDIMM)
- Compatible with ATCA form factors
- Fast data transfer rates: PC2-4200, PC2-5300, or PC2-6400
- Supports ECC error detection and correction
- $V_{DD} = V_{DDQ} = +1.8V$
- $V_{DDSPD} = +1.7V$ to $+3.6V$
- JEDEC-standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- 4n-bit prefetch architecture
- Dual rank using TwinDie™ devices
- Multiple internal device banks for concurrent operation
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency - 1 tCK
- Programmable burst lengths (BL): 4 or 8
- Adjustable data-output drive strength
- 64ms, 8,192-cycle refresh
- On-die termination (ODT)
- Serial presence-detect (SPD) with EEPROM
- Gold edge contacts

Figure 1: 240-Pin VLP RDIMM (ATCA Form Factor)

PCB height: 17.9mm (0.705in)



Options

- Full module heat spreader (4GB density only)
- Parity
- Operating temperature¹
 - Commercial ($0^{\circ}C \leq T_A \leq +70^{\circ}C$)
 - Industrial ($-40^{\circ}C \leq T_A \leq +85^{\circ}C$)
- Package
 - 240-pin DIMM (Pb-free)
- Frequency/CAS latency²
 - 2.5ns @ CL = 5 (DDR2-800)
 - 2.5ns @ CL = 6 (DDR2-800)
 - 3.0ns @ CL = 5 (DDR2-667)
 - 3.75ns @ CL = 4 (DDR2-533)³

Marking

- Z
- P
- None
- I
- Y
- -80E
- -800
- -667
- -53E

- Notes: 1. Contact Micron for industrial temperature module offerings.
 2. CL = CAS (READ) latency; registered mode will add one clock cycle to CL.
 3. Not recommended for new designs.

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)				t _{RCD} (ns)	t _{RP} (ns)	t _{RC} (ns)
		CL = 6	CL = 5	CL = 4	CL = 3			
-80E	PC2-6400	–	800	533	–	12.5	12.5	55
-800	PC2-6400	800	667	533	–	15	15	55
-667	PC2-5300	–	667	533	400	15	15	55
-53E	PC2-4200	–	–	533	400	15	15	55

Table 2: Addressing

Parameter	2GB	4GB
Refresh count	8K	8K
Row address	16K A[13:0]	16K A[13:0]
Device bank address	4 BA[1:0]	8 BA[2:0]
Device configuration	1Gb TwinDie (256 Meg x 4)	2Gb TwinDie (512 Meg x 4)
Column address	2K A[11, 9:0]	2K A[11, 9:0]
Module rank address	2 S#[1:0]	2 S#[1:0]

Table 3: Part Numbers and Timing Parameters – 2GB Modules

Base device: MT47H256M4THK,¹ 1Gb TwinDie DDR2 SDRAM

Part Number ²	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL- ^t RCD- ^t RP)
MT36HVS25672(P)Y-667__	2GB	256 Meg x 72	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT36HVS25672(P)Y-53E__	2GB	256 Meg x 72	4.3 GB/s	3.75ns/533 MT/s	4-4-4

Table 4: Part Numbers and Timing Parameters – 4GB Modules

Base device: MT47H512M4THN,¹ 2Gb TwinDie DDR2 SDRAM

Part Number ²	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL- ^t RCD- ^t RP)
MT36HVS51272(P)Y-80E__	4GB	512 Meg x 72	6.2 GB/s	2.5ns/800 MT/s	5-5-5
MT36HVS51272(P)Y-800__	4GB	512 Meg x 72	6.2 GB/s	2.5ns/800 MT/s	6-6-6
MT36HVS51272(P)Y-667__	4GB	512 Meg x 72	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT36HVS51272(P)Y-53E__	4GB	512 Meg x 72	4.3 GB/s	3.75ns/533 MT/s	4-4-4

Table 5: Part Numbers and Timing Parameters – 4GB Modules with Heat Spreader

Base device: MT47H512M4THN,¹ 2Gb TwinDie DDR2 SDRAM

Part Number ²	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL- ^t RCD- ^t RP)
MT36HVZS51272(P)Y-80E__	4GB	512 Meg x 72	6.2 GB/s	2.5ns/800 MT/s	5-5-5
MT36HVZS51272(P)Y-800__	4GB	512 Meg x 72	6.2 GB/s	2.5ns/800 MT/s	6-6-6
MT36HVZS51272(P)Y-667__	4GB	512 Meg x 72	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT36HVZS51272(P)Y-53E__	4GB	512 Meg x 72	4.3 GB/s	3.75ns/533 MT/s	4-4-4

- Notes:
1. The data sheets for the base devices can be found on Micron's Web site.
 2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes.
Example: MT36HVS51272PY-667D1.



Pin Assignments and Descriptions

Table 6: Pin Assignments

240-Pin DDR2 VLP RDIMM Front								240-Pin DDR2 VLP RDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREF	31	DQ19	61	A4	91	Vss	121	Vss	151	Vss	181	VDDQ	211	DQS14
2	Vss	32	Vss	62	VDDQ	92	DQS5#	122	DQ4	152	DQ28	182	A3	212	DQS14#
3	DQ0	33	DQ24	63	A2	93	DQS5	123	DQ5	153	DQ29	183	A1	213	Vss
4	DQ1	34	DQ25	64	VDD	94	Vss	124	Vss	154	Vss	184	VDD	214	DQ46
5	Vss	35	Vss	65	Vss	95	DQ42	125	DQS9	155	DQS12	185	CK0	215	DQ47
6	DQS0#	36	DQS3#	66	Vss	96	DQ43	126	DQS9#	156	DQS12#	186	CK0#	216	Vss
7	DQS0	37	DQS3	67	VDD	97	Vss	127	Vss	157	Vss	187	VDD	217	DQ52
8	Vss	38	Vss	68 ³	NC/ PAR_IN	98	DQ48	128	DQ6	158	DQ30	188	A0	218	DQ53
9	DQ2	39	DQ26	69	VDD	99	DQ49	129	DQ7	159	DQ31	189	VDD	219	Vss
10	DQ3	40	DQ27	70	A10	100	Vss	130	Vss	160	Vss	190	BA1	220	RFU
11	Vss	41	Vss	71	BA0	101	SA2	131	DQ12	161	CB4	191	VDDQ	221	RFU
12	DQ8	42	CB0	72	VDDQ	102	NC	132	DQ13	162	CB5	192	RAS#	222	Vss
13	DQ9	43	CB1	73	WE#	103	Vss	133	Vss	163	Vss	193	S0#	223	DQS15
14	Vss	44	Vss	74	CAS#	104	DQS6#	134	DQS10	164	DQS17	194	VDDQ	224	DQS15#
15	DQS1#	45	DQS8#	75	VDDQ	105	DQS6	135	DQS10#	165	DQS17#	195	ODT0	225	Vss
16	DQS1	46	DQS8	76	S1#	106	Vss	136	Vss	166	Vss	196	A13	226	DQ54
17	Vss	47	Vss	77	ODT1	107	DQ50	137	RFU	167	CB6	197	VDD	227	DQ55
18	RESET#	48	CB2	78	VDDQ	108	DQ51	138	RFU	168	CB7	198	Vss	228	Vss
19	NC	49	CB3	79	Vss	109	Vss	139	Vss	169	Vss	199	DQ36	229	DQ60
20	Vss	50	Vss	80	DQ32	110	DQ56	140	DQ14	170	VDDQ	200	DQ37	230	DQ61
21	DQ10	51	VDDQ	81	DQ33	111	DQ57	141	DQ15	171	CKE1	201	Vss	231	Vss
22	DQ11	52	CKE0	82	Vss	112	Vss	142	Vss	172	VDD	202	DQS13	232	DQS16
23	Vss	53	VDD	83	DQS4#	113	DQS7#	143	DQ20	173	A14	203	DQS13#	233	DQS16#
24	DQ16	54 ¹	NC/BA2	84	DQS4	114	DQS7	144	DQ21	174	A15	204	Vss	234	Vss
25	DQ17	55 ²	NC/ ERR_OUT	85	Vss	115	Vss	145	Vss	175	VDDQ	205	DQ38	235	DQ62
26	Vss	56	VDDQ	86	DQ34	116	DQ58	146	DQS11	176	A12	206	DQ39	236	DQ63
27	DQS2#	57	A11	87	DQ35	117	DQ59	147	DQS11#	177	A9	207	Vss	237	Vss
28	DQS2	58	A7	88	Vss	118	Vss	148	Vss	178	VDD	208	DQ44	238	VDDSPD
29	Vss	59	VDD	89	DQ40	119	SDA	149	DQ22	179	A8	209	DQ45	239	SA0
30	DQ18	60	A5	90	DQ41	120	SCL	150	DQ23	180	A6	210	Vss	240	SA1

- Notes:
1. Pin 54 is NC for 2GB and BA2 for 4GB.
 2. Pin 55 is NC for nonparity and ERR_OUT for parity.
 3. Pin 68 is NC for nonparity and PAR_IN for parity.

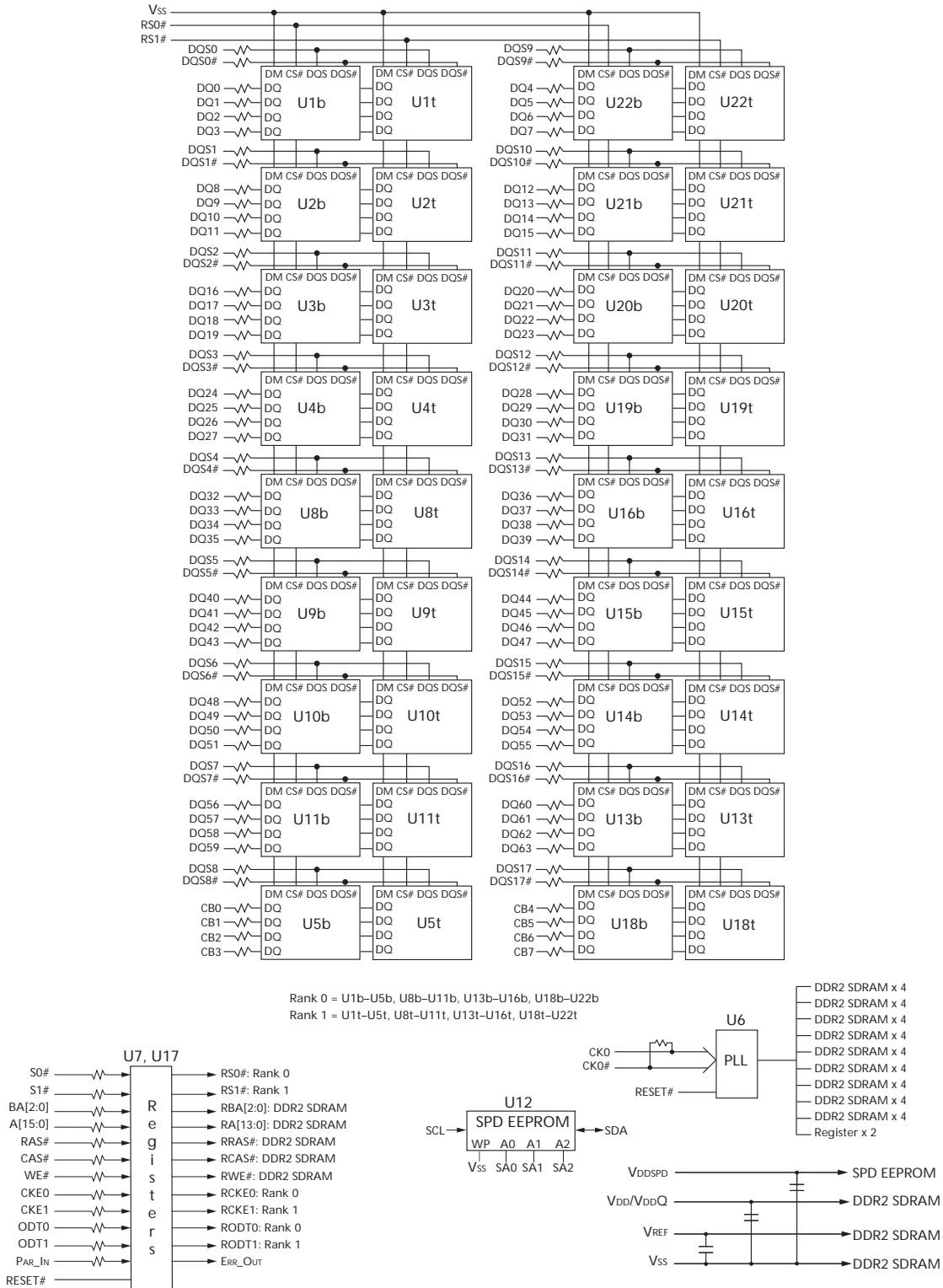


Table 7: Pin Descriptions

Symbol	Type	Description
A[15:0]	Input	Address inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA[2:0]) or all device banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. A[13:0] (2GB, 4GB). A[15:14] are connected for parity.
BA[2:0]	Input	Bank address inputs: BA[2/1:0] define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA[2/1:0] define which mode register (MR, EMR1, EMR2, and EMR3) is loaded during the LOAD MODE command. BA[1:0] (2GB), BA[2:0] (4GB).
CK0, CK0#	Input	Clock: CK and CK# are differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data (DQ, DQS, and DQS#) is referenced to the crossings of CK and CK#.
CKE[1:0]	Input	Clock enable: CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DDR2 SDRAM.
ODT[1:0]	Input	On-die termination: ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR2 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS, DQS#, DM, and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
PAR_IN	Input	Parity input: Parity bit for the address, RAS#, CAS#, and WE#.
RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input	Reset: Asynchronously forces all registered outputs LOW when RESET# is LOW. This signal can be used during power-up to ensure that CKE is LOW and DQ are High-Z.
S#[1:0]	Input	Chip select: S# enables (registered LOW) and disables (registered HIGH) the command decoder.
SA[2:0]	Input	Serial address inputs: These pins are used to configure the SPD EEPROM device.
SCL	Input	Serial clock for SPD EEPROM: SCL is used to synchronize communication to and from the SPD EEPROM.
CB[7:0]	I/O	Check bits.
DQ[63:0]	I/O	Data input/output: Bidirectional data bus.
DQS[17:0], DQS#[17:0]	I/O	Data strobe: DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command. Output with read data. Edge-aligned with read data. Input with write data. Center-aligned with write data.
SDA	I/O	Serial data: SDA is a bidirectional pin used to transfer addresses and data into and out of the SDA EEPROM portion of the module.
ERR_OUT	Output (open drain)	Parity error output: Parity error found on the command and address bus.
VDD/VDDQ	Supply	Power supply (1.8V ±0.1V): The component VDD and VDDQ are connected to the module VDD.
VDDSPD	Supply	Serial EEPROM power supply: +1.7V to +3.6V.
VREF	Supply	Reference voltage: VDD/2.
Vss	Supply	Ground.
NC	–	No connect: These pins are not connected on the module.
RFU	–	Reserved for future use.

Functional Block Diagram

Figure 2: Functional Block Diagram



General Description

The MT36HVS25672(P), MT36HVS51272(P), and MT36HVZS51272(P) DDR2 SDRAM modules are high-speed, CMOS dynamic random access 2GB and 4GB memory modules organized in a x72 configuration. These DDR2 SDRAM modules use internally configured, 4-bank (2GB) or 8-bank (4GB) DDR2 Twin Die SDRAM devices.

DDR2 SDRAM modules use double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a $4n$ -prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR2 SDRAM module effectively consists of a single $4n$ -bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding n -bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR2 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Clock, control, command, and address signals are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Register and PLL Operation

These DDR2 SDRAM modules operate in registered mode, where the command/address input signals are latched in the registers on the rising clock edge and sent to the DDR2 SDRAM devices on the following rising clock edge (data access is delayed by one clock cycle). A phase-lock loop (PLL) on the module receives and redrives the differential clock signals (CK, CK#) to the DDR2 SDRAM devices. The register(s) and PLL reduce clock, control, command, and address signals loading by isolating DRAM from the system controller. PLL clock timing is defined by JEDEC specifications and ensured by use of the JEDEC clock reference board. Registered mode will add one clock cycle to CL.

Serial Presence-Detect Operation

DDR2 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I²C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA[2:0], which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is connected to VSS, permanently disabling hardware write protect.

Electrical Specifications

Stresses greater than those listed in Table 8 may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 8: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	
VDD/VDDQ	VDD/VDDQ supply voltage relative to Vss	-0.5	2.3	V	
VIN, VOUT	Voltage on any pin relative to Vss	-0.5	2.3	V	
II	Input leakage current; Any input $0V \leq V_{IN} \leq V_{DD}$; VREF input $0V \leq V_{IN} \leq 0.95V$ (All other pins not under test = 0V)	Address inputs, RAS#, CAS#, WE#, S#, CKE, BA, ODT	-10	10	μA
		CK, CK#	-250	250	
IOZ	Output leakage current; $0V \leq V_{OUT} \leq V_{DDQ}$; DQ and ODT are disabled	DQ, DQS, DQS#	-10	10	μA
IVREF	VREF leakage current; VREF = valid VREF level		-72	72	μA
TA	Module ambient operating temperature	Commercial	0	+70	$^{\circ}C$
		Industrial	-40	+85	$^{\circ}C$
TC ¹	DDR2 SDRAM component case operating temperature ²	Commercial	0	+85	$^{\circ}C$
		Industrial	-40	+95	$^{\circ}C$

- Notes: 1. The refresh rate is required to double when $85^{\circ}C < T_C \leq 95^{\circ}C$.
2. For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.

DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR2 component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades, as shown in Table 9.

Table 9: Module and Component Speed Grades
DDR2 components may exceed the listed module speed grades

Module Speed Grade	Component Speed Grade
-80E	-25E
-800	-25
-667	-3
-53E	-37E

Design Considerations

Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

Power

Operating voltages are specified at the DRAM, not at the edge connector of the module. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.

IDD Specifications

Table 10: DDR2 IDD Specifications and Conditions – 2GB

Values are for the MT47H256M4 DDR2 SDRAM only and are computed from values specified in the 1Gb TwinDie (256 Meg x 4) component data sheet

Parameter/Condition	Symbol	-667	-53E	Units
Operating one bank active-precharge current: $t_{CK} = t_{CK} (IDD)$, $t_{RC} = t_{RC} (IDD)$, $t_{RAS} = t_{RAS} \text{ MIN} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD0 ¹	1,836	1,656	mA
Operating one bank active-read-precharge current: I _{OUT} = 0mA; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$, $t_{RC} = t_{RC} (IDD)$, $t_{RAS} = t_{RAS} \text{ MIN} (IDD)$, $t_{RCD} = t_{RCD} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is the same as IDD4W	IDD1 ¹	2,106	1,926	mA
Precharge power-down current: All device banks idle; $t_{CK} = t_{CK} (IDD)$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	IDD2P ²	252	252	mA
Precharge quiet standby current: All device banks idle; $t_{CK} = t_{CK} (IDD)$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating	IDD2Q ²	1,026	936	mA
Precharge standby current: All device banks idle; $t_{CK} = t_{CK} (IDD)$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching	IDD2N ²	1,116	1,026	mA
Active power-down current: All device banks open; $t_{CK} = t_{CK} (IDD)$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN exit MR[12] = 0	756	666	mA
	Slow PDN exit MR[12] = 1	342	342	mA
Active standby current: All device banks open; $t_{CK} = t_{CK} (IDD)$, $t_{RAS} = t_{RAS} \text{ MAX} (IDD)$, $t_{RP} = t_{RP} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	IDD3N ²	1,386	1,206	mA
Operating burst write current: All device banks open; Continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$, $t_{RAS} = t_{RAS} \text{ MAX} (IDD)$, $t_{RP} = t_{RP} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD4W ¹	3,276	2,736	mA
Operating burst read current: All device banks open; Continuous burst reads; I _{OUT} = 0mA; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$, $t_{RAS} = t_{RAS} \text{ MAX} (IDD)$, $t_{RP} = t_{RP} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD4R ¹	3,456	2,826	mA
Burst refresh current: $t_{CK} = t_{CK} (IDD)$; REFRESH command at every $t_{RFC} (IDD)$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	IDD5 ²	3,456	3,276	mA
Self refresh current: CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating	IDD6 ²	252	252	mA
Operating bank interleave read current: All device banks interleaving reads; I _{OUT} = 0mA; BL = 4, CL = CL (IDD), AL = $t_{RCD} (IDD) - 1 \times t_{CK} (IDD)$; $t_{CK} = t_{CK} (IDD)$, $t_{RC} = t_{RC} (IDD)$, $t_{RRD} = t_{RRD} (IDD)$, $t_{RCD} = t_{RCD} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching	IDD7 ¹	4,536	4,266	mA

- Notes: 1. Value calculated as one module rank in this operating condition; all other module ranks in IDD2P (CKE LOW) mode.
2. Value calculated reflects all module ranks in this operating condition.

Table 11: DDR2 IDD Specifications and Conditions – 4GB

Values are for the MT47H512M4 DDR2 SDRAM only and are computed from values specified in the 2Gb TwinDie (512 Meg x 4) component data sheet

Parameter/Condition	Symbol	-80E/ -800	-667	-53E	Units
Operating one bank active-precharge current: $t_{CK} = t_{CK} (IDD)$, $t_{RC} = t_{RC} (IDD)$, $t_{RAS} = t_{RAS} MIN (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD0 ¹	1,836	1,746	1,476	mA
Operating one bank active-read-precharge current: I _{OUT} = 0mA; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$, $t_{RC} = t_{RC} (IDD)$, $t_{RAS} = t_{RAS} MIN (IDD)$, $t_{RCD} = t_{RCD} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is the same as IDD4W	IDD1 ¹	2,196	2,016	1,926	mA
Precharge power-down current: All device banks idle; $t_{CK} = t_{CK} (IDD)$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	IDD2P ²	252	252	252	mA
Precharge quiet standby current: All device banks idle; $t_{CK} = t_{CK} (IDD)$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating	IDD2Q ²	1,026	846	846	mA
Precharge standby current: All device banks idle; $t_{CK} = t_{CK} (IDD)$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching	IDD2N ²	1,116	936	936	mA
Active power-down current: All device banks open; $t_{CK} = t_{CK} (IDD)$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN exit MR[12] = 0	846	666	666	mA
	Slow PDN exit MR[12] = 1	306	306	306	mA
Active standby current: All device banks open; $t_{CK} = t_{CK} (IDD)$, $t_{RAS} = t_{RAS} MAX (IDD)$, $t_{RP} = t_{RP} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	IDD3N ²	1,296	1,206	1,026	mA
Operating burst write current: All device banks open; Continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$, $t_{RAS} = t_{RAS} MAX (IDD)$, $t_{RP} = t_{RP} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD4W ¹	2,826	2,376	2,196	mA
Operating burst read current: All device banks open; Continuous burst reads; I _{OUT} = 0mA; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$, $t_{RAS} = t_{RAS} MAX (IDD)$, $t_{RP} = t_{RP} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD4R ¹	2,826	2,376	2,196	mA
Burst refresh current: $t_{CK} = t_{CK} (IDD)$; REFRESH command at every $t_{RFC} (IDD)$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	IDD5 ²	4,446	4,086	3,996	mA
Self refresh current: CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating	IDD6 ²	252	252	252	mA
Operating bank interleave read current: All device banks interleaving reads; I _{OUT} = 0mA; BL = 4, CL = CL (IDD), AL = $t_{RCD} (IDD) - 1 \times t_{CK} (IDD)$; $t_{CK} = t_{CK} (IDD)$, $t_{RC} = t_{RC} (IDD)$, $t_{RRD} = t_{RRD} (IDD)$, $t_{RCD} = t_{RCD} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching	IDD7 ¹	6,246	5,256	5,076	mA

- Notes: 1. Value calculated as one module rank in this operating condition; all other module ranks in IDD2P (CKE LOW) mode.
2. Value calculated reflects all module ranks in this operating condition.

Register and PLL Specifications

Table 12: Register Specifications
SSTU32868 devices or equivalent JESD82-17

Parameter	Symbol	Pins	Condition	Min	Max	Units
DC high-level input voltage	V _{IH(DC)}	Control, command, address	SSTL_18	V _{REF(DC)} + 125	V _{DDQ} + 250	mV
DC low-level input voltage	V _{IL(DC)}	Control, command, address	SSTL_18	0	V _{REF(DC)} - 125	mV
AC high-level input voltage	V _{IH(AC)}	Control, command, address	SSTL_18	V _{REF(DC)} + 250	V _{DD}	mV
AC low-level input voltage	V _{IL(AC)}	Control, command, address	SSTL_18	0	V _{REF(DC)} - 250	mV
Output high voltage	V _{OH}	Parity output	LVC MOS	1.2	–	V
Output low voltage	V _{OL}	Parity output	LVC MOS	–	0.5	V
Input current	I _I	All pins	V _I = V _{DDQ} or V _{SSQ}	–5	5	μA
Static standby	I _{DD}	All pins	RESET# = V _{SSQ} (I _o = 0)	–	100	μA
Static operating	I _{DD}	All pins	RESET# = V _{SSQ} ; V _I = V _{IH(AC)} or V _{IL(DC)} I _o = 0	–	80	mA
Dynamic operating (clock tree)	I _{DD}	n/a	RESET# = V _{DD} , V _I = V _{IH(AC)} or V _{IL(AC)} , I _o = 0; CK and CK# switching 50% duty cycle	–	Varies by manufacturer	μA
Dynamic operating (per each input)	I _{DD}	n/a	RESET# = V _{DD} , V _I = V _{IH(AC)} or V _{IL(AC)} , I _o = 0; CK and CK# switching 50% duty cycle; One data input switching at ^t CK/2, 50% duty cycle	–	Varies by manufacturer	μA
Input capacitance (per device, per pin)	C _I	All inputs except RESET#	V _I = V _{REF} ±250mV; V _{DDQ} = 1.8V	2.5	4	pF
Input capacitance (per device, per pin)	C _I	RESET#	V _I = V _{DDQ} or V _{SSQ}	–	Varies by manufacturer	pF

- Notes: 1. Timing and switching specifications for the register listed above are critical for proper operation of the DDR2 SDRAM RDIMMs. These are meant to be a subset of the parameters for the specific device used on the module. Detailed information for this register is available in JEDEC Standard JESD82.

Table 13: PLL Specifications
CU877 device or equivalent JESD82-8.01

Parameter	Symbol	Pins	Condition	Min	Max	Units
DC high-level input voltage	V _{IH}	RESET#	LVC MOS	0.65 × V _{DD}	–	V
DC low-level input voltage	V _{IL}	RESET#	LVC MOS	–	0.35 × V _{DD}	V
Input voltage (limits)	V _{IN}	RESET#, CK, CK#	–	–0.3	V _{DDQ} + 0.3	V
DC high-level input voltage	V _{IH}	CK, CK#	Differential input	0.65 × V _{DD}	–	V
DC low-level input voltage	V _{IL}	CK, CK#	Differential input	–	0.35 × V _{DD}	V
Input differential-pair cross voltage	V _{IX}	CK, CK#	Differential input	(V _{DDQ} /2) - 0.15	(V _{DDQ} /2) + 0.15	V
Input differential voltage	V _{ID(DC)}	CK, CK#	Differential input	0.3	V _{DDQ} + 0.4	V
Input differential voltage	V _{ID(AC)}	CK, CK#	Differential input	0.6	V _{DDQ} + 0.4	V
Input current	I _I	RESET#	V _I = V _{DDQ} or V _{SSQ}	–10	10	μA
		CK, CK#	V _I = V _{DDQ} or V _{SSQ}	–250	+250	μA
Output disabled current	I _{ODL}	–	RESET# = V _{SSQ} ; V _I = V _{IH(AC)} or V _{IL(DC)}	100	–	μA
Static supply current	I _{DDLD}	–	CK = CK# = LOW	–	500	μA
Dynamic supply	I _{DD}	n/a	CK, CK# = 270 MHz, all outputs open (not connected to PCB)	–	300	mA
Input capacitance	C _{IN}	Each input	V _I = V _{DDQ} or V _{SSQ}	2	3	pF

Table 14: PLL Clock Driver Timing Requirements and Switching Characteristics

Parameter	Symbol	Min	Max	Units
Stabilization time	t _L	–	15	μs
Input clock slew rate	t _{slr(i)}	1.0	4	V/ns
SSC modulation frequency	–	30	33	kHz
SSC clock input frequency deviation	–	0.0	–0.5	%
PLL loop bandwidth (–3dB from unity gain)	–	2.0	–	MHz

Notes: 1. PLL timing and switching specifications are critical for proper operation of the DDR2 DIMM. This is a subset of parameters for the specific PLL used. Detailed PLL information is available in JEDEC Standard JESD82.

Serial Presence-Detect

Table 15: Serial Presence-Detect EEPROM DC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	VDDSPD	1.7	3.6	V
Input high voltage: Logic 1; All inputs	V _{IH}	VDDSPD × 0.7	VDDSPD + 0.5	V
Input low voltage: Logic 0; All inputs	V _{IL}	-0.6	VDDSPD × 0.3	V
Output low voltage: I _{OUT} = 3mA	V _{OL}	-	0.4	V
Input leakage current: V _{IN} = GND to VDD	I _{LI}	0.1	3.0	μA
Output leakage current: V _{OUT} = GND to VDD	I _{LO}	0.05	3.0	μA
Standby current	I _{SB}	1.6	4.0	μA
Power supply current, READ: SCL clock frequency = 100 kHz	I _{CCR}	0.4	1.0	mA
Power supply current, WRITE: SCL clock frequency = 100 kHz	I _{CCW}	2.0	3.0	mA

Table 16: Serial Presence-Detect EEPROM AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	t _{AA}	0.2	0.9	μs	1
Time the bus must be free before a new transition can start	t _{BUF}	1.3	-	μs	
Data-out hold time	t _{DH}	200	-	ns	
SDA fall time	t _F	-	300	ns	2
SDA rise time	t _R	-	300	ns	2
Data-in hold time	t _{HD:DAT}	0	-	μs	
Start condition hold time	t _{H:STA}	0.6	-	μs	
Clock HIGH period	t _{HIGH}	0.6	-	μs	
Noise suppression time constant at SCL, SDA inputs	t _I	-	50	ns	
Clock LOW period	t _{LOW}	1.3	-	μs	
SCL clock frequency	f _{SCL}	-	400	kHz	
Data-in setup time	t _{SU:DAT}	100	-	ns	
Start condition setup time	t _{SU:STA}	0.6	-	μs	3
Stop condition setup time	t _{SU:STO}	0.6	-	μs	
WRITE cycle time	t _{WRC}	-	10	ms	4

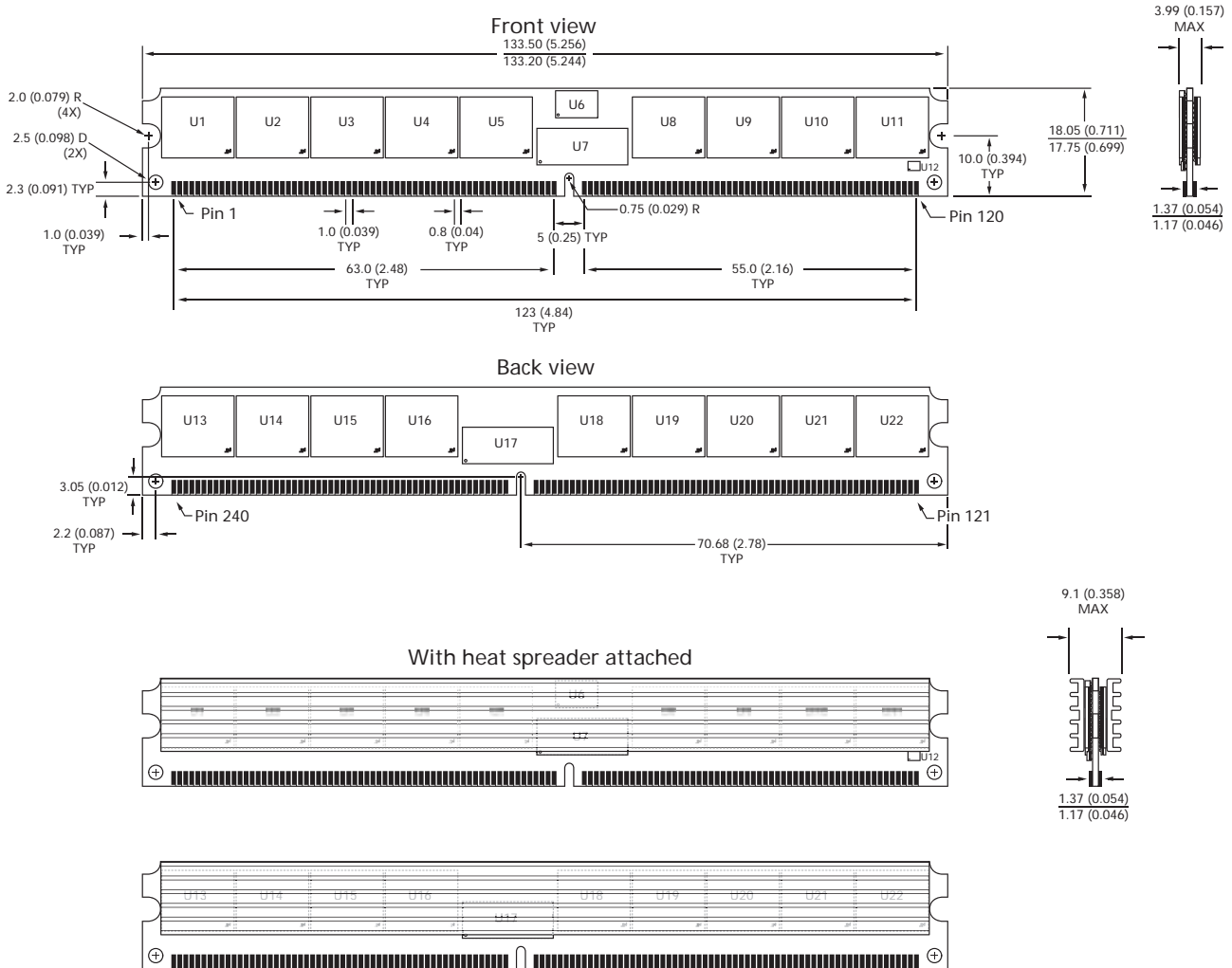
- Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
 2. This parameter is sampled.
 3. For a restart condition or following a WRITE cycle.
 4. The SPD EEPROM WRITE cycle time (t_{WRC}) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistance, and the EEPROM does not respond to its slave address.

Serial Presence-Detect Data

For the latest serial presence-detect data, refer to Micron's SPD page:
www.micron.com/SPD.

Module Dimensions

Figure 3: 240-Pin DDR2 VLP RDIMM



- Notes: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only.



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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.