ALPHA SEMICONDUCTOR
Excellence in Analog Power Products

# AS OP-207

## Dual Matched-Ultra Low offset Operational Amplifier

### FEATURES

- Low Offset.....100μV Max.
- Low $V_{OS}$ Drift.....1.0Vμ/°C Max
- Offset Voltage Match..... 90mV Max
- Low Bias Current Match..... 3.5 nA Max
- Common-Mode Rejection Match ..... 120dBMin
- Offset Voltage Match vs. Temp..... 1.0μV/°C Max
- Low Noise.....0.6μ$V_{pp}$Max

### APPLICATIONS

- Differential-In/Differential-Out Amplifiers
- High-Stability Instrumentation Amplifiers
- Medical Instrumentation
- Strain Gauge & Thermocouple
- Precision Absolute Value Circuits

### PRODUCT DESCRIPTION

The ALPHA Semiconductor AS OP-207 is a dual-matched operational amplifier that offers two independent monolithic high-performance OP07 operational amplifiers in a single 14-pin dual-in-line package. Tight matching between channels is provided on the main parameters including offset, tracking of offset vs. temperature, non-inverting bias current and common mode and power supply rejection ratios. Each amplifier is fully internally compensated and protected.

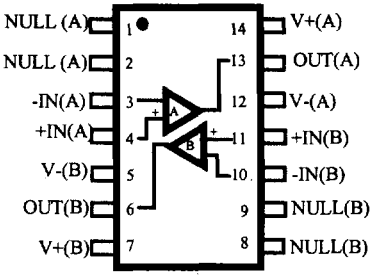
The OP-207 is available in several different grades. The AS OP-207 is available in a hermetically sealed 14 pin dual-in-line package. The operating temperature is 0°C to 70°C and -55°C to +125°C.

### ORDERING INFORMATION

| Plastic DIP 14-PIN | TA=25°C $V_{OS}$ Max (mv) | Oper. Temp. Range |
|---|---|---|
| OP207EP | 100 | COM |
| OP207FP | 200 | COM |

### PIN CONNECTIONS

**14-Pin EPOXY DIP**




**Top View**

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage..... ±22V
Internal Power Dissipation (Note 1) .....500mW
Differential Input Voltage..... ±30V
Input Voltage (Note 2)..... ±22V
Output Short-Circuit Duration .....Indefinite
Storage Temperature Range
Y Package.....-65 to +150°C
Operating Temperature Range
OP207A, OP207 B .....-55 to +125°C
OP207E, OP207F .....0 to +70°C
Dice Junction Temperature(Tj).....-65 to +150°C
Lead Temperature (Soldering, 60 Sec.) ..... 300°C

**NOTES:**

1. See Table for maximum ambient temperature rating and derating factor.
2. Absolute maximum ratings apply to both DICE and packaged parts unless otherwise noted.
3. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

| PACKAGE TYPE | MAXIMUM AMBIENT TEMPERATURE FOR RATING | DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE |
|---|---|---|
| 14-Pin Plastic DIP | 106°C | 11.3 mW/°C |
| 14-Pin Hermetic DIP | 42°C | 6.0mW/°C |

## ELECTRICAL CHARACTERISTICS at $V_S$=±15V, Ta=25°C, unless otherwise specified.

| Parameter | Symbol | Conditions | OP207E | | | OP207F | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| *Input Offset Voltage* | $V_{os}$ | R=100W | | 35 | 100 | | 60 | 200 | µV |
| Input Offset Voltage Stability | $V_{OS}$/Time | (Note 1) | | 0.3 | 1.5 | | 0.4 | 2.0 | $\mu V/M_o$ |
| Input Offset Current | $I_{os}$ | | | 0.9 | 2.8 | | 1.5 | 6.0 | nA |
| Input Bias Current | $I_B$ | | | ±1 | ±3 | | ±2 | ±7 | nA |
| Input Noise Voltage (Note 2) | $e_{npp}$ | 0.1Hz to10Hz | | 0.35 | 0.6 | | 0.35 | 0.6 | $\mu V_{p-p}$ |
| *Input Noise Voltage Density (Note 2)* | $e_n$ | $f_o$=10Hz | | *10.3* | *18.0* | | *10.3* | *18.0* | nV/√Hz |
| Input Noise Voltage Density (Note 2) | $e_n$ | $f_o$=100Hz | | 10.0 | 13.0 | | 10.0 | 13.0 | nV/√Hz |
| Input Noise Voltage Density (Note 2) | $e_n$ | $f_o$=1000Hz | | 9.6 | | | 9.6 | | nV/√Hz |
| Input Noise Current (Note 2) | $i_{np\ p}$ | 0.1 Hz to 10Hz | | 14 | 30 | | 14 | 30 | $pA_{p-p}$ |
| *Input Noise Current Density (Note 2)* | $i_n$ | $f_o$=10Hz | | 0.32 | 0.80 | | 0.32 | 0.80 | nV/√Hz |
| Input Noise Current Density (Note 2) | $i_n$ | $f_o$=100 Hz | | 0.14 | 0.23 | | 0.14 | 0.23 | nV/√Hz |
| Input Noise Current Density (Note 2) | $i_n$ | $f_o$=1000Hz | | 0.12 | | | 0.12 | | nV/√Hz |
| Input Resistance-Differential-Mode | $R_{in}$ | (Note 3) | 20 | 60 | | 8 | 30 | | MΩ |
| Input Resistance-Common-Mode | $R_{inCM}$ | | | 200 | | | 120 | | GΩ |
| Input Voltage Range | IVR | | ±13 | ±14 | | ±13 | ±14 | | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM}$=±13.0 | 106 | 123 | | 100 | 120 | | dB |
| Power Supply Rejection Ratio | PSRR | $V_S$=±3V to ±18 | | 5 | 20 | | 7 | 32 | µV/V |
| Large-Signal Voltage Gain | $AV_O$ | $R_l$ ≥2kΩ, $V_o$=±10V | 200 | 500 | | 150 | 400 | | V/mV |
| Output Voltage Swing | $V_o$ | Rl≥10kΩ | ±12.5 | ±13.0 | | ±12.5 | ±13.0 | | V |
| Output Voltage Swing | $V_o$ | Rl ≥2kΩ | ±12.0 | ±12.8 | | ±12.0 | ±12.8 | | V |
| Output Voltage Swing | $V_o$ | Rl ≥1kΩ | ±10.0 | ±12.0 | | ±10.0 | ±12.0 | | V |
| Slew Rate | SR | Rl ≥2kΩ | | 0.2 | | | 0.2 | | V/µs |
| Closed-Loop Bandwidth | BW | $A_{vcl}$=+1.0(Note 1) | | 0.6 | | | 0.6 | | MHz |
| Open-Loop Output Resistance | $R_o$ | $V_o$=0, Io=0 | | 60 | | | 60 | | W |
| Power Consumption | $P_d$ | Each Amplifiers No Load | | 180 | 240 | | 200 | 300 | mW |
| Offset Adjustment Range | | $R_p$=20kΩ | | ±4 | | | ±4 | | mV |
| Input Capacitance | Cin | | | 8 | | | 8 | | pF |

**Notes:**
1. Long term input offset voltage stability refers to the averaged trend line of Vos Vs. time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in Vos during the first 30 operating days are typically. 2.5 mV.
2. Sample tested
3. Guaranteed by design.

## INDIVIDUAL CHARACTERISTICS at $V_S$=±15V, -55°C≤Ta≤+125°C, unless otherwise specified.

| Parameter | Symbol | Conditions | OP207E Min. | OP207E Typ. | OP207E Max. | OP207F Min. | OP207F Typ. | OP207F Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage | $V_{os}$ | | | 75 | 230 | | 100 | 400 | µV |
| Average Input Offset Voltage<br>Drift Without External Trim<br>With External Trim | <br>$TCV_{os}$<br>$TCV_{os}$ | <br>(Note 1)<br>Rp=20Ω (note 3) | | <br>0.4<br>0.4 | <br>1.3 | | <br>0.7<br>0.7 | <br>1.8 | µV/°C<br>µV/°C |
| Input Offset Current | $I_{os}$ | | | 1.8 | 5.6 | | 3.0 | 12.0 | nA |
| Average Input Offset Current Drift | $TCI_{os}$ | Note 2 | | 10 | | | 12 | | pA/°C |
| Input Bias Current | $I_B$ | | | ±3.0 | ±5.6 | | ±4.0 | ±14.0 | nA |
| Average Input Bias Current Drift | $TCI_B$ | Note 2 | | 12 | | | 18 | | pA/°C |
| Input Voltage Range | IVR | | ±13 | ±13.5 | | ±13 | ±13.5 | | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM}$ ±13.0 V | 103 | 120 | | 97 | 117 | | dB |
| Power Supply Rejection Ratio | PSRR | $V_s$=±3V to ±18V | | 7 | 32 | | 10 | 51 | µV/V |
| Large-Signal Voltage Gain | $A_{vo}$ | $R_l$≥2Ω, $V_o$= ±10V | 150 | 400 | | 120 | 350 | | V/mV |
| Output Voltage Swing | $V_o$ | $R_l$≥2Ω | ±12.0 | ±12.8 | | ±12.0 | ±12.8 | | V |

## MATCHING CHARACTERISTICS at $V_S$=±15V, Ta=+25°C, Unless otherwise specified.

| Parameter | Symbol | Conditions | OP207E Min. | OP207E Typ. | OP207E Max. | OP207F Min. | OP207F Typ. | OP207F Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage Match | $V_{os}$ | | | 30 | 90 | | 50 | 280 | µV |
| Average Noninverting Bias Current | $I_B$+ | | | ±1.5 | ±3.5 | | ±1.5 | ±6.0 | nA |
| Noninverting Offset Current | $I_{OS}$+ | | | ±0.7 | ±3.5 | | ±1.0 | ±6.0 | nA |
| Inverting Offset Current | $I_{OS}$+ | | | ±0.7 | ±3.5 | | ±1.0 | ±6.0 | nA |
| Common-Mode Rejection Ratio Match | CMRR | $V_{CM}$=±13V | 103 | 120 | | 96 | 114 | | dB |
| Power Supply Rejection Ratio Match | PSRR | $V_S$=3V to ±18 | | 7 | 32 | | 10 | 51 | µV/V |
| Channel Separation | CS | (Note 2) | 126 | 140 | | 126 | 140 | | dB |

## MATCHING CHARACTERISTICS at $V_S$=±15V, -55°C≤Ta≤+125°C, unless otherwise specified.

| Parameter | Symbol | Conditions | OP207B Min. | OP207B Typ. | OP207B Max. | Units |
|---|---|---|---|---|---|---|
| Input Offset Voltage Match | $V_{os}$ | | | 180 | 450 | µV |
| Input Offset Voltage Tracking<br>Drift Without External Trim<br>With External Trim | <br>$TCV_{os}$<br>$TCV_{os}$ | <br>(Note 2)<br>Rp=20W (note 3), Channel A only | | <br>0.9<br>0.4 | <br>1.5<br>1.3 | µV/°C<br>µV/°C |
| Average Noninverting Bias Current | $I_B$+ | | | ±3 | ±12 | nA |
| Average Drift of Noninverting Bias Current | $TCI_B$+ | Note 2 | | 12 | | pA/°C |
| Noninverting Offset Current | $I_{OS}$+ | | | 3 | 12 | nA |
| Average Drift of Noninverting Offset Current | $TCI_{OS}$ | Note 2 | | 15 | | pA/°C |
| Inverting Offset Current | $I_{OS}$ | | | 3 | 12 | nA |
| Common-Mode Rejection Ratio Match | CMRR | $V_{CM}$=±13V | 94 | 114 | | dB |
| Power Supply Rejection Ratio Match | PSRR | $V_s$=±3V to +18 | | 16 | 100 | µV/V |

## INDIVIDUAL CHARACTERISTICS at $V_S$=±15V, 0°C≤Ta≤+70°C, unless otherwise specified.

| Parameter | Symbol | Conditions | OP207E Min. | OP207E Typ. | OP207E Max. | OP207F Min. | OP207F Typ. | OP207F Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage | $V_{os}$ | | | 60 | 200 | | 90 | 350 | µV |
| Average Input Offset Voltage<br>Drift Without External Trim<br>With External Trim | <br>$TCV_{os}$<br>$TCV_{os}$ | <br>(Note 1,2)<br>Rp=20Ω (note 3) | | <br>0.4<br>0.4 | <br>1.3 | | <br>0.7<br>0.7 | <br>1.8 | µV/°C<br>µV/°C |
| Input Offset Current | $I_{os}$ | | | 1.4 | 5 | | 2.5 | 10 | nA |
| Average Input Offset Current Drift | $TCI_{os}$ | | | 10 | | | 12 | | pA/°C |
| Input Bias Current | $I_B$ | | | ±2 | ±5 | | ±3 | ±11 | nA |
| Average Input Bias Current Drift | $TCI_B$ | | | 12 | | | 18 | | pA/°C |
| Input Voltage Range | IVR | | ±13 | ±13.5 | | ±13 | ±13.5 | | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM}$ ±13.0 V | 103 | 120 | | 97 | 117 | | dB |
| Power Supply Rejection Ratio | PSRR | $V_s$=±3V to ±18V | | 7 | 32 | | 10 | 51 | µV/V |
| Large-Signal Voltage Gain | $A_{vo}$ | $R_l$ ≥2Ω, $V_o$= ±10V | 150 | 400 | | 120 | 350 | | V/mV |
| Output Voltage Swing | $V_o$ | $R_l$ ≥2Ω | ±12.0 | ±12.8 | | ±12.0 | ±12.8 | | V |

**Notes:**
1. Exclude the first hour of operation to allow for stabilization of external circuitry
2. Sample tested

## MATCHING CHARACTERISTICS at $V_S$=±15V, 0°C≤Ta≤ +70°C, unless otherwise specified.

| Parameter | Symbol | Conditions | OP-207E Min. | OP-207E Typ. | OP-207E Max. | OP-207F Min. | OP-207F Typ. | OP-207F Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage Match | $V_{os}$ | | | 60 | 150 | | 120 | 350 | µV |
| Input Offset Voltage Tracking<br>Drift Without External Trim<br>With External Trim | <br>$TCV_{os}$<br>$TCV_{os}$ | <br>(Note 1)<br>Rp=20Ω (Note 3), Channel A only | | <br>0.5<br>0.3 | <br>1.0<br>1.0 | | <br>0.9<br>0.4 | <br>1.5<br>1.3 | µV/°C<br>µV/°C |
| Average Noninverting Bias Current | $I_B^+$ | | | ±2 | ±5 | | ±3 | ±10 | nA |
| Average Drift of Noninverting Bias Current | $TCI_B^+$ | (Note 1) | | 10 | | | 12 | | pA/°C |
| Noninverting Offset Current | $I_{OS}^+$ | | | 2 | 5 | | 3 | 10 | nA |
| Average Drift of Noninverting Offset Current | $TCI_{OS}$ | (Note 1) | | 12 | | | 15 | | pA/°C |
| Inverting Offset Current | $I_{OS-}$ | | | 2 | 5 | | 3 | 10 | nA |
| Common-Mode Rejection Ratio Match | CMRR | $V_{CM}$=±13V | 100 | 117 | | 94 | 114 | | dB |
| Power Supply Rejection Ratio Match | PSRR | $V_s$=±3V to +18 | | 10 | 51 | | 16 | 100 | µV/V |

**Notes:**
1. Sample tested

## OFFSET NULLING CIRCUIT

## BURN-IN CIRCUIT

## APPLICATION INFORMATION

### DUAL MATCHED OP-AMP ADVANTAGES

Dual matched operational amplifiers provide a powerful tool in solving some difficult circuit design problems. Circuits include true instrumentation amplifiers, high common-mode rejection DC amplifiers, extremely low drift, low DC drift active filters, dual tracking voltage references and many other demanding applications. These designs all require good matching between two operational amplifiers.

The circuit below shows the how the errors can be reduced through these advantages. If the resistors are matched, then the gain of each side will be identical. If the offset voltage of each amplifier is matched, then the net differential voltage at the amplifiers output will be zero. The impedance of each input, both common-mode and differential-mode, are extremely high, an important feature not possible with single operational amplifier circuits.

### POWER SUPPLIES

The positive supply terminals are completely independent and may be powered by separate supplies if desired. However, this method would sacrifice the advantages of power supply rejection ratio matching. The negative supply terminals are both connected to the common substrate and must be tied to the same voltage.

### OFFSET TRIMMING

Each amplifier has its own offset voltage trimming. The performance over temperature is done by trimming one side to match the offset of the other side.

The AS OP-207 provides the lowest drift when trimmed with 20kΩ potentiometer. This value provides about ±4mV of adjustment range..