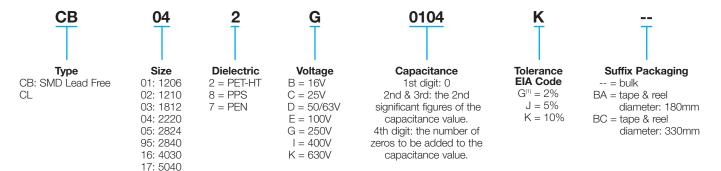
# Film Chip Capacitors



# How to Order, Dimensions and Construction

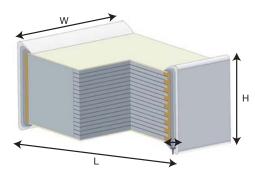
### **HOW TO ORDER**



Example of an order: How to order a chip film PET-HT 100nF ±10% 250V bulk packaging.

(1): Tolerance G available only for PPS Series.

18: 6054



### **CASE DIMENSIONS: millimeters (inches)**

Size Code	Equivalent size	Length (L)	Width (W)	Termination Return
01	1206	3.30±0.30 (0.130±0.012)	1.60±0.30 (0.063±0.012)	0.50±0.30 (0.020±0.012)
02	1210	3.30±0.30 (0.130±0.012)	2.50±0.30 (0.098±0.012)	0.50±0.30 (0.020±0.012)
03	1812	4.50±0.50 (0.177±0.020)	3.20±0.50 (0.126±0.020)	0.60±0.40 (0.024±0.157)
04	2220	5.80±0.50 (0.228±0.020)	5.00±0.50 (0.197±0.020)	0.80±0.60 (0.032±0.024)
05	2824	7.20±0.50 (0.283±0.020)	6.10±0.50 (0.240±0.020)	0.80±0.60 (0.032±0.024)
95	2840	7.20±0.50 (0.283±0.020)	10.0±0.80 (0.343±0.031)	0.80±0.60 (0.032±0.024)
16	4030	10.5±0.60 (0.413±0.024)	7.60±0.80 (0.299±0.031)	0.80±0.60 (0.032±0.024)
17	5040	12.8±0.60 (0.504±0.024)	10.2±0.80 (0.401±0.031)	0.80±0.60 (0.032±0.024)
18	6054	15.3±0.60 (0.602±0.024)	13.7±0.80 (0.539±0.031)	0.80±0.60 (0.032±0.024)

#### STACKED FILM CONSTRUCTION

Our SMD Film capacitors (CB series) are using stacked technology with metallized plastic film, which forms the basis for the capacitive element. Combined with the nacked design choice, it gives our products an again better self-healing capability as well as a very good capacitance per volume ratio. This also means that internal construction of the multilayer stack, usually hidden in encapsulated film capacitors design, is visible at the cut edges in the surface mount configuration. In a typical film capacitor stack, hundreds of film layers are compacted during manufacture. Under a micro-

scope these have the appearance of pages in a book. Subsequent manufacturing and pcb assembly processes allow a small amount of relaxation in these layers. In some cases, small gaps between layers may become visible. These are referred to as microgaps, and their occurrence is a standard feature of this technology. Even if it can be considered an cosmetic issue, presence of these gaps has no effect at all on mechanical or electrical performance or reliability. (Detailed report is available upon request.)



# Film Chip Capacitors



# **Electrical Properties and Test Conditions - CB Series**

## **STANDARDIZATION**

Reference Standard is CECC 32201

Test	Description	Performance
Capacitance C	Measurement frequency 1 KHz 20°C	Shall be within tolerance of the rated value
Dissipation Factor DF	Measurement frequency 1 KHz 20°C	DF < 100.10 <sup>-4</sup>
Insulation Resistance IR	Voltage applied: 10V  for  Vr < 100V 100V  for  Vr > = 100V	IR > 1000 Mohms for C <= 0.33µF IR x C > 400sec. For C > 0.33µF
Dielectric Strength	Surge Voltage = 1.4Vr applied for 1mm between terminals	There shall be no direct breakdown
Mounting	Board = 1.6mm (0.063") thick epoxy glass laminated or alumine substrate	C = within ± 2% of initial value DF = < = 50.10⁴ at 1 KHz IR = within initial limit
Adhesion	Force of 5 N applied for 10 secs.	No visible damage
Board Bending Test	Bending of 1 mm(0.039") for 90 mm (3.543") length	C = within ± 2% of initial value No visible damage
Thermal Shock	500 cycles -55/+125°C	C = within ± 5% of initial value ESR = no more than 3 times initial value IR = not less than 50% of the initial limit
Damp Heat Steady State	40°C 93% RH / no voltage / 56 days	C = within ± 7% of initial value Delta DF = < 50.10 <sup>-4</sup> at 1 KHz IR = not less than 50% of the initial limit
Accelerated Damp Heat (Load Humidity)	85℃ 85% RH 1.5V-500H	C = within $\pm$ 7% of initial value Delta DF = $<$ = 70.10 <sup>-4</sup> at 1 KHz IR = not less than 50% of the initial limit
Life Test	85℃ / 1.25Vr / 1000H	C = within $\pm$ 8% of initial value Delta DF = $<$ 50.10 $^{-4}$ at 1 KHz IR = not less than 50% of the initial limit
Life Test	105°C / Vr/1,000 Hours 125°C / Vr/1,000 Hours	C = within ± 7% of initial value Delta DF = < 50.10 <sup>-4</sup> at 1 KHz IR = not less than 50% of the initial limit
Charge/Discharge	10,000 cycle / Vr	C = within $\pm$ 5% of initial value DF = $<$ 50.10 <sup>-4</sup> at 1 KHz IR = not less than 50% of the initial limit

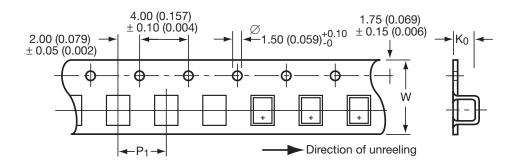


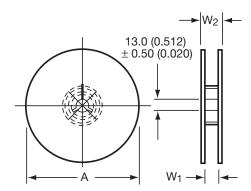
# Film Chip Capacitors

# Packaging - CB Series



#### **TAPE & REEL DIMENSIONS**





### **TAPE & REEL CHARACTERISTICS**

In accordance with IEC 286 and EIA 481, the material used:

Carrier tape: Antistatic Material

Cover tape: Polyester Reel: Recyclable Material

Parts in bulk or on reel are packed in hermetically sealed

plastic bags.

#### RECOMMENDATIONS

Once the sealed bag is opened, the capacitors must be stored in a dry atmosphere until soldering.

Recommended storage conditions are:

PET & PEN: < 30°C and R.H.<60% for a maximum of

168 hours

PPS: < 30°C and R.H.<60% for a maximum of

4 weeks

The use-by date is 3 years if kept in origin plastic bags. In case of storage outside the conditions recommended above the capacitors must be dried prior to soldering.

Recommended drying conditions are:

48 hours minimum at 60°C and RH < 10%.

