iC-OC
INTEGRATING LIGHT-VOLTAGE CONVERTER

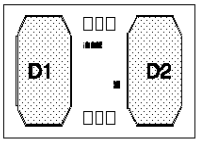
FEATURES

- Two photosensors with integrating amplifiers
- Integration time can be set externally
- Internal shift register for chain connection
- Detection of low supply voltage
- TTL/CMOS-compatible logic inputs and outputs
- 5V supply voltage
- Low power consumption
- Photosensors with 1mm pitch; active area ca. 0.97mm x 0.55mm (0.4mm^2)

APPLICATIONS

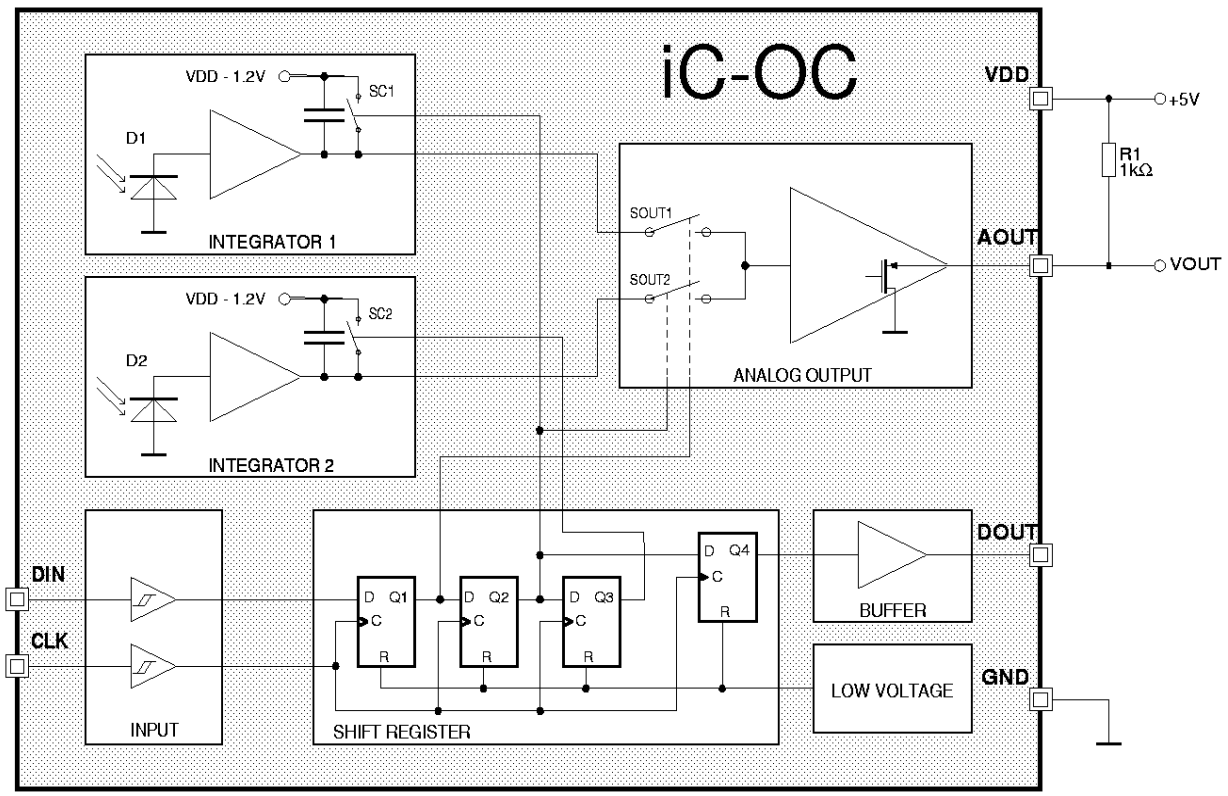
- Optical row sensors
- As substitutes for CCDs

PACKAGES



customized COB
(die size 1.7mm x 1.2mm)

BLOCK DIAGRAM



Rev A1

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DESCRIPTION

iC-OC is an optical sensor with two photodiodes, two integrating amplifiers and a control logic which enables several iC-OCs to be connected in a chain.

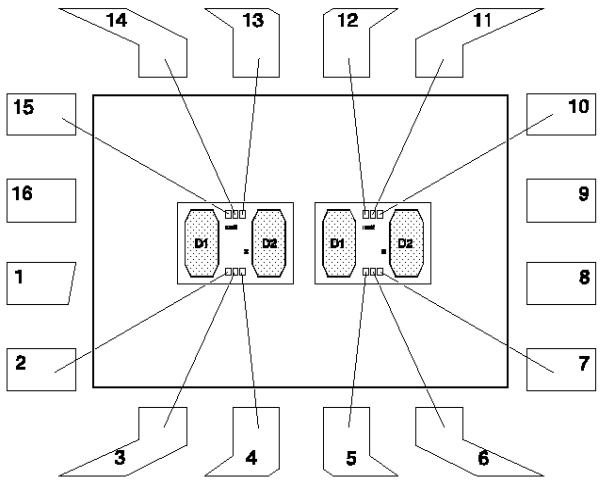
Furthermore, the control logic, consisting of a two-stage shift register, determines when the integration time starts and ends and switches the integrators in sequence to the analog output. The analog output is a source follower and in its deactivated state has a high impedance and can thus be used in buses.

The control logic output supplies a CMOS-compatible signal and in chain connection it can be directly linked to the digital input of the next device. Logic inputs are configured as Schmitt triggers and are TTL/CMOS-compatible.

All the registers in the device are reset with low voltage (power-down reset).
All pins are protected against ESD.

PACKAGES CDIP16 (for samples only)

PIN CONFIGURATION
(top view)



PIN FUNCTIONS

No.	Name	Function
1	n.c.	
2	DIN1	Input 1
3	CLK1	Clock 1
4	DOUT1	Digital Output 1
13	VDD1	+5V Supply Voltage
14	AOUT1	Analog Output 1
15	GND1	Ground
16	n.c.	
5	DIN2	Input 2
6	CLK2	Clock 2
7	DOUT2	Digital Output 2
8	n.c.	
9	n.c.	
10	VDD2	+5V Supply Voltage
11	AOUT2	Analog Output 2
12	GND2	Ground

ABSOLUTE MAXIMUM RATINGS

Values beyond which damage may occur; device operation is not guaranteed.

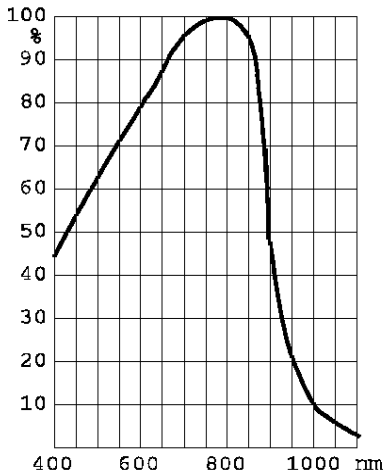
Item	Symbol	Parameter	Conditions	Fig.	Min.	Max.	Unit
G001	VDD	Supply Voltage			-0.3	6.5	V
G002	Ic()	Schutzdiodenstrom in DIN, CLK, DOUT, AOUT			-20	20	mA
G003	I()	Current in DOUT			-10	10	mA
G004	Ilu()	Pulse Current in all Pins (Latch-up strength)	pulse width ≤ 10µs		-100	100	mA
E001	Vd()	ESD-Susceptibility, at all Pins	MIL-STD-883, Method 3015, HBM 100pF discharged through 1.5kΩ			2	kV
TG1	Tj	Junction-Temperatur			-40	150	°C
TG2	Ts	Storage-Temperatur			-40	150	°C

THERMAL DATA

Operating Conditions: VDD= 5V ±10%

Item	Symbol	Parameter	Conditions	Fig.	Min.	Typ.	Max.	Unit
T1	Ta	Operating Ambient Temperature Range			0		70	°C

ELECTRICAL CHARACTERISTICS: Diagramms



Relative spectral sensitivity

All voltages are referenced to ground unless otherwise noted.
All currents into the device pins are positive; all currents out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions:
VDD= 5V ±10%, RL(VDD/AOUT)= 1kΩ, Tj= 0..85°C unless otherwise noted

Item	Symbol	Parameter	Conditions	Tj °C	Fig.	Min.	Typ.	Max.	Unit
Total Device									
001	VDD	Permissible Supply Voltage Range				4.5		5.5	V
002	I(VDD)	Supply Current in VDD				100		700	µA
003	Vc()hi	Clamp Voltage hi at DIN, CLK, DOUT, AOUT	Vc()hi= V() -VDD, I()= 10mA other Pins open			0.3		1.5	V
004	Vc()lo	Clamp Voltage lo at DIN, CLK, DOUT, AOUT	I()= -10mA, other Pins open			-1.5		-0.3	V
Analog Output AOUT									
201	V0()	Output Voltage at no illuminance	V0()= VDD -V(AOUT)max, AOUT active (* see below)			0.8		1.5	V
202	ΔV0()	Variation of Output Voltage at no illuminance	ΔV0()= V(AOUT)t1 -V(AOUT)t2, Δt= t2 -t1= 1ms					50	mV
203	Vlin()	Range of Linearity for Output Voltage	Vlin()= VDD -V0() -V(AOUT)			1.6			V
204	K	Transfer Factor Output voltage - Light Power					0.4		V/ pWs
205	ΔKlin	Transfer Factor Deviation within Linearity Range						5	%
206	I()	Leakage Current	V(AOUT)= 0..VDD, AOUT high impedance (* see below)			-5		5	µA
Shift-Register Inputs DIN, CLK									
301	Vt()hi	Threshold Voltage hi at DIN, CLK				1.4		2.2	V
302	Vt()lo	Threshold Voltage lo at DIN, CLK				0.8		1.3	V
303	Vt()hys	Hysteresis at DIN, CLK	Vt()hys= Vt()hi -Vt()lo			300		1300	mV
304	Ii()	Input Current in DIN, CLK	V()= 0..VDD			-1		1	µA
305	f()	Permissible Frequency at CLK						10	MHz
306	tw()hi	Permis. Pulse Width hi at CLK				20			ns
307	tw()lo	Permis. Pulse Width lo at CLK				20			ns
308	tplh	Propagation Delay: CLK hi→lo until DOUT lo→hi	CL(DOUT)= 50pF		2			40	ns
309	tphl	Propagation Delay: CLK hi→lo until DOUT hi→lo	CL(DOUT)= 50pF		2			40	ns
310	tpon	Propagation Delay: CLK lo→hi until AOUT active	CL(VDD/AOUT)= 1nF		2			800	ns
311	tpoff	Propagation Delay: CLK lo→hi until AOUT high impedance	CL(VDD/AOUT)= 1nF		2			100	ns
Buffer DOUT									
312	Vs()hi	Saturation Voltage hi	Vs()hi= VDD -V(), I()= -1mA					0.4	V
314	Vs()lo	Saturation Voltage lo	I()= 1mA					0.4	V
Low Voltage Detection									
401	VDDon	Turn-on Threshold VDD	increasing voltage at VDD			2.3		3.8	V
402	VDDoff	Undervoltage Threshold VDD	decreasing voltage at VDD			1.2		1.9	V
403	VDDhys	Hysteresis	VDDhys= VDDon -VDDoff			0.8		2	V

(*) AOUT active: SOUT1 or SOUT2 closed; AOUT high impedance: SOUT1 and SOUT2 open.

OPERATING REQUIREMENTS: Logic

Operating Conditions: VDD= 5V ±10%, Ta= 0..70°C,
input levels lo= 0..0.45V, hi= 2.4V..VDD, see Fig. 1 for reference levels

Item	Symbol	Parameter	Conditions	Fig.	Min.	Max.	Unit
I1	tset	Setup time: DIN stable before CLK lo→hi		2	10		ns
I2	thold	Hold time: DIN stable after CLK lo→hi		2	5		ns

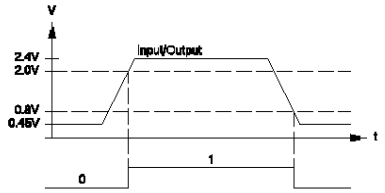


Fig. 1: Reference levels

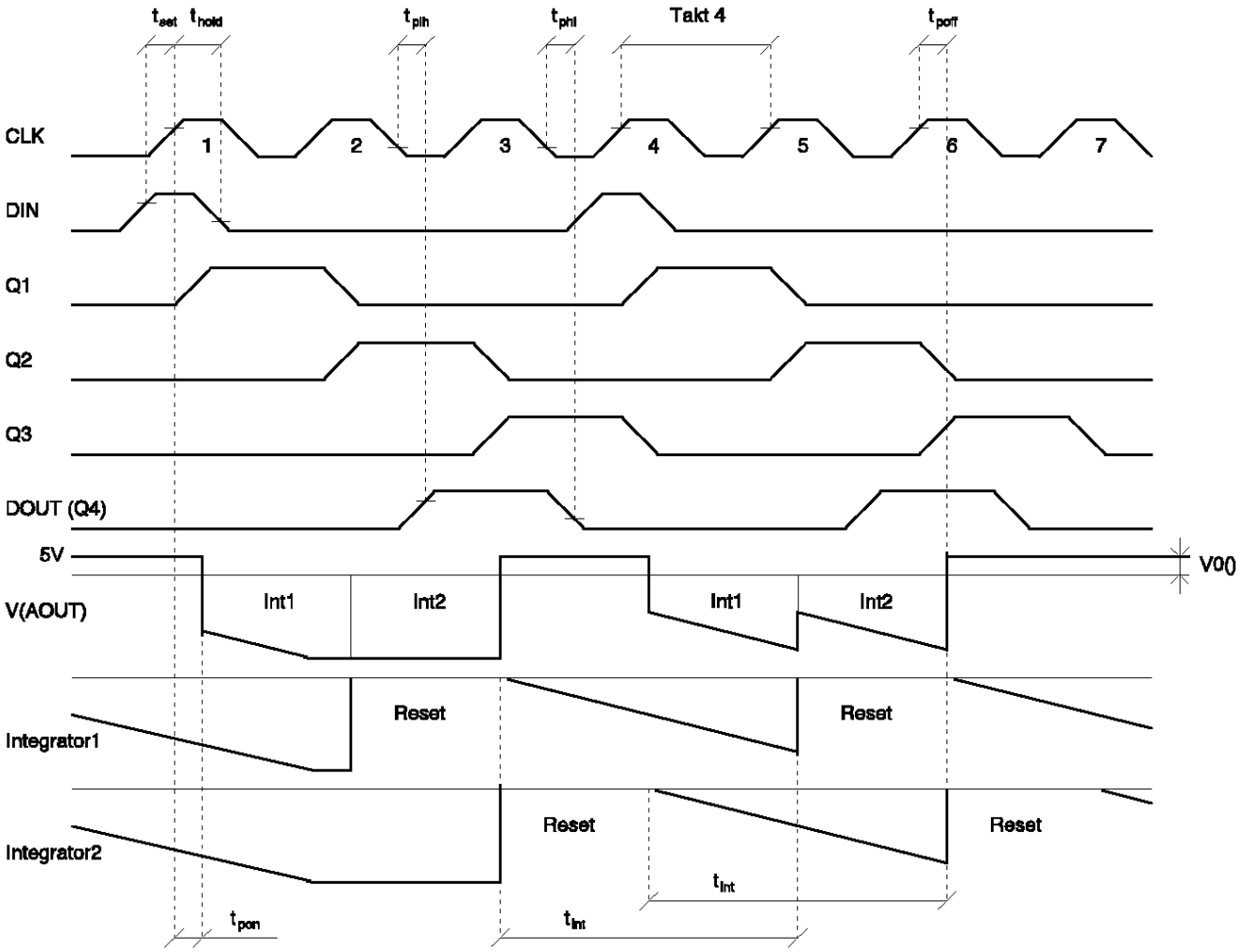


Fig. 2: Timing characteristics after power on (assumption: V0()1= V0()2= V0(), VDD= 5V)

DESCRIPTION OF FUNCTIONS

iC-OC is an integrating light-voltage converter with two separate photodiodes and two integrators. The integration time starts when the supply voltage is applied. To obtain a specified integration time a hi pulse must first be available at the digital input DIN and clocked by the device. This process sequentially resets the integrators to their initial value and restarts the integration time with the next clock pulse.

Flip-flops Q1 to Q3 sequentially accept the signal at DIN with the positive CLK edge. Flip-flop Q4, which controls the DOUT output signal, reacts to the negative CLK edge. The switching states in the IC always remain for the duration of a clock cycle. The process depicted in Fig. 2 is initiated when a hi pulse is applied to DIN.

During the first clock cycle integrator 1 is switched to the analog output AOUT (switch SOUT1 closes). AOUT initially supplies a voltage value which cannot be reproduced as the integration time is unknown. The second clock cycle switches the analog output from integrator 1 to integrator 2 (SOUT1 opens, SOUT2 closes). A non-reproducible voltage value is again present at AOUT (see above). At the same time the integration capacity of integrator 1 is short-circuited by switch SC1 (reset).

Flip-flop Q4 is set in the second clock cycle with the negative clock edge (DOUT1) and thus the DIN signal for the next device in the chain is produced.

During the third clock cycle integrator 2 is disconnected from AOUT (SOUT2 opens) and reset (SC2 closes). Simultaneously, the integration time for integrator 1 starts anew (SC1 opens). If several iC-OCs are connected in a chain, then the hi signal from DOUT is shifted into the first flip-flop of the next device with the third clock cycle.
During the fourth clock cycle switch SC2 opens and starts the integration time for integrator 2.

APPLICATIONS INFORMATION

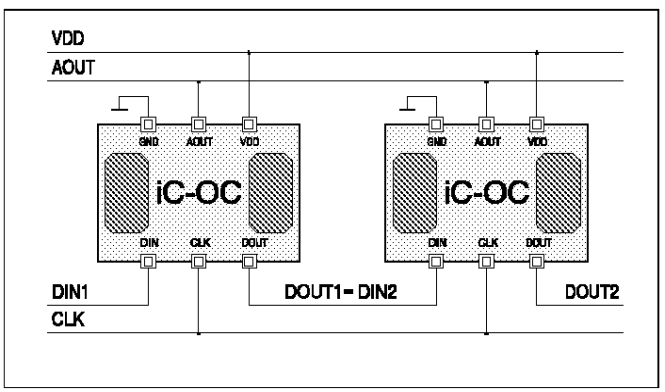


Fig. 3: Example of a chain connection for two devices

Only when the DOUT2 output has a hi level can the next hi signal be applied to DIN1. The first hi signal clocked by the device implements a sequential reset of the integrators, followed by the integration time starting in sequence.

The second hi signal shifted through the register determines the end of the integration time and restarts the integration time after a reset. The integrators can be read out with the aid of a sample and hold circuit, as the device itself has no hold mode.

Besides the clock a periodic signal at DIN is also necessary for the continuous operation of the device.

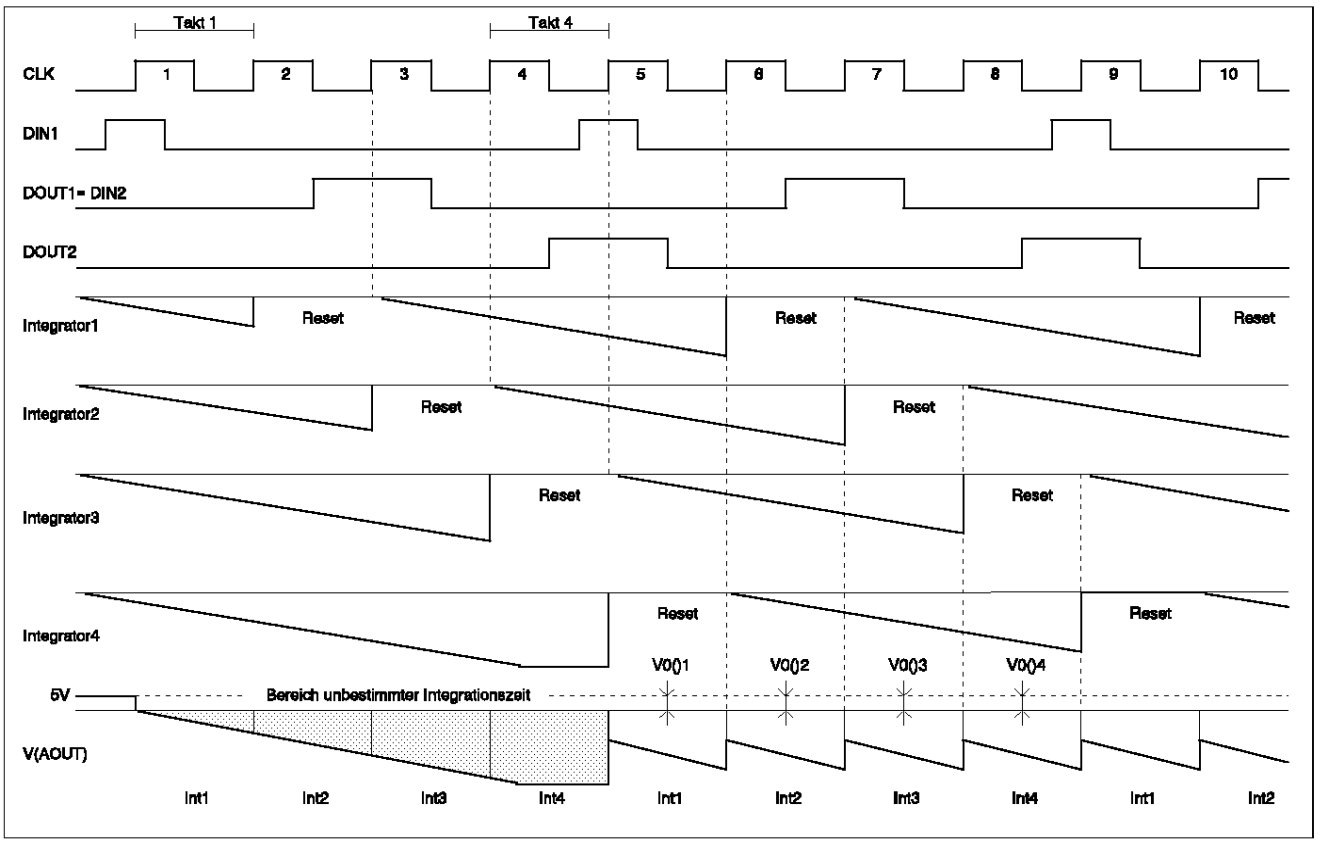


Fig. 4: Time sequence for the chain connection in Fig. 3 after the device has been switched on

With operation of the device at low level illumination the output voltage V(AOUT) decreases by V0(AOUT). When calibrating, this drop in voltage must be determined for each of the photosensors.

ORDERING INFORMATION

Type	Package	Order designation
iC-OC	CDIP16	iC-OC-CDIP16
OC Demo-Board		OC Demo-Board

For information about prices, terms of delivery, options for other case types, etc., please contact:

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