



# 128Kx32 3.3V SRAM MODULE PRELIMINARY\*

## FEATURES

- Access Times of 15\*\*, 17, 20, 25, 35ns
- MIL-STD-883 Compliant Devices Available
- Low Voltage Operation
- Packaging
  - 66-pin, PGA Type, 1.075 inch square Hermetic Ceramic HIP (Package 400)
  - 68 lead, 40mm, Hermetic CQFP (Package 501)
  - 68 lead, Hermetic CQFP (G2), 22mm (0.880 inch) square (Package 500). Designed to fit JEDEC 68 lead 0.990" CQFJ footprint (Fig. 3)
- Organized as 128Kx32; User Configurable as 256Kx16 or 512Kx8
- Commercial, Industrial and Military Temperature Ranges
- 3.3 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
  - WS128K32V-XG2X - 8 grams typical
  - WS128K32V-XH1X - 13 grams typical
  - WS128K32V-XG4X - 20 grams typical

\* This data sheet describes a product under development, not fully characterized, and is subject to change without notice.

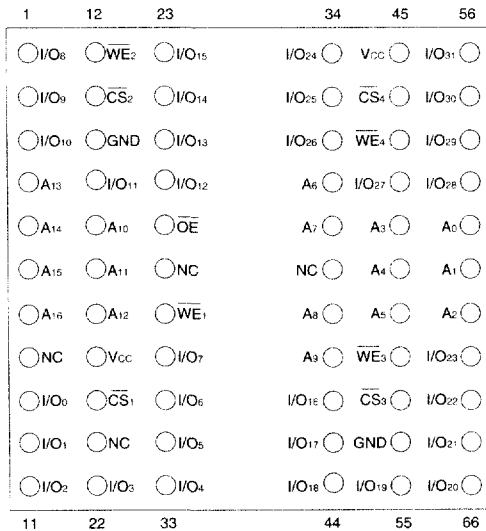
\*\* Commercial and Industrial only.

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### FIG. 1 PIN CONFIGURATION FOR WS128K32NV-XH1X

TOP VIEW



PIN DESCRIPTION

I/O <sub>0-31</sub>	Data Inputs/Outputs
A <sub>0-16</sub>	Address Inputs
WE <sub>1-4</sub>	Write Enables
CS <sub>1-4</sub>	Chip Selects
OE	Output Enable
V <sub>CC</sub>	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM

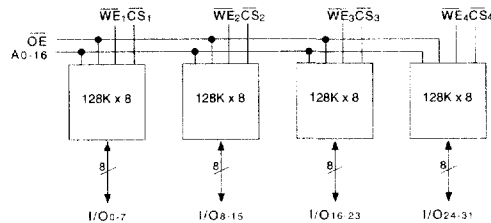
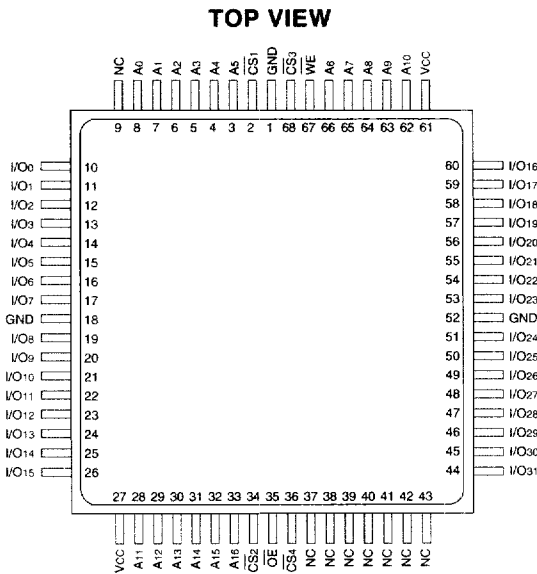




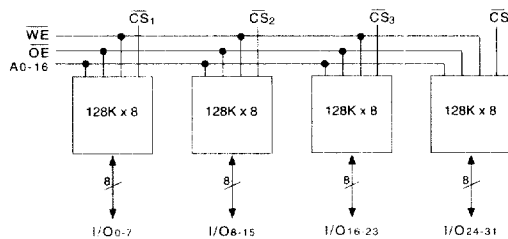
FIG. 2 PIN CONFIGURATION FOR WS128K32V-XG4X



**PIN DESCRIPTION**

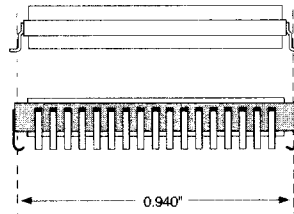
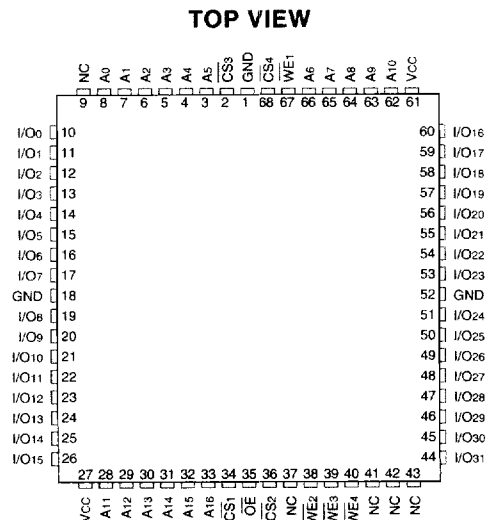
I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected

**BLOCK DIAGRAM**



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FIG. 3 PIN CONFIGURATION FOR WS128K32V-XG2X

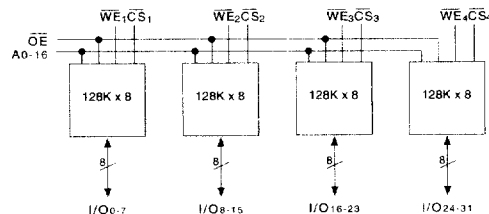


The White 68 lead G2 CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2 has the TCE and lead inspection advantage of the CQFP form.

**PIN DESCRIPTION**

I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected

**BLOCK DIAGRAM**





**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T <sub>A</sub>	-55	+125	°C
Storage Temperature	T <sub>STG</sub>	-65	+150	°C
Signal Voltage Relative to GND	V <sub>I</sub>	-0.5	4.6	V
Junction Temperature	T <sub>J</sub>		150	°C
Supply Voltage	V <sub>CC</sub>	-0.5	5.5	V

**TRUTH TABLE**

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V <sub>CC</sub>	3.0	3.6	V
Input High Voltage	V <sub>IH</sub>	2.2	V <sub>CC</sub> + 0.3	V
Input Low Voltage	V <sub>IL</sub>	-0.3	+0.8	V

**CAPACITANCE**

(T<sub>A</sub> = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C <sub>OE</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	50	pF
$\overline{WE}$ 1-4 capacitance HIP (PGA)	C <sub>WE</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	20	pF
CQFP G4			50	
CQFP G2			20	
$\overline{CS}$ 1-4 capacitance	C <sub>CS</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C <sub>AD</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

**DC CHARACTERISTICS**

(V<sub>CC</sub> = 3.3V ±0.3V, V<sub>SS</sub> = 0V, T<sub>A</sub> = -55°C to +125°C)

Parameter	Sym	Conditions	Min		Units
				Max	
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> = GND to V <sub>CC</sub>		10	μA
Output Leakage Current	I <sub>LO</sub>	$\overline{CS}$ = V <sub>IH</sub> , $\overline{OE}$ = V <sub>IH</sub> , V <sub>OUT</sub> = GND to V <sub>CC</sub>		10	μA
Operating Supply Current (x 32 Mode)	I <sub>CC</sub> x 32	$\overline{CS}$ = V <sub>IL</sub> , $\overline{OE}$ = V <sub>IH</sub> , f = 5MHz		500	mA
Standby Current	I <sub>SB</sub>	$\overline{CS}$ = V <sub>IH</sub> , $\overline{OE}$ = V <sub>IH</sub> , f = 5MHz		32	mA
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8mA		0.4	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4.0mA	2.4		V



AC CHARACTERISTICS
(VCC = 3.3V, TA = -55°C to +125°C)

Table with 12 columns: Parameter, Symbol, -15\* (Min, Max), -17 (Min, Max), -20 (Min, Max), -25 (Min, Max), -35 (Min, Max), Units. Rows include Read Cycle Time, Address Access Time, Output Hold from Address Change, etc.

1. This parameter is guaranteed by design but not tested.

\* Commercial and Industrial only.

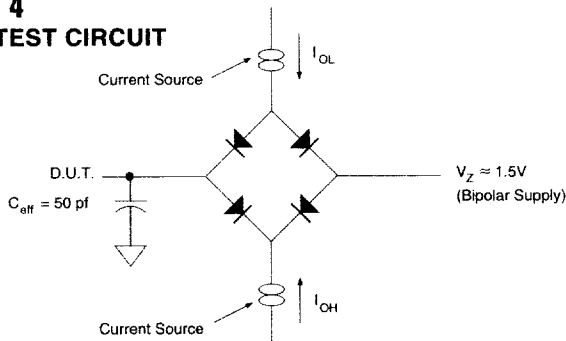
AC CHARACTERISTICS
(VCC = 3.3V, TA = -55°C to +125°C)

Table with 12 columns: Parameter, Symbol, -15\* (Min, Max), -17 (Min, Max), -20 (Min, Max), -25 (Min, Max), -35 (Min, Max), Units. Rows include Write Cycle Time, Chip Select to End of Write, Address Valid to End of Write, etc.

1. This parameter is guaranteed by design but not tested.

\* Commercial and Industrial only.

FIG. 4
AC TEST CIRCUIT



AC TEST CONDITIONS

Table with 3 columns: Parameter, Typ, Unit. Rows include Input Pulse Levels, Input Rise and Fall, Input and Output Reference Level, Output Timing Reference Level.

NOTES:

Vz is programmable from -2V to +7V.
IOL & IOH programmable from 0 to 16mA.
Tester Impedance Zo = 75 Ohm.
Vz is typically the midpoint of VOH and VOL.
IOL & IOH are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.



ORDERING INFORMATION

W S 128K 32 X V - XXX X X X

LEAD FINISH:

Blank = Gold plated leads

A = Solder dip leads

DEVICE GRADE:

M = Military Screened -55°C to +125°C

I = Industrial -40°C to +85°C

C = Commercial 0°C to +70°C

PACKAGE TYPE:

H1 = Ceramic Hex-In-line Package, HIP (Package 400)

G2 = 22 mm Ceramic Quad Flat Pack, CQFP (Package 500)

G4 = 40 mm Ceramic Quad Flat Pack, CQFP (Package 501)

ACCESS TIME (ns)

Low Voltage Supply 3.3V ± 10%

IMPROVEMENT MARK:

N = No Connect at pins 8, 21, 28, 39 in HIP for upgrade.

ORGANIZATION, 128Kx32

User configurable as 256Kx16 or 512Kx8

SRAM

WHITE MICROELECTRONICS

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