ALPHA SEMICONDUCTOR
Excellence in Analog Power Products

AS OP-77

Ultra Low Offset Voltage Operational Amplifier

FEATURES

- Low offset Vos 25μV max.....
- Low drift vs. temperature:..... 0.3μV/°C
- High CMMR ... . 1.0 mV/VMax
- High PSRR..... .....3 μV/V Min
- Low power ....60 mW Max
- High gain..... ..... 5,000,000 V/mV Min
- Direct replacement for OP-07,725, 108A/308A, 741 sockets

APPLICATIONS

- Sampling & Hold Amplifiers
- Integrators
- Medical Instrumentation
- Strain Gauge & Thermocouple
- Precision Absolute Value Circuits

PRODUCT DESCRIPTION

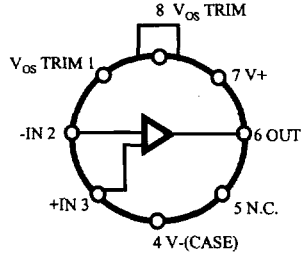
The ALPHA Semiconductor AS OP-77 is the next generation of OP-07. The OP-77 offers very high open-loop gain of 10,000,000 over the full ±10V output range. The low initial offset drift with the low power dissipation of 50 mW makes OP-77 a significant improvement over the similar, previous operational amplifiers. PSRR of 3μV/V (110 dB) and CMRR of 1.0μV/V maximum, virtually eliminates errors caused by power supply drift and common-mode signal.

The OP-77 is available in several different grades. The AS OP-77 is available in hermetically sealed TO-99 metal can, plastic DIP 8-pin and 8-pin plastic SOIC packages. The operating temperature is 0°C to 70°C and -55°C to +125°C. The AS OP-77 is a direct replacement for the OP-07, 05, 725, or 108A OP amps.

ORDERING INFORMATION

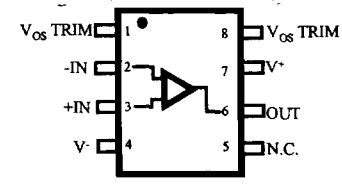
TO-99 8-PIN	PLASTIC DIP 8-PIN	PLASTIC SOIC 8-PIN	TA=25°C V_{OS} Max (mv)	Oper. Temp. Range
OP77AJ			25	MIL.
OP77EJ			25	IND
OP77BJ			60	MIL.
OP77FJ			60	IND
	OP77FP	OP77FS	60	COM
	OP77GP	OP77GS	100	COM.

PIN CONNECTIONS



Bottom View

8-Pin Surface Mount
8-Pin MINI-DIP



Top View

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage ..... ±22V
Internal Power Dissipation (Note 1) 500mW
Differential Input Voltage ..... ±30V
Input Voltage (Note 2) ..... ±22V
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range
J Package ..... -65 to +150°C
P and SO Packages ..... -65 to +125°C
Operating Temperature Range
OP77A, OP77B (J) ..... -55 to +125°C
OP77E, OP77F (J) ..... -40 to +85°C
OP77F, OP77G(P,S) ..... 0 to +70°C
Dice Junction Temperature(Tj) ..... -65 to +150°C
Lead Temperature (Soldering, 60 Sec.) ..... 300°C

NOTES:
1. See Table for maximum ambient temperature rating and derating factor.
2. Absolute maximum ratings apply to both DICE and packaged parts unless otherwise noted.
3. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99(J)	80°C	7.1 mW/°C
9-Pin Plastic DIP (P)	36°C	5.6 mW/°C
8 pin SOIC	36°C	5.6 mW/°C

ELECTRICAL CHARACTERISTICS at V_S=±15V, Ta=25°C, unless otherwise specified.

Parameter	Symbol	Conditions	OP-77A			OP-77B			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage	V_{os}			10	25		20	60	µV
Long-Term Input Offset Voltage Stability	V_{OS}/Time	(Note 1)		0.2			0.2		µV/M_o
Input Offset Current	I_{os}			0.3	1.5		0.3	2.8	nA
Input Bias Current	I_B		0.2	1.2	2.0	0.2	1.2	2.8	nA
Input Noise Voltage (Note 2)	e_{npp}	0.1Hz to10Hz		0.35	0.6		0.35	0.6	μV_{p-p}
Input Noise Current (Note 2)	$i_{np\,p}$	0.1 Hz to 10Hz		14	30		14	30	pA_{p-p}
Input Resistance-Differential-Mode	R_{in}	(Note 3)	26	45		18.5	45		MΩ
Input Resistance-Common-Mode	R_{inCM}			200			200		GΩ
Input Voltage Range	IVR		±13	±14		±13	±14		V
Common-Mode Rejection Ratio	CMRR	V_{CM}=±13.0		0.1	1.0		0.1	1.6	µV/V
Power Supply Rejection Ratio	PSRR	V_S=±3V to ±18		0.7	3		0.7	3	µV/V
Large-Signal Voltage Gain	AV_O	R_l ≥2kΩ, V_o=±10V	5000	12000		2000	8000		V/mV
Output Voltage Swing	V_o	Rl ≥10kΩ	±13.5	±14.0		±13.5	±14.0		V
Output Voltage Swing	V_o	Rl ≥ 2kΩ	±12.5	±13.0		±12.5	±13.0		V
Output Voltage Swing	V_o	Rl ≥1kΩ	±12.0	±12.5		±12.0	±12.5		V
Slew Rate	SR	Rl ≥ 2kΩ	0.1	0.3		0.1	0.3		V/µs
Closed-Loop Bandwidth	BW	A_{vcl}=+1.0(Note 1)	0.4	0.6		0.4	0.6		MHz
Open-Loop Output Resistance	R_o	V_o=0, Io=0		60			60		Ω
Power Consumption	P_d	Vs=±15V, No Load		50	60		50	60	mW
Power Consumption	P_d	V_s=±3V, No load		3.5	4.5		3.5	4.5	mW
Offset Adjustment Range		R_p=20kΩ		+3			+3		mV

Notes:
1. Long term input offset voltage stability refers to the averaged trend line of Vos Vs. time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in Vos during the first 30 operating days are typically. 2.5 mV.
2. Sample tested
3. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at V_S=±15V, Ta=25°C, unless otherwise specified.

Parameter	Symbol	Conditions	OP-77E			OP-77F			OP-77G			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage	V_{os}			10	25		20	60		50	100	μV
Long-Term V_{os} Stability	V_{OS}/Time	(Note 1)		0.3			0.4			0.4		$\mu V/M_o$
Input Offset Current	I_{os}			0.3	1.5		0.3	2.8		0.3	2.8	nA
Input Bias Current	I_B		0.2	1.2	2.0	0.2	1.2	2.8	0.2	1.2	2.8	nA
Input Noise Voltage (Note 2)	e_{npp}	0.1Hz to10Hz		0.35	0.6		0.38	0.65		0.38	0.65	μV_{P-P}
Input Noise Current (Note 2)	$i_{np\ p}$	0.1 Hz to 10Hz		14	30		15	35		15	35	pA_{P-P}
Input Resistance-Differential-Mode	R_{in}	(Note 3)	26	45		18.5	45		18.5	45		MΩ
Input Resistance-Common-Mode	R_{inCM}			200			200			200		GΩ
Input Voltage Range	IVR		±13	±14		±13	±14		±13	±14		V
Common-Mode Rejection Ratio	CMRR	V_{CM}=±13.0		0.1	1.0		0.1	1.6		0.1	1.6	μV/V
Power Supply Rejection Ratio	PSRR	V_S=±3V to ±18		0.7	3.0		0.7	3.0		0.7	3.0	μV/V
Large-Signal Voltage Gain	AV_O	R_l ≥2kΩ, V_o=±10V	5000	12000		5000	6000		2000	6000		V/mV
Output Voltage Swing	V_o	Rl ≥10kΩ	±13.5	±14.0		±13.5	±14.0		±13.5	±14.0		V
Output Voltage Swing	V_o	Rl ≥ 2kΩ	12.5	±13.0		±12.5	±13.0		±12.5	±13.0		V
Output Voltage Swing	V_o	Rl ≥1kΩ	±12.0	±12.5		±12.0	±12.5		±12.0	±12.5		V
Slewing Rate	SR	Rl ≥ 2kΩ	0.1	0.3		0.1	0.3		0.1	0.3		V/μs
Closed-Loop Bandwidth	BW	A_{vcl}=+1.0(Note 1)	0.4	0.6		0.4	0.6		0.4	0.6		MHz
Open-Loop Output Resistance	R_o	V_o=0, Io=0		60			60			60		Ω
Power Consumption	P_d	Vs=±15V, No Load		50	60		50	60		50	60	mW
Power Consumption	P_d	V_S=±3V, No load		3.5	4.5		3.5	4.5		3.5	4.5	mW
Offset Adjustment Range		R_p=20kΩ		±3			±3			±3		mV

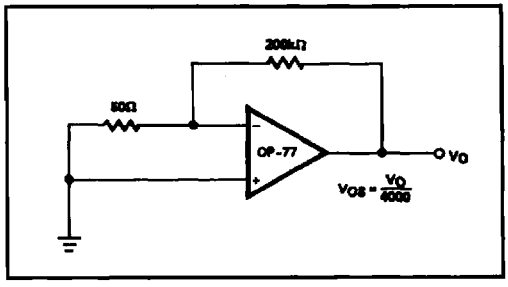
Notes:

.1. Long term input offset voltage stability refers to the averaged trend line of Vos Vs. time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in Vos during the first 30 operating days are typically 2.5 mV.

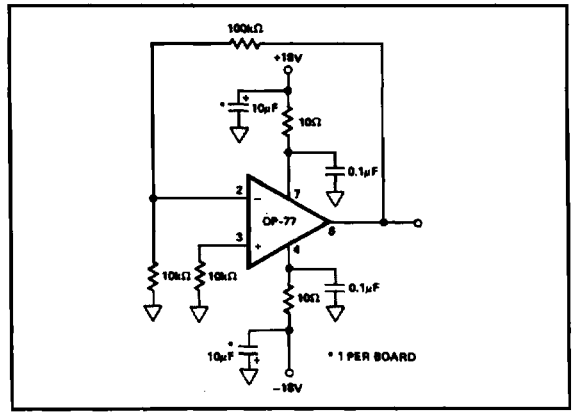
2. Sample tested

3. Guaranteed by design.

OFFSET VOLTAGE TEST CIRCUIT



BURN-IN CIRCUIT



ELECTRICAL CHARACTERISTICS at V_S=±15V, -55°C≤Ta≤+125°C, unless otherwise specified.

Parameter	Symbol	Conditions	OP-77A			OP-77B			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage	V_{os}			25	60		45	120	µV
Average Input Offset Voltage Drift	TCV_{os}	(Note 1)		0.1	0.3		0.2	0.6	µV/°C µV/°C
Input Offset Current	I_{os}			0.5	2.2		0.5	4.5	nA
Average Input Offset Current Drift	TCI_{os}	Note 2		1.5	2.5		1.5	50	pA/°C
Input Bias Current	I_B		0.2	2.4	4.0	0.2	2.4	6.0	nA
Average Input Bias Current Drift	TCI_B	Note 2		8	25		15	35	pA/°C
Input Voltage Range	IVR		±13	±13.5		±13	±13.5		V
Common-Mode Rejection Ratio	CMRR	V_{CM} ±13.0 V		0.1	1.0		1.0	3	µV/V
Power Supply Rejection Ratio	PSRR	V_s=±3V to ±18V		1	3		1	5	µV/V
Large-Signal Voltage Gain	A_{vo}	R_l ≥2Ω, V_o= ±10V	2080	6000		1000	4000		V/mV
Output Voltage Swing	V_o	R_l ≥2Ω	±12	±13.0		±12	±13.0		V
Power Consumption	P_d	V_s ' 15kV, No Load		60	75		60	75	mW

Notes:
1. OP-77; TCVos is 100% tested.
2. Guaranteed by end point limits.

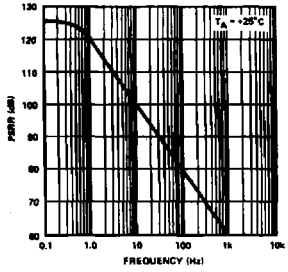
ELECTRICAL CHARACTERISTICS at V_S=±15V, -25°C≤Ta≤+85°C, for OP-77/FJ, 0°C≤Ta≤+70°C for OP-77/F/GP and OP-77 /F/GS unless otherwise specified.

Parameter	Symbol	Conditions	OP-77E			OP-77F			OP-77G			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage	V_{os}	J Package P Package		10 10	45 55		20 20	100 100		80	150	µV/V
Average Input Offset Voltage	TCV_{os}	J Package P Package		0.1 0.3	0.3 0.6		0.2 0.4	0.6 1.0				µV/°C µV/°C
Input Offset Current	I_{os}			0.5	2.2		0.5	4.5		0.5	4.5	nA
Average Input Offset Current Drift	TCI_{os}	(Note 2)		1.5	4.0		1.5	80		1.5	85	pA/°C
Input Bias Current	I_B		0.2	2.4	4.0	0.2	2.4	4.0	0.2	2.4	6.0	nA
Average Input Bias Current Drift	TCI_B	Note 2		8	40		15	60		15	60	pA/°C
Input Voltage Range	IVR		±13	±13.5		±13	±13.5		±13.0	±13.5		V
Common Mode Rejection Ratio	CMRR	V_{CM} ±13.0 V		0.1	1.0		0.1	3.0		0.1	3.0	µV/V
Power Supply Rejection Ratio	PSRR	V_s=±3V to ±18V		1.0	3.0		1.0	5.0		1.0	5.0	µV/V
Large-Signal Voltage Gain	A_{vo}	R_l ≥2Ω, V_o= ±10V	2000	6000		2000	6000		1000	4000		V/mV
Output Voltage Swing	V_o	R_l ≥2Ω	±12	±13.0		±12	±13.0		±12	±13.0		V
Power Consumption	P_d	V_s ' 15kV, No Load		60	75		60	75		60	75	mW

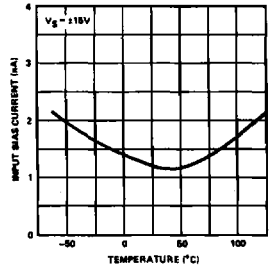
Notes:
1. OP-77; TCVos is 100% tested on J packages
2. Guaranteed by end point limits.

TYPICAL PERFORMANCE

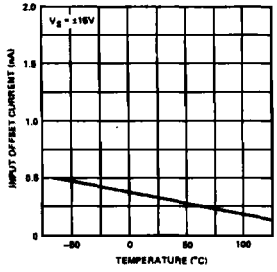
PSRR vs FREQUENCY



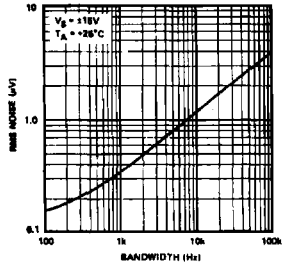
INPUT BIAS CURRENT vs TEMPERATURE



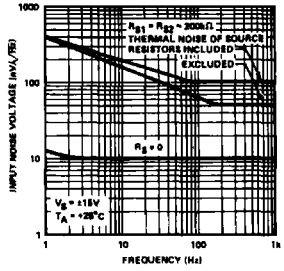
INPUT OFFSET CURRENT vs TEMPERATURE



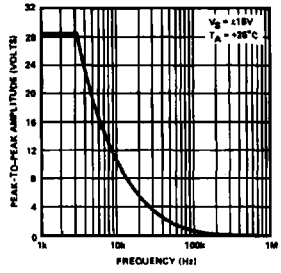
INPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



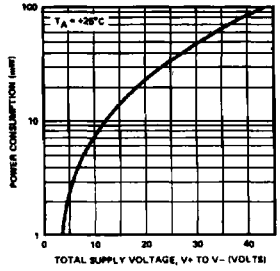
TOTAL INPUT NOISE VOLTAGE vs FREQUENCY



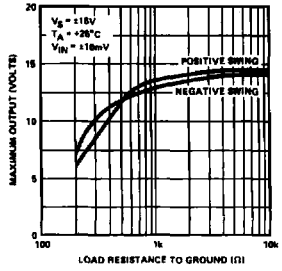
MAXIMUM OUTPUT SWING vs FREQUENCY



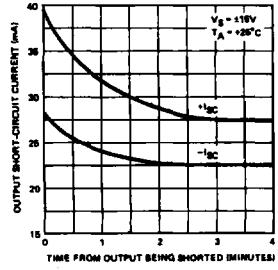
POWER CONSUMPTION vs POWER SUPPLY



MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE

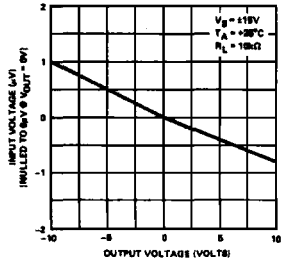


OUTPUT SHORT-CIRCUIT CURRENT vs TIME

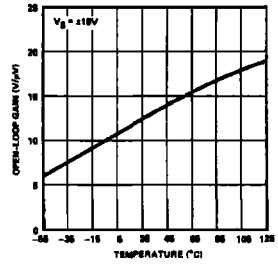


TYPICAL PERFORMANCE (continued)

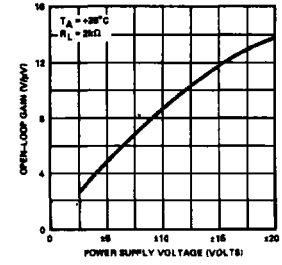
GAIN LINEARITY (INPUT VOLTAGE vs OUTPUT VOLTAGE)



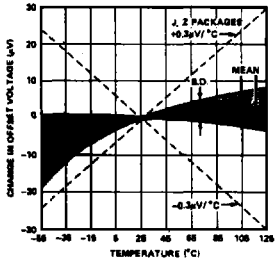
OPEN-LOOP GAIN vs TEMPERATURE



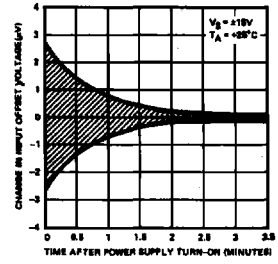
OPEN-LOOP GAIN vs POWER SUPPLY VOLTAGE



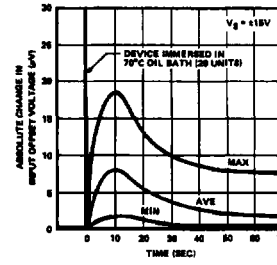
UNTRIMMED OFFSET VOLTAGE vs TEMPERATURE



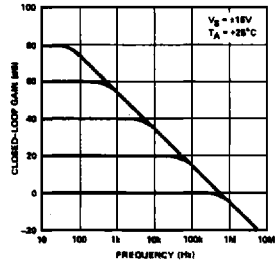
WARM-UP DRIFT



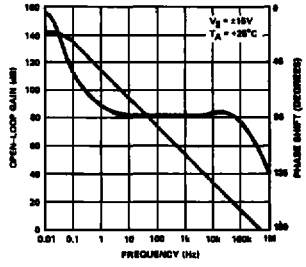
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



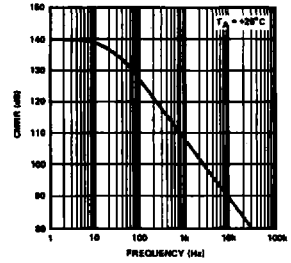
CLOSED-LOOP RESPONSE FOR VARIOUS GAIN CONFIGURATIONS



OPEN-LOOP GAIN/PHASE RESPONSE

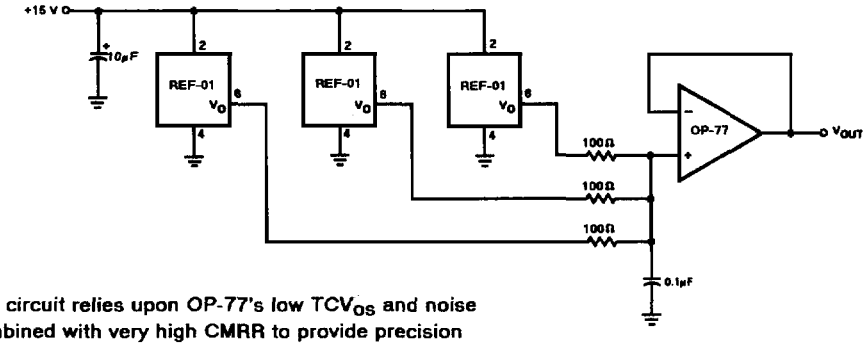


CMRR vs FREQUENCY



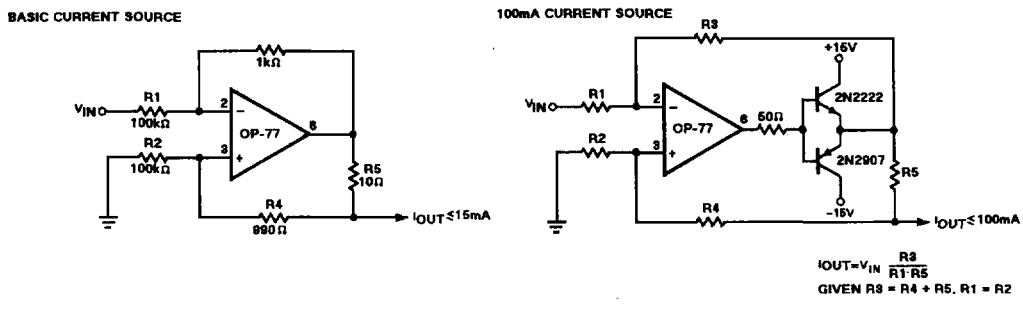
TYPICAL APPLICATIONS

LOW NOISE PRECISION REFERENCE



This circuit relies upon OP-77's low TCV_{OS} and noise combined with very high CMRR to provide precision buffering of the averaged REF-01 voltage outputs.

BILATERAL CURRENT SOURCE



These current sources will supply both positive and negative current into a grounded load.

Note that $Z_O = \dfrac{R5\left(\dfrac{R4}{R2}+1\right)}{\dfrac{R5+R4}{R2} - \dfrac{R3}{R1}}$ and that for Z_O to be infinite, $\dfrac{R5+R4}{R2}$ must $= \dfrac{R3}{R1}$