Precision Picoampere Input Current Quad Operational Amplifier

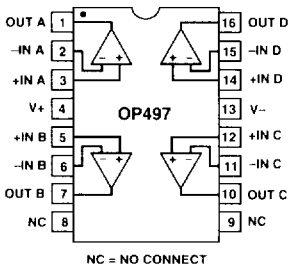
OP497

FEATURES
- Low Offset Voltage: 50 μV max
- Low Offset Voltage Drift: 0.5 μV/°C max
- Very Low Bias Current
  - +25°C: 100 pA max
  - −55°C to +125°C: 450 pA max
- Very High Open-Loop Gain: 2000 V/mV min
- Low Supply Current (per Amplifier): 625 μA max
- Operates from ±2 V to ±20 V Supplies
- High Common-Mode Rejection: 120 dB min

APPLICATIONS
- Strain Gage and Bridge Amplifiers
- High Stability Thermocouple Amplifiers
- Instrumentation Amplifiers
- Photo-Current Monitors
- High Gain Linearity Amplifiers
- Long-Term Integrators/Filters
- Sample-and-Hold Amplifiers
- Peak Detectors
- Logarithmic Amplifiers
- Battery-Powered Systems

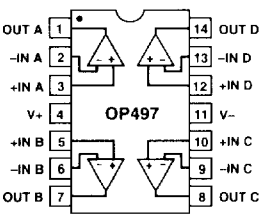
PIN CONNECTIONS

16-Lead Wide Body SOIC
(S Suffix)

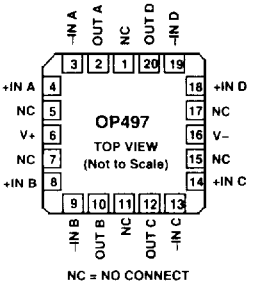


NC = NO CONNECT

14-Lead Plastic DIP
(P Suffix)
14-Lead Ceramic DIP
(Y Suffix)



20-Position Chip Carrier
(RC Suffix)



NC = NO CONNECT

GENERAL DESCRIPTION

The OP497 is a quad op amp with precision performance in the space saving, industry standard 16-pin SOIC package. Its combination of exceptional precision with low power and extremely low input bias current makes the quad OP497 useful in a wide variety of applications.

Precision performance of the OP497 includes very low offset, under 50 μV, and low drift, below 0.5 μV/°C. Open-loop gain exceeds 2000 V/mV insuring high linearity in every application. Errors due to common-mode signals are eliminated by the OP497's common-mode rejection of over 120 dB. The OP497's power supply rejection of over 120 dB minimizes offset voltage changes experienced in battery powered systems. Supply current of the OP497 is under 625 μA per amplifier, and it can operate with supply voltages as low as ±2 V.

The OP497 utilizes a superbeta input stage with bias current cancellation to maintain picoamp bias currents at all temperatures. This is in contrast to FET input op amps whose bias currents start in the picoamp range at 25°C, but double for every 10°C rise in temperature, to reach the nanoamp range above 85°C. Input bias current of the OP497 is under 100 pA at 25°C and is under 450 pA over the military temperature range.

Combining precision, low power and low bias current, the OP497 is ideal for a number of applications including instrumentation amplifiers, log amplifiers, photodiode preamplifiers and long-term integrators. For a single device see the OP97, for a dual see the OP297.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
OP497AY	55°C to +125°C	14-Pin Cerdip	Q-14
OP497BY/883C	55°C to +125°C	14-Pin Cerdip	Q-14
OP497CY	−55°C to +125°C	14-Pin Cerdip	Q-14
OP497BRC/883	55°C to +125°C	20-Contact LCC	E-20A
OP497FY	40°C to +85°C	14-Pin Cerdip	Q-14
OP497FP	40°C to +85°C	14-Pin Plastic DIP	N-14
OP497FS	40°C to +85°C	16-Pin SOIC	R-16
OP497GP	40°C to +85°C	14-Pin Plastic DIP	N-14
OP497GS	40°C to +85°C	16-Pin SOIC	R-16
OP497GS-REEL	40°C to +85°C	16-Pin SOIC	R-16

*For outline information see Package Information section.

OP497–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Condition	A Min	A Typ	A Max	B/F Min	B/F Typ	B/F Max	C/G Min	C/G Typ	C/G Max	Units
INPUT CHARACTERISTICS												
Offset Voltage	V_{OS}			20	50		40	75		80	150	µV
		40°C < T_A < +85°C					70	150		120	250	
		55°C < T_A < +125°C		40	100		80	150		140	300	
Average Input Offset Voltage Drift	TCV_{OS}	T_{MIN} to T_{MAX}		0.2	0.5		0.4	1.0		0.6	1.5	µV/°C
Long Term Input Offset Voltage Stability				0.1			0.1			0.1		µV/Mo
Input Bias Current	I_B	V_{CM} = 0 V		30	100		40	150		60	200	pA
		40°C < T_A < +85°C					60	200		80	300	
		55°C < T_A < +125°C		80	450		110	600		130	600	
Average Input Bias Current Drift	TC_{IB}	40°C < T_A < +85°C					0.3			0.3		
		55°C < T_A < +125°C		0.5			0.7			0.7		pA/°C
Input Offset Current	I_{OS}	V_{CM} = 0 V		15	100		30	150		50	200	pA
		40°C < T_A < +85°C					50	200		80	300	
		55°C < T_A < +125°C		35	400		60	600		90	600	
Average Input Offset Current Drift	TC_{IOS}			0.2			0.3			0.4		pA/°C
Input Voltage Range[1]	IVR		±13	±14		±13	±14		±13	±14		V
		T_{MIN} to T_{MAX}	±13	±13.5		±13	±13.5		±13	±13.5		
Common-Mode Rejection	CMR	V_{CM} = ±13 V	120	140		114	135		114	135		dB
		T_{MIN} to T_{MAX}	114	130		108	120		108	120		
Large Signal Voltage Gain	A_{VO}	V_O = +10 V, R_L = 2 kΩ	2000	6000		1500	4000		1200	4000		V/mV
		–40°C ≤ T_A ≤ +85°C				800	2000		800	2000		
		–55°C ≤ T_A < +125°C	1200	4000		1000	3000		800	3000		
Input Resistance Differential Mode	R_{IN}			30			30			30		MΩ
Input Resistance Common Mode	R_{INCM}			500			500			500		GΩ
Input Capacitance	C_{IN}			3			3			3		pF
OUTPUT CHARACTERISTICS												
Output Voltage Swing	V_O	R_L = 2 kΩ	±13	±13.7		±13	±13.7		±13	±13.7		V
		R_L = 10 kΩ	±13	±14		±13	±14		±13	±14		
		T_{MIN} to T_{MAX}, R_L = 10 kΩ	±13	±13.5		±13	±13.5		±13	±13.5		
Short Circuit	I_{SC}			±25			±25			±25		mA
POWER SUPPLY												
Power Supply Rejection Ratio	PSRR	V_S = ±2 V to ±20 V	120	140		114	135		114	135		dB
		V_S = ±2.5 V to ±20 V										
		T_{MIN} to T_{MAX}	114	130		108	120		108	120		
Supply Current (per Amplifier)	I_{SY}	No Load		525	625		525	625		525	625	µA
		T_{MIN} to T_{MAX}		580	750		580	750		580	750	
Supply Voltage Range	V_S	Operating Range	±2		±20	±2		±20	±2		±20	V
		T_{MIN} to T_{MAX}	±2.5		±20	±2.5		±20	±2.5		±20	
DYNAMIC PERFORMANCE												
Slew Rate	SR		0.05	0.15		0.05	0.15		0.05	0.15		V/µs
Gain Bandwidth Product	GBW			500			500			500		kHz
Channel Separation	CS	V_O = 20 V p-p, f_O = 10 Hz		150			150			150		dB
NOISE PERFORMANCE												
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.3			0.3			0.3		µV p-p
Voltage Noise Density	e_n	= 10 Hz		17			17			17		nV/√Hz
	e_n	= 1 kHz		15			15			15		nV/√Hz
Current Noise Density	i_n	= 10 Hz		20			20			20		fA/√Hz

NOTES

[1]Guaranteed by CMR test.

Specifications subject to change without notice

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ..... ±20 V
Input Voltage[2] ..... ±20 V
Differential Input Voltage[2] ..... 40 V
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range
  Y, RC Package ..... –65°C to +175°C
  P, S Package ..... –65°C to +150°C
Operating Temperature Range
  OP497A, B, C (Y) ..... –55°C to +125°C
  OP497F, G (Y) ..... –40°C to +85°C
  OP497F, G (P, S) ..... –40°C to +85°C
Junction Temperature
  Y, RC Package ..... –65°C to +175°C
  P, S Package ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... +300°C

Package Type	θ_{JA}	θ_{JC}	Units
14-Pin Cerdip (Y)	94	10	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W
20-Contact LCC (RC)	78	33	°C/W
16-Pin SOIC (S)	92	23	°C/W