PA7128 PEEL™ Array
Programmable Electrically Erasable Logic Array

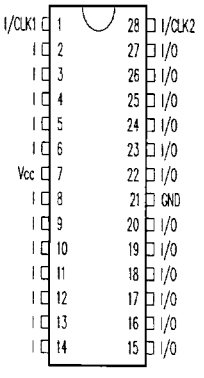
Features

- **CMOS Electrically Erasable Technology**
  - Reprogrammable in 28-pin DIP, SOIC, and PLCC packages
- **Versatile Logic Array Architecture**
  - 12 I/Os, 14 inputs, 36 registers/latches
  - Up to 36 logic cell output functions
  - PLA structure with true product-term sharing
  - Logic functions and registers can be I/O-buried
- **Flexible Logic Cell**
  - Up to 3 output functions per logic cell
  - D,T and JK registers with special features
  - Independent or global clocks, resets, presets, clock polarity, and output enables
  - Sum-of-products logic for output enables
- **High-Speed, Moderate Power Consumption**
  - As fast as 9ns/15ns (tpdi/tpdx), 83.3MHz fmax
  - ICC 95mA max, 75mA typical
- **Ideal for Combinatorial, Synchronous and Asynchronous Logic Applications**
  - Integration of multiple PLDs and random logic
  - Buried counters, complex state-machines
  - Comparitors, decoders, multiplexers and other wide-gate functions
- **Development and Programmer Support**
  - ICT PLACE Development Software
  - Fitters for ABEL and CUPL design software
  - Programming support by ICT PDS-3 and other popular third-party programmers

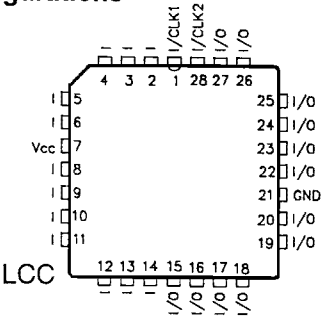
General Description

The PA7128 is a member of the Programmable Electrically Erasable Logic (PEEL) Array family based on ICT's 1-micron CMOS EEPROM technology. PEEL Arrays free designers from the limitations of ordinary PLDs by providing the architectural flexibility and speed needed for today's programmable logic designs. The PA7128 offers a versatile logic array architecture with 12 I/O pins, 14 input pins and 36 registers/latches (12 buried logic cells, 12 input reg/latches, 12 buried I/O reg/latches). Its logic array implements 50 sum-of-product logic functions that share 64 product terms. The PA7128's logic and I/O cells (LCCs, IOCs) are extremely flexible offering up to three output functions per cell (a total of 36 for all 12 logic cells). Cells are configurable as D, T and JK registers with independent or global clocks, resets, presets, clock polarity, and other special features, making the PA7128 suitable for a variety of combinatorial, synchronous and asynchronous logic applications. The PA7128 offers pin compatibility and super-set functionality to popular 28-pin PLDs, like the 26V12. Thus, designs that exceed the architectures of such devices can be expanded upon. The PA7128 supports speeds as fast as 9ns/15ns (tpdi/tpdx) and 83.3MHz (fmax) at moderate power consumption 95mA (75mA typical). Packaging includes 28-pin DIP, SOIC, and PLCC. Development and programming support for the PA7128 is provided by ICT and popular third party development tool manufacturers.

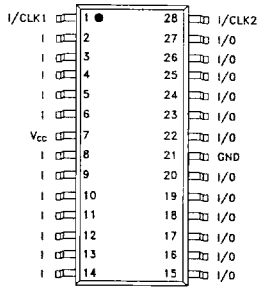
Pin Configurations



DIP

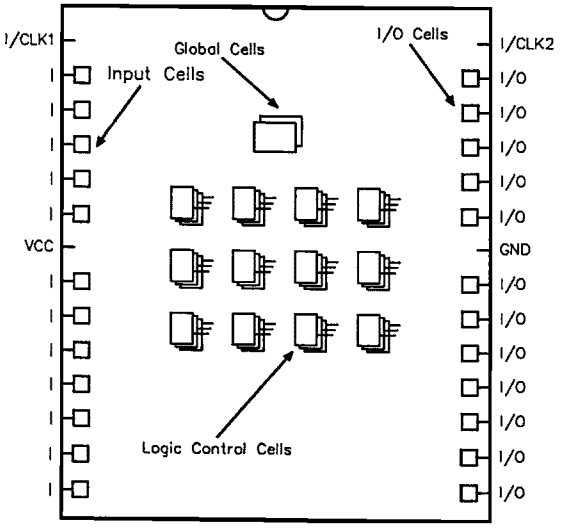


PLCC



SOIC

Block Diagram



Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	− 0.5 to + 7.0	V
V_I, V_O	Voltage Applied to Any Pin	Relative to GND [1]	− 0.5 to V_{CC} + 0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	± 25	mA
T_{ST}	Storage Temperature		− 65 to + 150	°C
T_{LT}	Lead Temperature	(Soldering 10 seconds)	+ 300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial [2]	4.75	5.25	V
T_A	Ambient Temperature	Commercial [2]	0	+ 70	°C
T_R	Clock Rise Time	(Note 3)		20	ns
T_F	Clock Fall Time	(Note 3)		20	ns
T_{RVCC}	V_{CC} Rise Time	(Note 3)		250	ms

D.C. Electrical Characteristics

Over the operating range

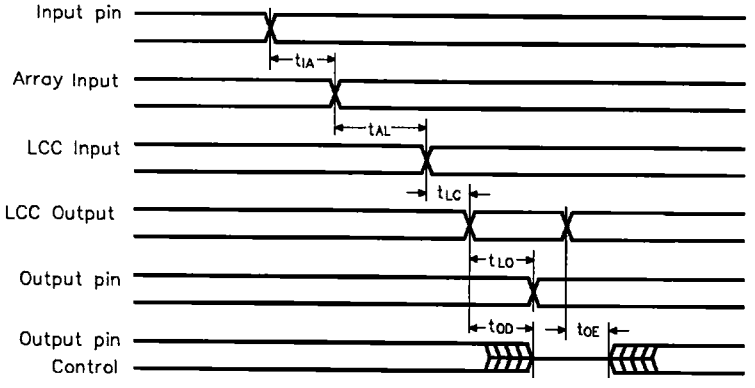
Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage - TTL	V_{CC} = Min, I_{OH} = − 4.0mA	2.4		V
V_{OHC}	Output HIGH Voltage-CMOS	V_{CC} = Min, I_{OH} = −10µA	V_{CC} − 0.1		V
V_{OL}	Output LOW Voltage - TTL	V_{CC} = Min, I_{OL} = 16mA		0.5	V
V_{OLC}	Output LOW Voltage-CMOS	V_{CC} = Min, I_{OL} = 10µA		0.1	V
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level		− 0.3	0.8	V
I_{IL}	Input Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V_O ≤ V_{CC}		±10	µA
I_{SC}	Output Short Circuit Current [5]	V_{CC}=5V, V_O=0.5V, T_A=25°C	− 30	− 120	mA
I_{CC}	V_{CC} Current	V_{IN} = 0V or V_{CC} [4, 12] f = 25MHz All outputs disabled		95 (typ=75) [20]	mA
C_{IN}	Input Capacitance [6]	T_A = 25°C, V_{CC} = 5.0V @ f = 1MHz		6	pF
C_{OUT}	Output Capacitance [6]			12	pF

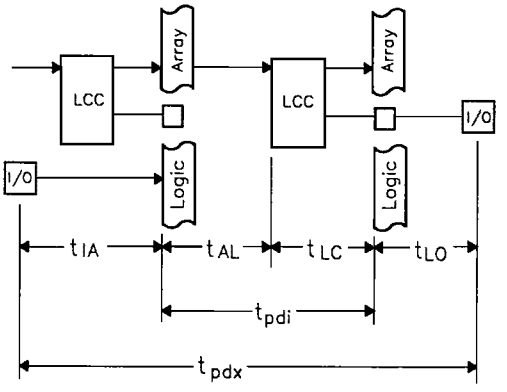
A.C. Electrical Characteristics Combinatorial

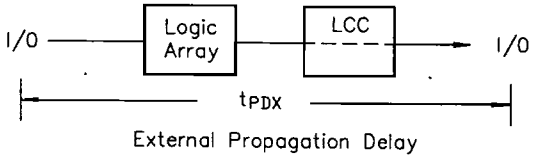
Over operating conditions

Symbol	Parameters [7, 13]	PA7128-15 PA7128-1[18]		PA7128-20 PA7128-2[18]		Units
		Min	Max	Min	Max	
t_{PDI}	Propagation delay Internal (t_{AL}+ t_{LC})		9		12	ns
t_{PDX}	Propagation delay External (t_{IA}+ t_{AL}+ t_{LC}+ t_{LO})		15		20	ns
t_{IA}	Input or I/O pin to Array input		2		3	ns
t_{AL}	Array input to LCC		8		10	ns
t_{LC}	LCC input to LCC output [11]		1		2	ns
t_{LO}	LCC output to output pin		4		5	ns
t_{OD}, t_{OE}	Output Disable, Enable from LCC output [8]		4		5	ns
t_{OX}	Output Disable, Enable from input pin[8]		15		20	ns

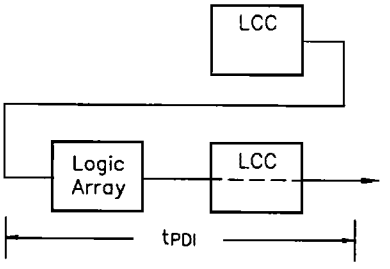
Combinatorial Timing - Waveforms and Block Diagram







External Propagation Delay



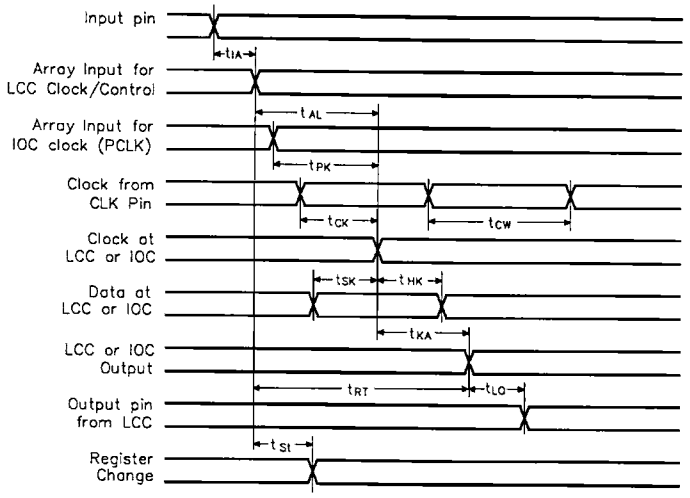
Internal Propagation Delay

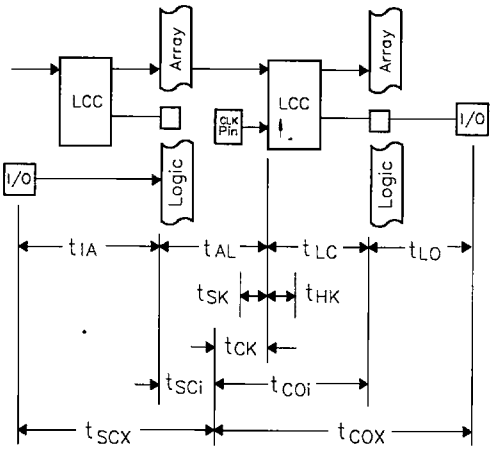
A.C. Electrical Characteristics Sequential

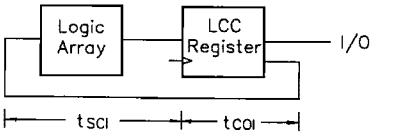
Over operating conditions

Symbol	Parameters [7, 13]	PA7128-15 PA7128-1[18]		PA7128-20 PA7128-2[18]		Units
		Min	Max	Min	Max	
t_{SCI}	Internal set-up to system-clock[9] , - LCC [15] (t_{AL}+ t_{SK}+ t_{LC} - t_{CK})	5		7		ns
t_{SCX}	Input [17] (Ext.) set-up to system-clock,-LCC(t_{IA}+ t_{SCI})	7		10		ns
t_{COI}	System-clock to Array Int.-LCC/IOC/INC[15] (t_{CK}+ t_{LC})		7		9	ns
t_{COX}	System-clock to Output Ext. - LCC (t_{COI}+ t_{LO})		11		14	ns
t_{HX}	Input hold time from system clock - LCC	0		0		ns
t_{SK}	LCC input set-up time to async. clock [14] - LCC	2		2		ns
t_{AK}	Clock at LCC or IOC - LCC output	1		1		ns
t_{HK}	LCC input hold time from async. clock - LCC	4		4		ns
t_{SI}	Input set-up to system clock -IOC/INC[15] (t_{SK} - t_{CK})	0		0		ns
t_{HI}	Input hold time from system clock -IOC/INC(t_{CK}-t_{SK})	4		5		ns
t_{PK}	Array input to IOC PCLK clock		6		7	ns
t_{SPI}	Input set-up to PCLK clock - IOC/INC (t_{SK}-t_{PK}-t_{IA})[19]	0		0		ns
t_{HPI}	Input hold PCLK clock [18]- IOC/INC (t_{PK} + t_{IA} - t_{SK})	6		8		ns
t_{SD}	Input set-up to system clock (t_{IA} + t_{AL} + t_{LC} + t_{SK} - t_{CK}) - IOC Sum-D [16]	7		10		ns
t_{HD}	Input hold time from system clock - IOC Sum-D	0		0		ns
t_{SDP}	Input set-up to PCLK clock (t_{IA} + t_{AL} + t_{LC} + t_{SK} - t_{PK}) - IOC Sum-D	7		10		ns
t_{HDP}	Input hold time from PCLK clock - IOC Sum-D	0		0		ns
t_{CK}	System-clock delay to LCC/IOC/INC		6		7	ns
t_{CW}	System-clock low or high pulse width	6		7		ns
f_{MAX1}	Max system-clock frequency Int/Int 1/(t_{SCI} + t_{COI})		83.3		62.5	MHz
f_{MAX2}	Max system-clock frequency Ext/Int 1/(t_{SCX} + t_{COI})		71.4		52.6	MHz
f_{MAX3}	Max system-clock frequency Int/Ext 1/(t_{SCI} + t_{COX})		62.5		47.6	MHz
f_{MAX4}	Max system-clock frequency Ext/Ext 1/(t_{SCX}+ t_{COX})		55.5		41.6	MHz
f_{TGL}	Max system-clock toggle frequency 1/(t_{CW} + t_{CW}) [10]		83.3		71.4	MHz
t_{PR}	LCC Preset/Reset to LCC output		1		2	ns
t_{ST}	Input to Global Cell preset/reset (t_{IA} + t_{AL} + t_{PR})		11		15	ns
t_{AW}	Asynch. preset/reset pulse width	8		8		ns
t_{RT}	Input to LCC Reg-Type (RT)		7		9	ns
t_{RTV}	LCC Reg-Type to LCC output register change		1		2	ns
t_{RTC}	Input to Global Cell reg.-type change (t_{RT} + t_{RTV})		8		11	ns
t_{RW}	Asynch. Reg-Type pulse width	10		10		ns
t_{reset}	Power-on reset time for register in clear state[3]		5		5	µs

Sequential Timing - Waveforms and Block Diagram

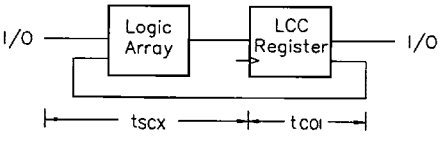






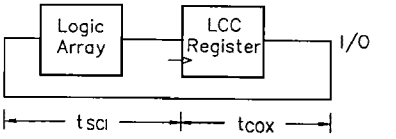
Internal Set–up, Internal Feedback (Int/Int)

$f_{MAX1} = 1/t_{SCI} + t_{COI}$



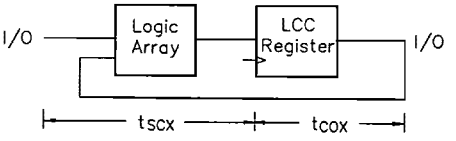
External Set–up, Internal Feedback (Ext/Int)

$f_{MAX2} = 1/t_{SCX} + t_{COI}$



Internal Set–up, External Feedback (Int/Ext)

$f_{MAX3} = 1/t_{SCI} + t_{COX}$



External Set–up, External Feedback (Ext/Ext)

$f_{MAX4} = 1/t_{SCX} + t_{COX}$

Notes:

1. Minimum DC input is – 0.5V, however inputs may undershoot to – 2.0V for periods less than 20ns.
2. Contact ICT for other operating ranges.
3. Test points for Clock and V_{CC} in t_R, t_F, t_{CL}, t_{CH}, and t_{RESET} are referenced at 10% and 90% levels.
4. I/O pins are 0V or VCC.
5. Test one output at a time for a duration of less than 1 sec.
6. Capacitances are tested on a sample basis.
7. Test conditions assume: signal transition times of 5ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
8. t_{OE} is measured from input transition to VREF ± 0.1V (See test loads at end of section 5 for VREF value). tOD is measured from input transition to VOH - 0.1V or VOL + 0.1V.
9. "System-clock" refers to pin 1 or pin 28 high speed clocks.
10. For T or JK registers in toggle (divide by 2) operation only.
11. For combinatorial and async-clock to LCC output delay.
12. ICC for a typical application: This parameter is tested with the device programmed as a 10-bit D type Counter.
13. Test loads are specified at the end of section 3 in this data book.
14. "Async. clock" refers to the clock from the Sum term (OR gate)
15. The "LCC" term indicates that the timing parameter is applied to the LCC register.
    The "IOC" term indicates that the timing parameter is applied to the IOC register.
    The "INC" term indicates that the timing parameter is applied to the INC register.
    The "IOC/INC" term indicates that the timing parameter is applied to both the IOC and INC registers.
    The "LCC/IOC/INC" term indicates that the timing parameter is applied to the LCC, IOC and INC registers.
16. This refers to the Sum-D gate routed to the IOC register for an additional buried register.
17. The term "Input" without any reference to another term refers to an (external) input pin.
18. PA7128-1 is an alternate number for PA7128-15. PA7128-2 is an alternate number for PA7128-20.
19. The parameter t_{SPI} indicates that the PCLK signal to the IOC register is always slower than the data from the pin or input by the absolute value of (t_{SK} - t_{PK} - t_{IA}). This means that no set-up time for the data from the pin or input is required, i.e. the external data and clock can be sent to the device simultaneously. Additionally, the data from the pin must remain stable for t_{HPI} time, i.e. to wait for the PCLK signal to arrive at the IOC register.
20. Typical (typ) ICC is measured at TA = 25°C, Freq = 25MHz, VCC = 5V.