iPLD610
FAST 16-MACROCELL CMOS PLD

Function, Pin, and JEDEC Compatible with EP600, EP610, EP610A, EP630, PALCE610, 85C060 and 5C060 PLDs

- t_{PD} 10 ns, 100 MHz Counter Frequency (w/Internal Feedback)
- I_{CC} = 105 mA max. @ 1 MHz
- Programmable Low-Power Option for "Standby" Operation; 20 μA Typ. in Standby Mode
- Clocking Speed Same as −7 ns PAL* (74 MHz w/External Feedback)
- 16 Macrocells with Programmable I/O Architecture (Register/Combinatorial). Registers Configurable as D/T/JK/RS Types
- Up to 20 Inputs (4 Dedicated and 16 I/O)
- 8 P-Terms, Selectable SOP Invert, Clear and OE P-Terms for Each Macrocell
- Programmable Clock System with 2 Synchronous Clocks and Asynchronous Clocking Option on all Registers
- Extensive Software and Programming Support via Intel and Third Party Tools
- 1-Micron CMOS* III-E EPROM Technology
- Programmable "Security Bit" Allows Total Protection of Proprietary Designs
- 100% Generically Tested Logic Array
- Available in 300-mil 24-Pin PDIP, CerDIP and 28-Pin PLCC Packages

  (See Packaging Specifications Order Number #240800-001, Package Type N and P)

4

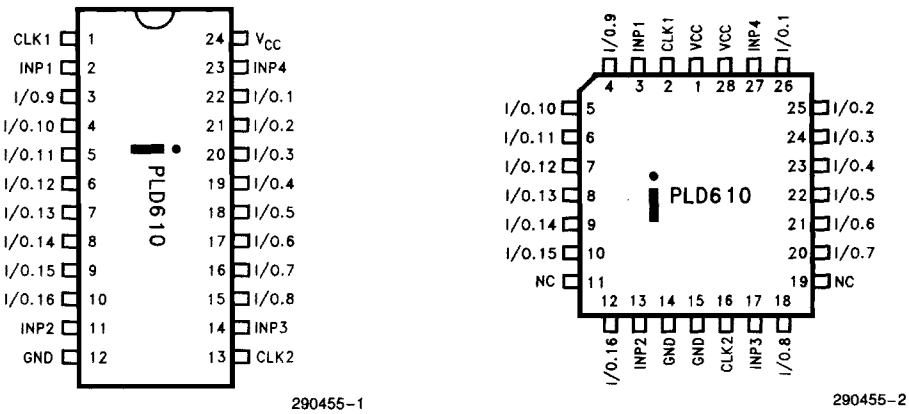

Figure 1. iPLD610 Pin Configurations

*PAL is a registered trademark of Advanced Micro Devices, Inc.

Refer to the 1994 Programmable Logic Handbook for the complete data sheet on this device.

October 1993
Order Number: 290455-002