GSM850/900/1800/1900 Single Chip GSM Radio

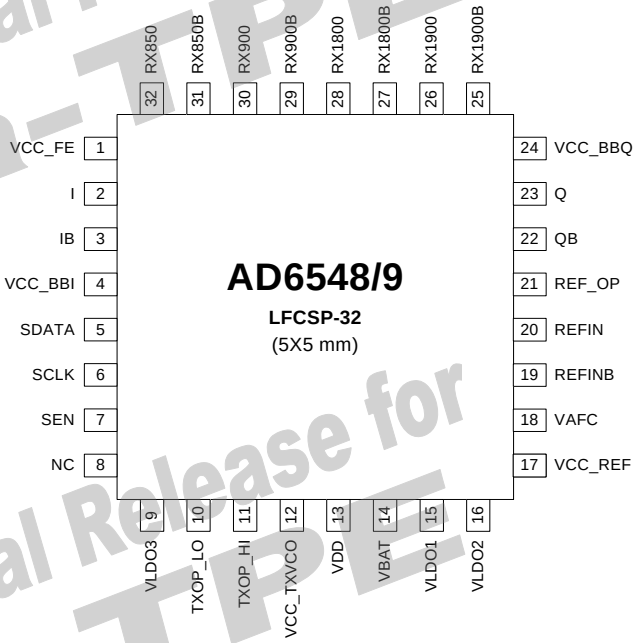
AD6548/9

FEATURES

Fully Integrated GSM Transceiver including
- **Direct Conversion Receiver**
  - **4 Differential LNAs**
  - **Integrated Active RX Channel Select Filters**
  - **Programmable Gain Baseband Amplifiers**
- **Translation Loop Direct VCO Modulator**
  - **Integrated TX VCO and tank**
  - **External TX filters eliminated**
  - **Integrated Loop filter components**
- **High performance multi band PLL system**
  - **Fast Fractional-N Synthesizer**
  - **Integrated Local Oscillator VCO**
  - **Fully Integrated Loop filters**
  - **Crystal Reference Oscillator & Tuning System (AD6548)**
- **Power Management**
  - **Integrated LDOs allow direct battery supply connection**
- **Small footprint**
  - **32-Lead 5 X 5 mm Chipscale Package**

APPLICATIONS

Dual, Triple and Quad Band Radios
- **GSM850, E-GSM 900, DCS1800 and PCS1900**
- **GPRS to Class 12- EDGE RX**



GENERAL DESCRIPTION

The AD6548/9 provides a highly integrated direct conversion radio solution that combines, on a single chip, all radio and power management functions necessary to build the most compact GSM radio solution possible. The only external components required for a complete radio design are the Rx SAWs, PA, Switchplexer and a few passives enabling an extremely small cost effective GSM Radio solution.

The AD6548/9 uses the industry proven direct conversion receiver architecture of the Othello™ family. For Quad band applications the front end features four fully integrated programmable gain differential LNAs. The RF is then downconverted by quadrature mixers and then fed to the baseband programmable-gain amplifiers and active filters for channel selection. The Receiver output pins can be directly connected to the baseband analog processor. The Receive path features automatic calibration and tracking to remove DC offsets.

The transmitter features a translation-loop architecture for directly modulating baseband signals onto the integrated TX VCO. The translation-loop modulator and TX VCO are extremely low noise removing the need for external SAW filters prior to the PA.

The AD6548/9 uses a single integrated LO VCO for both the receive and the transmit circuits. The synthesizer lock times are optimized for GPRS applications up to and including class 12.

To dramatically reduce the BOM both TX Translational loop and main PLL Loop Filters are fully integrated into the device.

AD6548 incorporates a complete reference crystal calibration system. This allows the external VCTCXO to be replaced with a low cost crystal. No other external components are required. The AD6549 uses the traditional VCTCXO reference source.

The AD6548/9 also contains on-chip low dropout voltage regulators (LDOs) to deliver regulated supply voltages to the functions on chip, with a battery input voltage of between 2.9V and 5.5V. Comprehensive power down options are included to minimize power consumption in normal use.

A standard 3 wire serial interface is used to program the IC. The interface features low-voltage digital interface buffers compatible with logic levels from 1.6V to 3.0V.

The AD6548/9 is packaged in a 5mm× 5mm , 32-lead LFCSP package.

ORDERING GUIDE

Model	Temperature Range	Package
AD6548BCPZ	-20°C to +85°C	LFCSP-32
AD6549BCPZ	-20°C to +85°C	LFCSP-32

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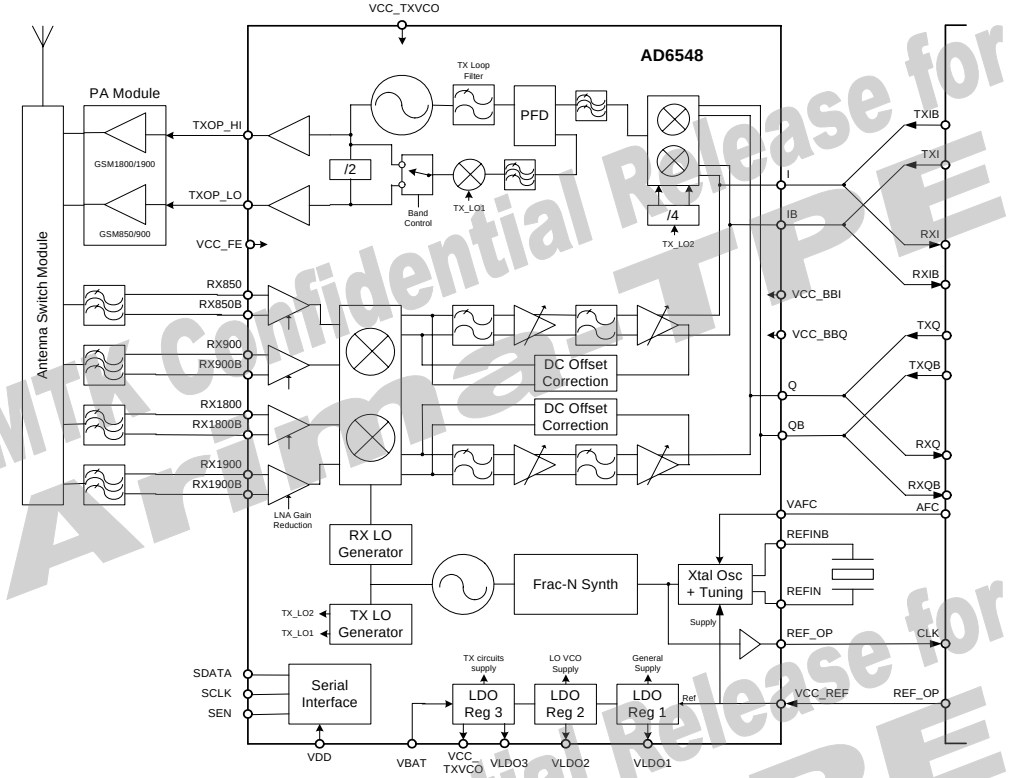

Figure 1 AD6548 & AD6549 Block Diagrams

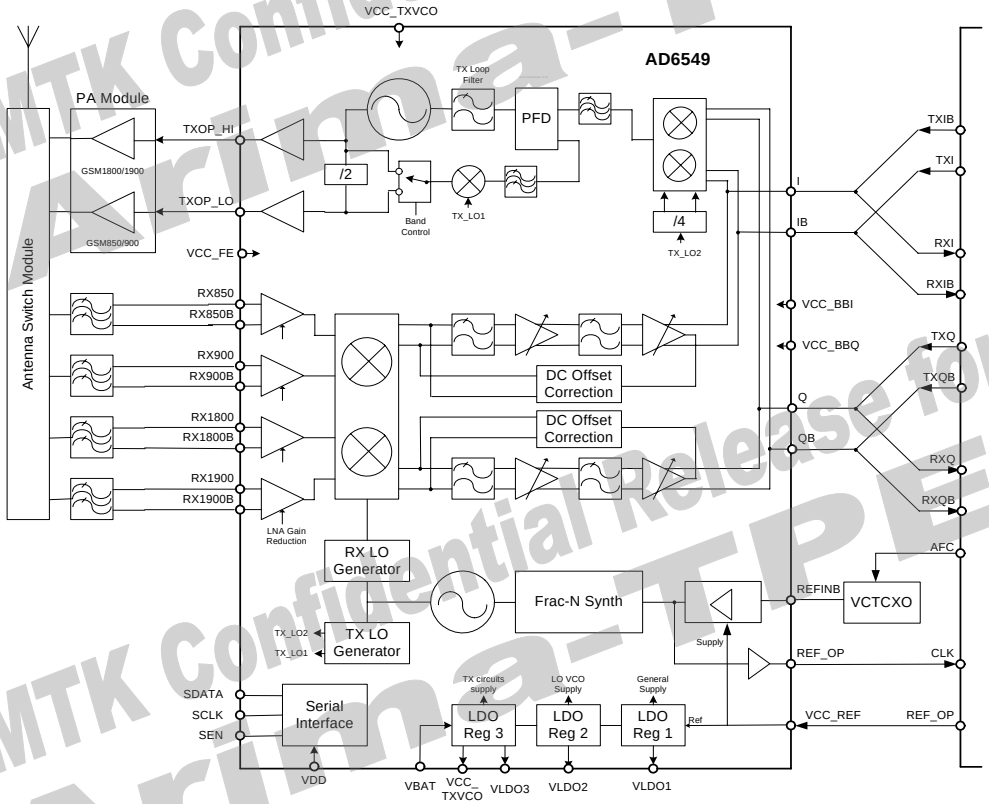

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Table 1. AD6548/9 Pin Descriptions

No	Name	Description	No	Name	Description
1	VCC_FE	Front end supply (IP)[3]	17	VCC_REF	Reference Oscillator Supply (IP)
2	I	I baseband input/output	18	VAFC	AD6548 Crystal Freq control (IP) AD6549: Connect to VCC_REF
3	IB	I baseband input/output	19	REFINB	Crystal / VCTCXO Connection
4	VCC_BBI	Baseband I, TX path supply (IP)[3]	20	REFIN	Crystal Connection
5	SDATA	Serial port data	21	REF_OP	Reference Frequency Output
6	SCLK	Serial port clock	22	QB	Q baseband input/output
7	SEN	Serial port enable	23	Q	Q baseband input/output
8	N/C	Not connected	24	VCC_BBQ	Baseband Q supply (IP)[3]
9	VLDO3	TX LDO Output[1]	25	RX1900B	PCS 1900 LNA input
10	TXOP_LO	Transmit O/P (850/900MHz)	26	RX1900	PCS 1900 LNA input
11	TXOP_HI	Transmit O/P (1800/1900MHz)	27	RX1800B	DCS 1800 LNA input
12	VCC_TXVCO	TX VCO supply (1)	28	RX1800	DCS 1800 LNA input
13	VDD	Serial interface supply	29	RX900B	E-GSM 900 LNA input
14	VBAT	Battery I/P for LDO reg's	30	RX900	E-GSM 900 LNA input
15	VLDO1	LDO regulator Output[2]	31	RX850B	GSM 850 LNA input
16	VLDO2	LO VCO Supply[1]	32	RX850	GSM 850 LNA input

Notes:
1. LDO output pin is for external decoupling only. Do not connect to any other supply.
2. Internally connected to Synth supply (Counters + SDM + Charge pump)
3. These Supply pins should **only** be connected to the regulated supply provided by VLDO1; not to any other supply.

FUNCTIONAL DESCRIPTION

Receiver

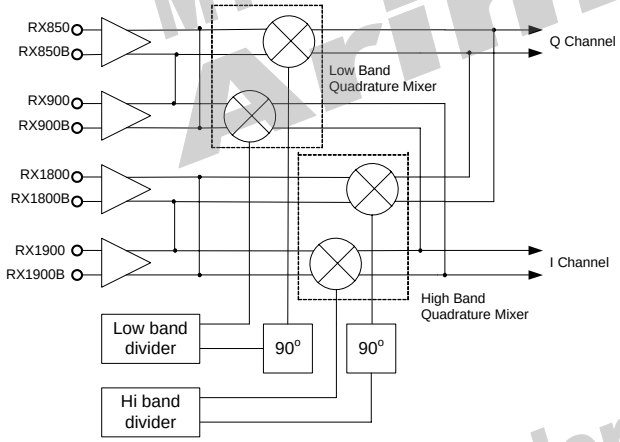


Figure 2 Receiver Chain

The AD6548/9 receiver section fully integrates all the RF and baseband signal processing. Each major block is described in the following sections.

Low Noise Amplifiers

The AD6548/9 includes four fully integrated Low Noise Amplifiers (LNAs), to support quad band applications without further external active components. The LNAs have differential inputs which minimize the effect of unwanted interferers. The inputs are easily matched to industry standard Front End Modules (FEMs) or discrete Rx SAW filters. The outputs of the LNAs are directly coupled to the down-converting mixers. The voltage gain of the LNAs are typically 24 dB. Each LNA can be switch to a low gain mode when receiving large input signals as part of the AGC system.

Down-Converting Mixers

Two quadrature mixers are used to mix down the signals from the LNAs, one for the high bands (1800 and 1900 MHz) and one for the low bands (850 and 900 MHz). The outputs of the mixers are connected to the baseband section through an integrated single pole filter with nominal cut-off frequency of 800kHz. This acts as a "roofing filter" for the largest blocking signals (i.e. those ≥ 3MHz) and prevents the baseband amplifiers from being overloaded.

Baseband Amplifiers / Low Pass Filters

The baseband amplifiers provide the majority of the analog receiver gain. The filtering is provided by an integrated 5th order Chebyshev filter giving the necessary adjacent channel and blocking filtering, it is also acting as an anti-alias filtering for Baseband IC's converters. A final low pass pole is possible

at each of the baseband outputs via internal series resistor along with an external shunt capacitor. The external capacitor is not normally required with ADI baseband ICs. The on chip filter has an auto calibration feature ensuring that the filters are tuned for optimum performance.

The baseband amplifiers have programmable gain for system AGC. A total of 57 dB of gain control is provided in 3dB steps programmable over the serial interface. This together with the LNA gain control gives a total of 77dB of gain control range.

The receive baseband outputs are routed to the common Rx/Tx I/Q ports for connection with the baseband converters.

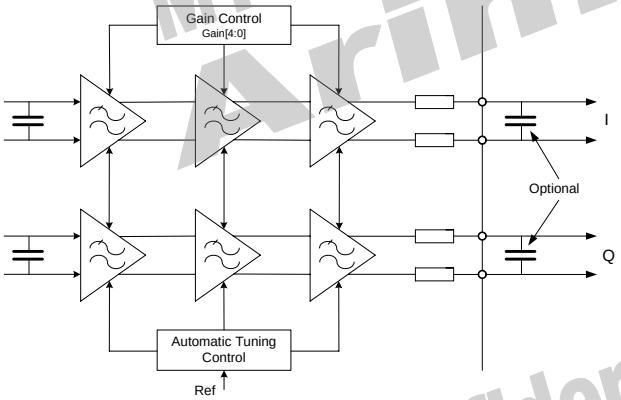


Figure 3 Baseband Amplifiers

Baseband Output D.C. Offset Correction

In order to minimize D.C. offsets inherent in the receiver and maximize dynamic range a D.C offset correction circuit is integrated. This correction is triggered over the serial bus and then an offset tracking loop is enabled to minimize residual offsets under all conditions. The tracking loop is fully hardware integrated, requiring no software intervention.

Receiver Local Oscillator (LO) Generator

The Rx LO generator is used to avoid DC offset problems associated with LO leakage into the receiver RF path. By operating the VCO at a frequency other than the desired receive frequencies, any leakage of the VCO will fall out of band. The LO generator is used to convert the offset synthesized VCO output to the on-frequency quadrature LO required by the chipset. The LO generator is implemented as a regenerative frequency divider, performing a 2/3 multiplication of the VCO output for the high band (DCS1800/PCS1900) and a 1/3 multiplication for low band (E-GSM 900/GSM850).

Transmitter

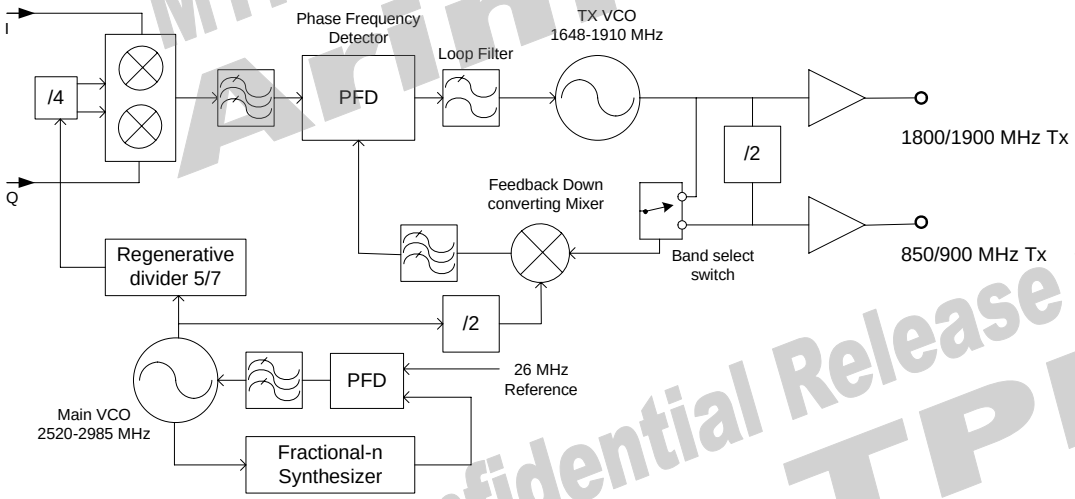


Figure 4 Transmit Path

Overview

The transmit section of the AD6548/9 radio implements a translation loop modulator. This consists of a quadrature modulator, high speed phase-frequency detector (PFD) with charge pump output, loop filter, TX VCO and a feedback down converting mixer. The VCO output (divided by 2 for low band) is fed to the power amplifier with a portion internally fed back into the down-converting feedback mixer to close the feedback loop.

Quadrature Modulator

The Quadrature modulator takes the baseband I & Q signals and translates these into a GMSK signal at the Transmit Intermediate Frequency (TX IF). After bandpass filtering and limiting the TX IF signal is used as the reference input to the Phase Frequency Detector (PFD) of the transmit PLL.

Phase Frequency Detector (PFD)

The PFD ensures that the transmitted signal contains the required modulation and is accurately locked to the desired GSM channel. The downconverted feedback signal from the TX VCO and the Quadrature Modulator output are phase compared by the PFD. The PFD charge pump generates a current pulse proportional to the difference in phase which is applied to the loop filter.

Loop filter

To minimize complexity of the external PCB layout the TX loop filter is fully integrated into the IC. At power up the filter is automatically calibrated as part of the baseband filter cal, eliminating process tolerances. The calibration is fully integrated and requires no extra programming.

TX VCO

The Transmit Voltage Controlled Oscillator (TX VCO) and tank components are a fully integrated subsystem. The subsystem includes PA drivers so the outputs are used to directly drive the external PAs. The low noise oscillator design and internal filtering mean that external TX SAW filters are not required. In Low band operation the TX VCO output is divided by two and filtered. The TX VCO is automatically calibrated to ensure optimum performance over its operating frequency of 1648 to 1910 MHz.

Feedback Down-Converting Mixer

The feedback down converting mixer is used to translate the TX VCO output frequency to the TX IF. An integrated band pass filter exists between the mixer and the PFD to filter the mixers unwanted side band and higher order mixing products.

Transmit Frequency Plan

Unlike many other translation loop modulators the AD6548/9 uses only a single VCO source to derive the local oscillator signal for both the Feedback Down-Converting Mixer and the Quadrature modulator. Therefore there is a fixed relationship between the Tx IF frequency and the LO VCO frequency such that:

$$F_{IF} = F_{VCO} \times \left[\frac{5}{28}\right]$$

This ratio was chosen to minimize VCO tuning range, TX IF frequency variation and ensure excellent transmit spectral mask performance.

The Feedback-Down Converting Mixer operates low side injection for the high bands and high side injection for the low bands. The final relationship between the transmitted TX frequency and the LO VCO frequency is different between the two bands. Specifically:

$$F_{VCO} = F_{TX\_LowBand} \times \left[\frac{28}{9}\right] \qquad F_{VCO} = F_{TX\_HiBand} \times \left[\frac{28}{19}\right]$$

These relationships are taken account of in the synthesizer architecture and programming.

Main Frequency Synthesizer

The AD6548/9 has a single fast-locking fractional synthesizer used for VCO control in both receive and transmit mode. The entire system including VCO, tank, fractional N dividers, sigma delta compensation, charge pump and loop filters are fully integrated. The only external component is the frequency reference. The synthesizer is controlled via the serial interface. The VCO is fed into the respective dividers to generate the appropriate LO frequencies for the RX and TX bands.

Fractional N Dividers

The fractional N divider allows the PLL system to have a smaller step size than the comparison frequency which is set by the external reference to 26 MHz. This feature allows all the GSM frequency band rasters to be achieved, with fast lock times and good phase noise characteristics.

The divider section consists of a dual modulus 8/9 prescaler, integer M & A dividers, and fractional N system based on sigma-delta modulation to generate the required fractional divide ratio. The Denominator of the fractional divider can be set to 3 different values, (1040, 1170, 1235), depending on the mode of operation. For example a denominator of 1040 with an input fraction F maintains an average value of F/1040 allowing 25 kHz steps when operated at a reference of 26 MHz.

The Overall count value is thus:

8*M + A + Fraction

Where:
M is 4 bits, but the MSB is set to 1
A is 3 Bits
Fraction is N/ Denominator.
The Denominator is set to one of 3 values: 1040, 1170, 1235.
N is a 11 bit value.

Values for M, A and N are loaded from serial interface word, but the denominator is automatically set according to the mode. Refer to the Programming Procedures for more details.

Phase Frequency Detector/Charge Pump

A Phase Frequency Detector (PFD) is used for the PLL phase detector. The charge pump is designed such that good matching of up and down currents is achieved over a wide output operating range. The charge pump output is internally routed to the integrated synthesizer loop filter.

Synthesizer Loop filter

To minimize complexity of the external PCB layout the Main Synthesizer loop filter is also fully integrated into the IC. No external components or adjustments are required .

Voltage Controlled Oscillator

The integrated voltage controlled oscillator (VCO) is a complete self-calibrating subsystem. This employs a fully automated digital self-calibration function to ensure optimum phase noise performance over the entire frequency range. The VCO generates frequencies between 2520MHz and 2985MHz as required to operate in the four GSM bands for RX and TX.

Reference Oscillator

The reference input circuitry is different between the AD6548 and AD6549 as described in the table.

Chip Number	Source
AD6549	VCTCXO
AD6548	Crystal

AD6549 Description:
The 26MHz reference frequency is provided by an external VCTCXO module, supplied to the REFINB pin. The REFIN pin must be AC grounded via a 1nF capacitor. In this case temperature and frequency stability are provided by the VCTCXO module.

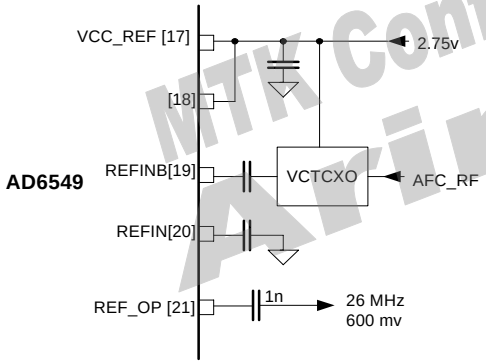


Figure 5 AD6549 Simplified Reference Connections

AD6548 Description:
The AD6548 requires only an external low cost crystal as the frequency reference. The circuitry to oscillate the crystal and tune its frequency is fully integrated. For good noise immunity the oscillator is a balanced implementation requiring the crystal to be connected across 2 pins. There is a programmable capacitor array included for coarse tuning of fixed offsets (e.g. crystal manufacturing tolerance), and an integrated varactor for dynamic control. The oscillator is designed for use with a 26MHz crystal. The crystal is connected as shown in figure 6.

Dedicated control software ensures excellent frequency stability under all circumstances.

Both AD6548 and AD6549 reference oscillators provides a 26 MHz 600mVpp (typical) output (REF_OP), for use as the baseband clock input. This is designed for low harmonic content.

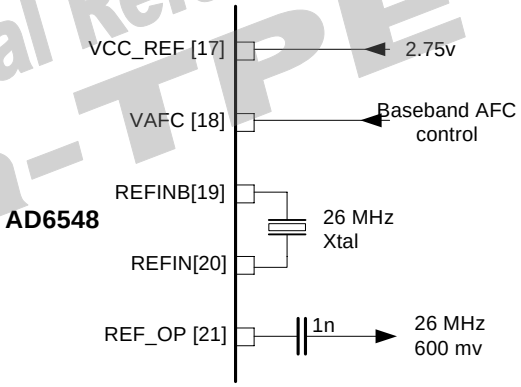


Figure 6 AD6548 Crystal Oscillator External Connections.

Power Management

Overview

For direct battery supply connect, and to reduce external circuitry complexity the AD6548/9 features three Low Drop Out Regulators (LDOs). The three LDOs provide isolation of the oscillators and sensitive circuits from unwanted power supply and cross coupled noise. They also ensure the IC operation is robust over a wide range of power supply voltages. For power management the LDOs are independently controlled via the 3 wire serial bus.

LDO Usage

The following table describes the LDO usage:

LDO1	LDO2	LDO3
Rx and Tx baseband sections	Main VCO	TX VCO

Table 2: Intended LDO Use

The LDO outputs require external connection to the respective pins described in table 3, and each requires decoupling capacitors. The LDOs are designed to be unconditionally stable regardless of the capacitor's ESR.

LDO OP	External Connection
VLDO1	VCC_FE, VCC_BBI, VCC_BBQ
VLDO2	No external Connections, except for decoupling
VLDO3	No external Connections, except for decoupling

Table 3: LDO Connections

LDO1 derives its input references from the crystal supply voltage (VCC_REF). It is therefore expected that VCC_REF be supplied from a external LDO of nominal supply voltage 2.75V (e.g. ADP3330 or Analog Baseband IC: Vout=2.75V±1.4%).

Serial Interface

Overview

A standard 3 wire bus is used to communicate with the device as shown in Figure 7. The serial bus is a common bus which can be shared with other RF and baseband devices.

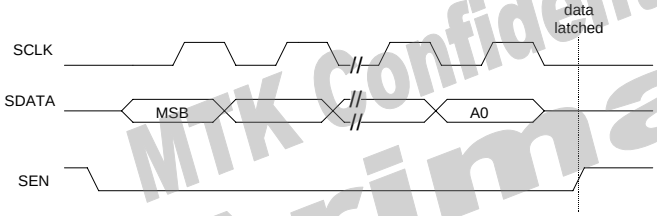


Figure 7 Serial interface bus

Data is clocked in on the rising edge of SCLK with MSB first. SDATA is latched on the rising edge of SEN. If immediate action is required this is aligned with rising edge of SEN. If this is not required the word is latched for later use.

Serial Word Format

SDATA is clocked through a set of flip-flops, the last 5 defining the address field. The address decoder runs all the time but SDATA is only latched on the rising edge of SEN. Preceding the address field is a 2 bit opcode field defining the action (Table 4). The remaining bits are for data to program register contents. The length of the data field varies depending on the specified register. Refer to the Register Definition section for details on register content, and the Specification section for details on the hardware timing parameters.

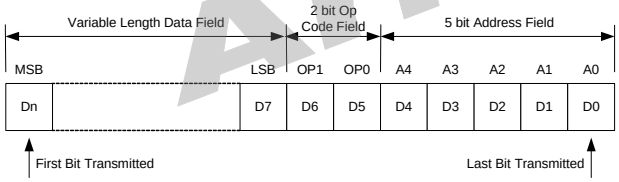


Figure 8 Serial Word Format.

OP0	OP1	Operation	Description
0	0	Write	Normal register write
0	1	Clear	Clear register with supplied mask
1	0	Set	Set register with supplied mask
1	1	Reserved	Do no use

Table 4 Op Code Definition

The data length on the serial bus can be adjusted to accommodate different word lengths needed in different situations. The maximum data word length in normal operation is 17, giving a total maximum length (Dn) of 24 bits.

PROGRAMMING PROCEDURES

Synthesiser Programming

The following section provides the method for deriving the AD6548/9 LO synthesizer programming words for receive and transmit modes. Worked examples are then provided for extra clarity.

Calculation of Nint and Nfrac:

1) Calculate the channel frequency from the mode and ARFCN number provide by the protocol stack. This is achieved using the frequency tables provided in 3GPP TS 45.005. This frequency is labelled RF in Step 2.

2) Calculate AD6548/9 LO frequency from the RF frequency and mode:

Receive Mode:

LO = 3*RF ..... (GSM850/E-GSM 900)
LO = (3/2)*RF .....(DCS1800/PCS1900)

Transmit Mode:

LO = (28/9)*RF .....(GSM850/E-GSM 900)
LO = (28/19)*RF ….(DCS1800/PCS1900)

3) Calculate Neff (effective value of the divider) for 26MHz reference.

Neff=LO / 26 (LO in MHz)

4) Neff must be expressed as integer and a fractional parts:

Nint + (Nfrac/MOD) = Neff

Nint is an integer
Nfrac is the fractional portion.
MOD is the sigma delta Modulus.

The modulus (MOD) is automatically selected depending on the Tx/Rx mode select and the band select according to the table below:

Mode	Band	MOD
RX	-	1040
TX	E-GSM900	1170
TX	DCS1800	1235
TX	PCS1900	1235
TX	GSM850	1170

5) Program register 6.
Use the binary equivalents of Nint and Nfrac to program register 6.

Note : The MSB of Nint (which should always be '1') is dropped as this bit is hardcoded internal to the IC.

Transmit Example

ARFCN=124, E-GSM 900, mode TX:
Carrier Frequency = 914.8 MHz (Step 1)
LO = 2846.04444… MHz (Step 2)
Neff = 109.4632479.. (Step 3)
MOD=1170 (Step 4)
Nint = Integer part of Neff = 109 [b1101101]
Nfrac =1170*0.4632479.. = 542 [b01000011110]
Combine binary Nint & Nfrac [Remember to drop Nint MSB]

Register 6 Content																LSB
Nfrac											Nint					
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	0	0	1	1	1	1	0	1	0	1	1	0	1

Receive Example

ARFCN=846, DCS1800, mode RX:
Carrier Frequency = 1872.0 MHz (Step 1)
LO = 2808.0 MHz (Step 2)
Neff = 108.00 (Step 3)
MOD = 1040 (Step 4)
Nint = Integer part of Neff = 108 [b1101100]
Nfrac =1040*0 = 0 [b00000000000]
Combine binary Nint & Nfrac [Remember to drop Nint MSB]

Register 6 Content																LSB
Nfrac											Nint					
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0

Modes of Operation

The AD6548/9 can be configured into many different states, however the six most commonly applied to a GSM handset are described in this section. The modes are determined by the VCC_REF and V_{DD} power supplies provided and by serial bus programming.

The V_{DD} logic supply and VCC_REF supply for the Reference supply and VCTCXO (if present) are external – either from the baseband or a separate regulator.

Off Mode

In Off Mode everything is powered down and only leakage current is drawn. All register contents & previous calibration results are lost. This mode is used when the handset is off.

States: V_{DD} is not present
VCC_REF is not present
LDOs & all power bits disabled

Power Down Mode

In Power Down Mode everything is powered down, but the logic supply is present to maintain calibration settings and register contents. Only leakage current is drawn. This mode is used between paging blocks.

States: V_{DD} is present
VCC_REF is not present
LDOs & all power bits disabled

Wait Mode

Transitioning between Power Down and Wait Mode is simply controlled by the reference power supply (VCC_REF). The Reference Oscillator will automatically start when power is applied.

This mode is used when the baseband section is transferring from sleep to fully operational before a receive or transmit burst. It can also be used if Power Down Mode is not desired between paging blocks. Minimum current consumption is drawn.

States: V_{DD} is present
VCC_REF is present
LDOs & all power bits disabled

Alert Mode

In Alert Mode the Reference Oscillator and synthesizer are active. This mode is present prior to a receive or transmit burst. LDO1 & LDO2 are enabled, but the RX_ON and TX_ON bits are clear in the Power Control register.

States: V_{DD} is present
VCC_REF is present
LDO1 & LDO2 enabled
Synth & LOVCO enabled

Receive Mode

In this mode the Receiver is active, so the radio will receive a GSM burst, after a short period has elapsed for the circuits to stabilize. It is the same as Alert Mode but with the receive section enabled via the serial interface.

States: V_{DD} is present
VCC_REF is present
LDO1 & LDO2 enabled
Synth & LOVCO enabled
RX_ON bit set

Transmit Mode

In this mode the Transmitter is active, so the radio will transmit a GSM burst, after a short period has elapsed for the circuits to stabilize. It is the same as Alert Mode but with the transmitter section enabled via the serial interface

States: V_{DD} is present
VCC_REF is present
LDO1 & LDO2 enabled
Synth & LOVCO enabled
TX_ON bit set
(LDO3 automatically enabled)

Control Sequence

Initially the handset is in Power Down mode. Only a very simple timer chain in the baseband is running supplied by a 32 kHz clock. AD6548/9 will only consume leakage current. After a set amount of time the Baseband IC will enable VCC_REF and the Reference Oscillator will begin to oscillator at 26 MHz. AD6548/9 will now be in Wait Mode. Once the Reference Oscillator is stabilized the microprocessor will start. It will then set the AD6548/9 into Alert mode and program the synthesizers. Just prior to the start of the receive burst the AD6548/9 will be set into Receive Mode until the burst ends where it will change back to Alert Mode and eventually all the way back to Power Down Mode. The same principle applies to when a burst is transmitted where AD6548/9 changes from Alert Mode to Transmit Mode when the burst starts and back from Transmit Mode to Alert Mode when the burst ends. The typical timing of the power up sequence prior to the RX or TX burst and the resulting current consumption are shown in Figures 7 and 8. Note that Tx VCO LDO is automatically enabled when Tx is enabled. The LDO's may be disabled in the inactive periods between bursts, however in the cases of GPRS and HSCSD LDO1 and LDO2 should be left enabled. The LDOs alone draw minimal current.

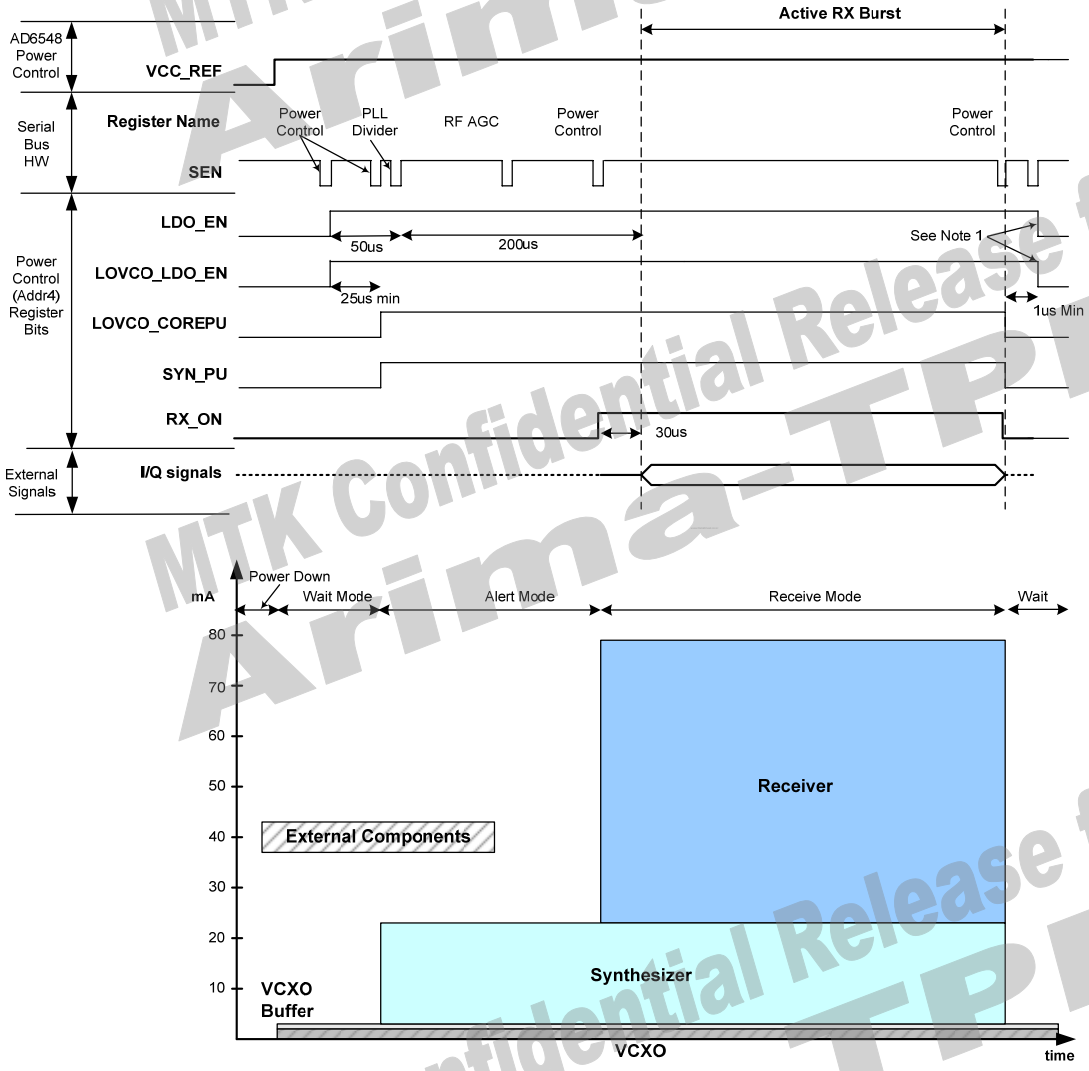


Figure 9 Typical timing of the power up sequence prior to the RX burst and the resulting current consumption

Note 1: The LDO's can remain powered up after the initial RX burst. This is to simplify the timing for subsequent RX and TX bursts in traffic mode, as the LDO start up timing is removed along with a Power Control register access. If the main LDO is powered down after the burst then the described wait time must be observed between the de assertion of RX_ON and LDO_EN.

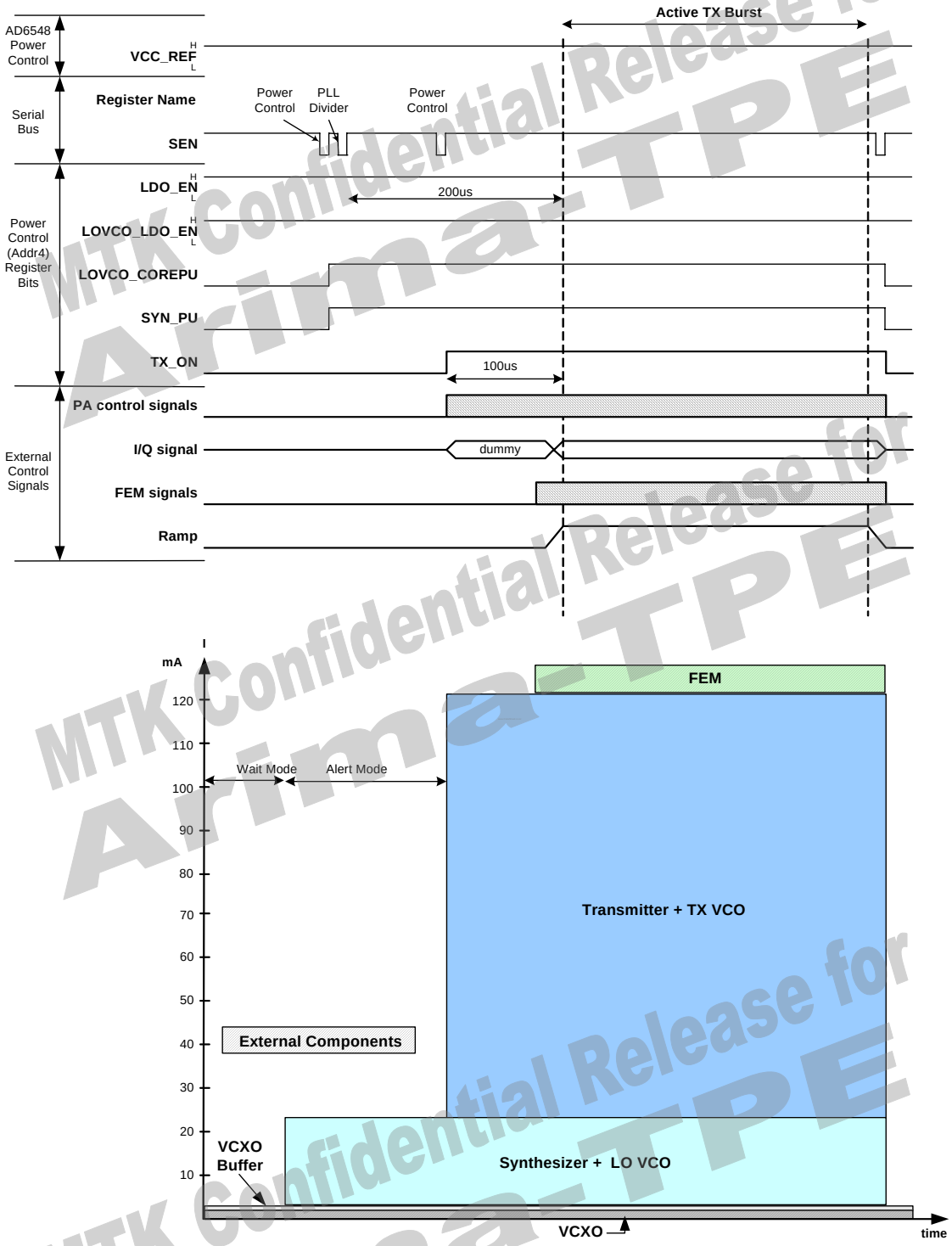


Figure 10 Typical timing of the power up sequence prior to the TX burst and the resulting current consumption

Note:
This timing diagram assumes a preceding RX burst as shown in figure 9, where the LDOs are not disabled. This is acceptable for traffic mode.

Calibration Description

The Integrated filters and Receiver DC offsets must be auto-calibrated to provide optimum IC performance. The Calibrations are an event that only needs to occurs upon powering up the device. They are initiated by software and can be run concurrently. The calibrations are fully automated and require no further action once initiated.

To perform the calibrations :

1) Ensure the VCC_REF is applied so that the 26MHz Reference Oscillator is running.
2) Power up and enable the receiver & synthesizer. (The DC_AUTOCAL must be Low.)
3) Wait 50us, for the receiver system to settle.
4) Set the ST_BB_CAL and DC_AUTOCAL[1] bits High (in the Initialization and Set up Register).
5) Integrated filter calibration will be completed within 1.28ms and the ST_BB_CAL is automatically cleared by hardware. The filter coefficients produced will be stored in the FLT_ADJ bits.
6) DC Offset Calibration (For both high and low bands) will be completed in 4.3ms from the start of calibration.
7) Once both calibrations are complete the receiver can be powered down; the calibration results are preserved as long as VDD is present. After calibration the PLL and gain settings will return to their pre calibration values automatically. Figure 11 shows the correct power down sequence using two Power Control writes; the first to turn off the RX_ON and circuit blocks, and the second to disable the LDOs.

Note 1: The DC Offset calibration is initiated on the **rising edge** of DC_AUTOCAL.

During normal operation the DC_AUTOCAL should remain high to ensure that the DC offset remains small over all conditions.

Figure 11 show the timing of the initialization and auto calibration sequence, as describe above.

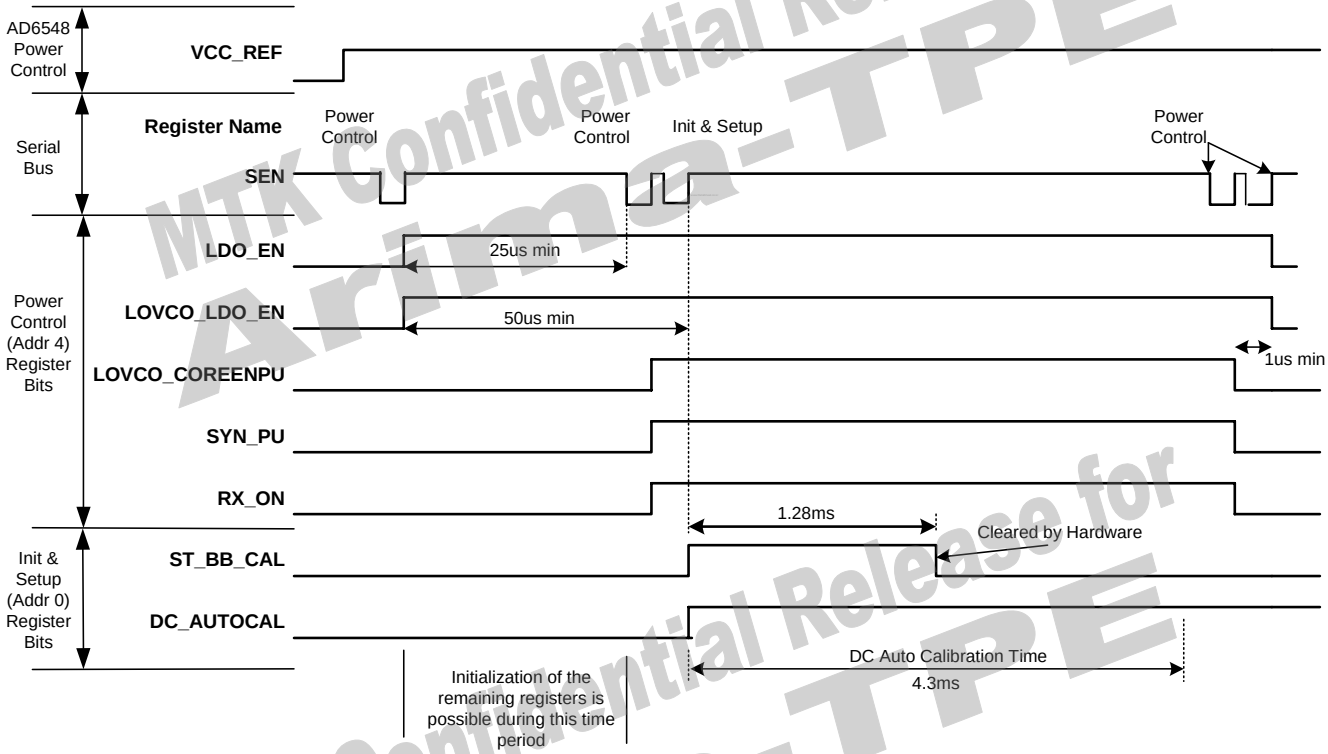


Figure 11 Initialization and auto calibration timing sequence

REGISTER DEFINITIONS

Register Addresses

The serial interface word definition provides 5 address bits, giving a maximum of 32 words in the protocol. For the AD6548/9 IC not all addresses are allocated. Table 5 describes the used addresses.

Address	Word Length	Data Width	Main function
0	18 bits	11 bits	Initialization and setup
1	14 bit	7 bits	Synthesizer initialization and setup
4	16 bits	9 bits	Power control
5	13 bits	6 bits	AGC and LNA gain
6	24 bits	17 bits	PLL divider
29	11 bits	4 bits	IC Test Register 1
31	11 bits	4 bits	IC Test Register 2

Register Map

The **bold** values are the default values after power-on reset or when the reset bit has been applied

Bit	Name	Description	Value

Address 0

D[6..0]	*Initialization and Setup*	*Initializes AD6548/9. This register is expected to be programmed mainly at power up.*	*Address 0 and opcode*
D[7]	RESET	Resets to the default values (usually zero). The reset bit will be cleared at the following clock edge, normally a part of the next programming word	0: Reset is performed **1: No reset is performed**
D[8]	ST_BB_CAL	Start baseband & Loop filter calibration. Calibration will last 1.28 ms. Completion clears ST_BB_CAL.	**0: Calibration inactive** 1: Start calibration
D[12..9]	FLT_ADJ[3..0]	Baseband and loop filter adjustments. Overwritten by baseband cal.	**0: Highest cut off** 0b1111: Lowest cut off
D[13]	DC_AUTOCAL	Positive transition triggers autocal. Should stay HIGH to keep autocal results	**0: Autocal inactive** 1: Use autocal values
D[15..14]	REF_OP[1..0]	Reference Output mode	**0: Normal** 1: CMOS Test Mode (PLL counter o/p) 2 : OFF 3 : High Current
D[16]	HI_BAND	Identifies hi band for use in DC autocal	**0: 1800** 1: 1900
D[17]	LOW_BAND	Identifies lo band for use in DC autocal	0: 850 **1: 900**

Address 1

D[6..0]	*Synthesizer Initialization and Setup*	*Initializes AD6548/9 synthesizer. This register is expected to be programmed mainly at power up.*	*Address 1 and opcode*
D[7]	RESERVED		0
D[13..8]	AFC_CAP[5..0]	Sets the internal caps to coarse tune the crystal frequency (~0.16F steps)	**0: min capacitance** 63: max capacitance

Address 4

D[6..0]	*Power Control*	*Enables/disables different sections. This register is expected to be programmed just before and after an active burst*	*Address 4 and opcode*
D[7]	LOVCO_LDO_EN	Enable regulator used for integrated LO VCO	**0: LO VCO LDO disabled** 1: LO VCO LDO enabled
D[8]	LDO_EN	Enable LDO regulator used for AD6548/9 RX/TX	**0: LDO disabled** 1: LDO enabled
D[9]	RX_ON	Enable receive section .	**0: Rx section disabled** 1: Rx section enabled
D[10]	TX_ON	Enable transmit section	**0: Tx section disabled** 1: Tx section enabled
D[12..11]	B_SEL[1..0]	Band selection . Only active with active Tx or Rx	**0: E-GSM 900 selected** 1: DCS1800 selected 2: PCS1900 selected 3: GSM850 selected
D[13]	LOVCO_COREPU	Enable LO VCO power up	**0: LO VCO disabled** 1: LO VCO enabled
D[14]	SYN_PU	Enable synthesizer	**0: Synthesizer disabled** 1: Synthesizer enabled
D[15]	PLL_TXRX	Indicate PLL word TX or RX	**0:Rx PLL word** 1:Tx PLL word

Address 5

D[6..0]	*RF AGC and LNA Gain Reduction*	*AGC and LNA programming. This register is expected to be programmed one or two times in every receive burst*	*Address 5 and opcode*
D[11..7]	GAIN[4..0]	Sets the AGC gain in 3 dB increments	0: 3 dB gain **1: 3 dB gain** 2: 3 dB gain 3: 6 dB gain 21: 60 dB gain
D[12]	GR	Reduces the LNA gain by 20 dB	**0: No gain reduction** 1: 20 dB gain reduction

Address 6

D[6..0]	*PLL Divider*	*Programs a new divide word for the PLL divider. Constructed as a 7 bit integer number [5..127] and an 11 bit fractional number [0..2047]*	*Address 6 and opcode*
D[12..7]	INT[5..0]	Integer part(lower 6 bits of 7 bit word-see section 5 pg 9)	**0x14**
D[23..13]	FRAC[10..0]	Fractional part	**0x000**

Address 29

D[6..0]	*Test Register # 1*	Test Bits	*Address 29 and opcode*
D[10..7]	Test Bits	Reserved	**0x0**

Address 31

D[6..0]	*Test Register # 2*	Test Bits	*Address 31 and opcode*
D[10..7]	Test Bits	Reserved	**0x4 (0b0100)**

Table 2 AD6548/9 programming words.

SPECIFICATIONS

Operating Conditions

Parameter	Symbol	Min	Max	Units
Battery Voltage	V_{BAT}	2.9	5.5	V
Crystal Oscillator Supply Voltage	VCC_REF	2.71	2.79	V
Serial Interface Supply Voltage	V_{DD}	1.6	3.0	V
Ambient Temperature	T_A	–20	85	°C
GSM850 Transmit band		824	849	MHz
E-GSM900 Transmit band		880	915	MHz
DCS1800 Transmit band		1710	1785	MHz
PCS1900 Transmit band		1850	1910	MHz
GSM850 Receive band		869	894	MHz
E-GSM900 Receive band		925	960	MHz
DCS1800 Receive band		1805	1880	MHz
PCS1900 Receive band		1930	1990	MHz

Absolute Maximum Ratings

(T_A= +25°C unless otherwise stated)

V_{BAT} to GND (Power Down Only) .....–0.3V to + 6.0V
V_{BAT} to GND powered up .....–0.3V to + 5.5V
V_{DD} to GND.....–0.3V to 3.3V
VCC_REF to GND.....–0.3V to 3.3V
Digital Input Voltage to GND.....–0.3V to V_{DD} +0.3V
Maximum power dissipation.....1000 mW
Maximum differential input voltage @ LNA (Rx off).....2 Vpk
Operating Temperature Range.....–20°C to +85°C
Storage Temperature Range.....–60°C to +150°C
Maximum Junction Temperature Tj.....+110°C
Note: Tj=Ta+PD*Rtheta, Rtheta = 25 C/W Where PD is the total power dissipation of the chip. This is dependent on mode (=duty cycle of the various blocks) and battery voltage

Notes: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD SENSITIVITY

The AD6548/9 is an ESD (electrostatic discharge) sensitive device. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur to devices subjected to high-energy electrostatic discharges. The AD6548/9 features proprietary ESD protection circuitry to dissipate high energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination before devices are removed.

SPECIFICATIONS

General + Regulators

Operating conditions as above, operating temperature –20°C TO +85°C

Parameter	Min	Typ	Max	Units	Test Conditions
Supply Current					
Off		0.05	2	µA	LDOs Off Vdd not present
Power Down		<1	10	µA	Vdd on, LDOs disabled
Wait Mode		1.5		mA	Cload 20pF
Alert		27	34	mA	Includes LO VCO
Receive		78	95	mA	
Transmit		120	150	mA	
Regulators					
LDO1					
Ground current unloaded		250		µA	
Start-up time			50	µSec	$C_{load} \leq 1uF$
Decoupling required for Guaranteed Stability	0.1		1	uF	Any ESR

SPECIFICATIONS

Receive Sections

Operating conditions as above, operating temperature –20°C TO +85°C, Input matched

Parameter	Min	Typ	Max	Units	Test Conditions / Comments
GSM850 and E-GSM 900 Receiver					All specifications are made on the full chain
Maximum Voltage Gain GSM 850	83.4	86	88.4	dB	GR=0
Maximum Voltage Gain E-GSM 900	83.4	86	88.4	dB	GR=0
Temperature Coefficient of Gain		-7		mdB/°C	
Gain Reduction	18	20	22	dB	GR=1
Input return loss	12	15		dB	Matched
Input Impedance GSM850		24-j51		Ω	Differential
E-GSM 900		24-j53			
DSB Noise Figure		3.0	4.5	dB	GR=0 includes baseband contribution gain set to maximum gain
Input Referred 1 dB Compression Point		-23		dBm	GR=0
		-20			GR=1
Input IP3	-18	-13		dBm	GR=0; Baseband Gain = 54 dB Input: –49 dBm tones @ f_c+800KHz and f_c+1600kHz
Input IP 2	38	45		dBm	Baseband Gain = 54 dB Input –30dBm tones @ f_c+6000kHz and f_c+6070kHz: see note
I/Q Gain error			0.5	dB	
Quadrature Phase Error	-3	0	3	degrees	
Noise Figure Degradation in the presence of blocker		3		dB	-26dBm @ 3MHz ,GR=0, Includes Synthesizer

IP2 Note (all Bands):
It can be shown that IP2 performance correlates to AM Suppression performance. The specified IP2 supports 3GPP TS 45.005 requirements with 0dB insertion loss from the antenna to IC pins. Additional insertion loss from the antenna improves overall AM Suppression performance

SPECIFICATIONS

Receive Section (continued)

Operating conditions as above, operating temperature –20°C TO +85°C, Input matched

Parameter	Min	Typ	Max	Units	Test Conditions / Comments
GSM1800 and GSM1900 Receivers					All specifications are made on the full chain
Maximum Voltage Gain GSM 1800	83.8	86.3	88.8	dB	GR=0
Maximum Voltage Gain GSM 1900	84.2	86.7	89.2	dB	GR=0
Temperature Coefficient of Gain		-8		mdB/°C	
Gain Reduction	18	20	22	dB	GR=1
Input return loss	12	15		dB	Matched
Input Impedance DCS 1800		8-j26		Ω	Differential
PCS 1900		10-j33			
DSB Noise Figure		3.0	4.5	dB	GR=0 includes baseband contribution gain set to maximum gain
Input Referred 1 dB Compression Point		-24		dBm	GR=0
		-21			GR=1
Input IP3	-18	-14		dBm	GR=0; Baseband Gain = 54 dB
					Input: –49 dBm tones @ f_c+800KHz and f_c+1600kHz
Input IP 2	36	43		dBm	Baseband Gain = 54 dB
					Input –30dBm tones @ f_c+6000kHz and f_c+6070kHz: see note
I/Q Gain error			0.4	dB	
Quadrature Phase Error	-2.5	2.0	6.5	degrees	
Noise Figure Degradation in the presence of blocker		4		dB	-29dBm at 3MHz ,GR=0

IP2 Note (all Bands):
It can be shown that IP2 performance correlates to AM Suppression performance. The specified IP2 supports 3GPP TS 45.005 requirements with 0dB insertion loss from the antenna to IC pins. Additional insertion loss from the antenna improves overall AM Suppression performance

SPECIFICATIONS

Receive Section (continued)

Operating conditions as above, operating temperature –20°C TO +85°C

Parameter	Min.	Typ.	Max.	Units	Test Conditions / Comments
Baseband Amplifiers					R_{load}>100 kΩ, C_{load}=47 pF ± 5%
Maximum Voltage Gain		60		dB	
Minimum Voltage Gain		3		dB	
Output 1 dB Compression Point		3		V_{pp}	Differential, Maximum Gain
Gain Control Range	56	57	58	dB	
Gain Control Resolution	2.5	3	3.5	dB	
Gain Control Linearity		1		dB	Integral Linearity
Baseband Filters					R_{load}>100 kΩ, C_{load}=47 pF ± 5%
3-dB Cutoff Frequency		200		kHz	All gain settings, Min/Max, after filter auto calibration
Gain Flatness			0.5	dBpp	DC to 80 kHz, Min/Max
Differential Group Delay		0.2	0.3	µs	DC to 80 kHz
Attenuation Template					After filter auto calibration
@ 200 kHz offset	0	3		dB	
@ 400 kHz offset	35			dB	
@ 600 kHz offset	50			dB	
@ 800 kHz offset	60			dB	
@ 1.6 MHz offset	80			dB	
@ 3 MHz offset	90			dB	
@ 6.5 MHz offset	100			dB	
@ >13 MHz offset	100			dB	
Output Common Mode Level	1.12	1.22	1.32	V	On I, IB, Q, and QB signals
Output Impedance		1.6		kΩ	Single Ended
Maximum residual DC			300	mV	Baseband gain 3dB to 54dB

SPECIFICATIONS

Transmit Section

Operating conditions as above, operating temperature –20°C TO +85°C

Parameter	Min	Typ	Max	Units	Test Conditions / Comments
Transmitter					Measured at TX VCO output. Includes contribution from the synthesizer I and Q Vin = 1Vpp (amplitude of I, IB, Q and QB = 0.5Vpp).
Low Band Modulation Template 200kHz		–35	–32	dB	GSM850/E-GSM900
Low Band Modulation Template 250kHz		–38	–35.5	dB	" "
Low Band Modulation Template 400kHz		–65	–62	dB	" "
High Band Modulation Template 200kHz		–36	–32	dB	DCS1800/PCS1900
High Band Modulation Template 250kHz		–39	–35.5	dB	" "
High Band Modulation Template 400kHz		–66	–62	dB	" "
GSM850/EGSM Phase Error		1	2.5	deg(rms)	
DCS1800/PCS1900 Phase Error		1	3.0	deg(rms)	
TxOP_LO Output[1]					
Operating Frequency Range	824		915	MHz	
Phase Noise @ 10MHz		-160	-154	dBc/Hz	
Phase Noise @ 20MHz		-166	-164	dBc/Hz	
Output Power	+6	+8	+10	dBm	Rl=50Ohm
Output VSWR		<1.5:1			50Ohm
Load Pull		+/-100		kHz	Open Loop, VSWR 2:1 all phases
Output Harmonics 2nd Harmonic		-20		dBc	
3rd Harmonic		-10		dBc	
TxOP_HI Output[1]					
Operating Frequency Range	1710		1910	MHz	
Phase Noise @ 20MHz		-162	-156	dBc/Hz	
Output Power	+5	+7	+9	dBm	Rl=50Ohm
Output VSWR		<1.5:1			50Ohm
Load Pull		+/-50		kHz	Open Loop, VSWR 2:1 all phases
Output Harmonics 2nd Harmonic		-20		dBc	
3rd Harmonic		-10		dBc	
Tx Baseband I/Q Inputs					
Input Resistance	30			kΩ	Each pin , 60k Differential
Input Capacitance		3		pF	
Input signal level	0.8	1.0	1.05	Vpp	Measured differentially at I or Q.
Common mode input level	1.14	1.2	1.26	V	

Note 1: The TxOP pins contain a DC voltage and should be AC coupled in the system.

SPECIFICATIONS

Fractional-N Synthesizer

Operating conditions as above, operating temperature –20°C to +85°C unless otherwise noted.

Parameter	Min	Typ	Max	Units	Test Conditions
Synthesizer					
SSB Phase Noise					
at 5kHz offset		-86		dBc/Hz	
at 400KHz offset		-122		dBc/Hz	
at 3MHz offset		-140		dBc/Hz	
Integrated Noise (DSB)			2.0	Deg(rms)	1KHz-1MHz
Channel Spacing		25		kHz	MOD = 1040 (Receive Mode)
		22.2222..		kHz	MOD = 1170 (GSM850/900 transmit mode)
		21.05263…		kHz	MOD = 1235 (GSM1800/1900 Transmit Mode)
Output frequency	2520		2985	MHz	
Lock Time			200	µs	Phase error <10 deg

Synthesizer Note:
Frequency division reduces phase noise contributions at the mixer port by:
9.5dB (Rx GSM850/E GSM)
3.5dB (Rx DCS/PCS)
9.8dB (Tx GSM850/E GSM)
3.4dB (Tx DCS/PCS)

SPECIFICATIONS

Reference Oscillator

Operating conditions as above, operating temperature –20°C to +85°C unless otherwise noted.

Parameter	Min	Typ	Max	Units	Test Conditions
AD6548 Crystal Oscillator[1]					26MHz operation
Output Frequency		26		MHz	Specified with recommended Crystal
AFC Capacitor Tuning Range	+/-20			ppm	25 deg C (63 Steps)
AFC Capacitor Step size	1.00	1.3	1.5	ppm	Around zero ppm operating point
Varactor Tuning Range[2]	+/-15			ppm	0.2V<VAFC<2.3V
Start-Up Time		<3	5	ms	Measured at REF_OP Output
AD6549 Input Reference Buffer					
Buffer Input Level	0.5		2	Vpp	AC coupled
Input Resistance (Shunt)	10			kΩ	
Input Capacitance (Shunt)			10	pF	
Phase Noise with Minimum input level @ 5KHz offset		-121		dBc/Hz	26 MHz measured at REF_OP
AD6548/9 Reference Output					
Output Frequency		26		MHz	26MHz Crystal
Output Swing	400	600		mVpp	Max load 20pF
Duty Cycle	45		55	%	50% duty cycle buffer input

Note 1:
Specification valid with a suitable crystal as defined in ADI Apps note GSM-0109
Note 2:
After selection of correct AFC capacitor value at 25 ºC as per GSM-0109 Apps note.
Crystal temperature-frequency behavior de-embedded

SPECIFICATION

Serial Port

Operating conditions as above, operating temperature –20°C to +85°C unless otherwise noted.

Parameter	Min	Typ	Max	Units	Test Conditions
Serial Interface					Timing Diagram Fig 14,15
V_{IH}, Input High Voltage	V_{DD} * 0.7			Volts	
V_{IL}, Input Low Voltage			V_{DD} * 0.3	Volts	
V_{OH}, Output High Voltage	V_{DD} - 0.2			Volts	I_{OH} = 100uA
V_{OL}, Output Low Voltage			0.2	Volts	I_{OL} = 100uA
Static Input Current	–1		1	µA	$0< V_{IN}< V_{DD}$
Serial Data Output Buffer Load			40	pF	
C_{IN}, Input Capacitance			5	pF	
Timing Conditions					
t_{clk_w} t_{clk_r} Serial Clock Period	38			nS	
t_{dst_w} t_{dst_r} Serial Data Set Up Time	8			nS	
t_{dhd_w} t_{dhd_r} Serial Data Hold Time	8			nS	
t_{hen_w} t_{hen_r} Enable Set Up Time to Clock High	10			nS	
t_{den_w} t_{den_r} Clock High to Enable High	8			nS	
t_{dhb_r} Serial hold on data bus after Enable High			5	nS	

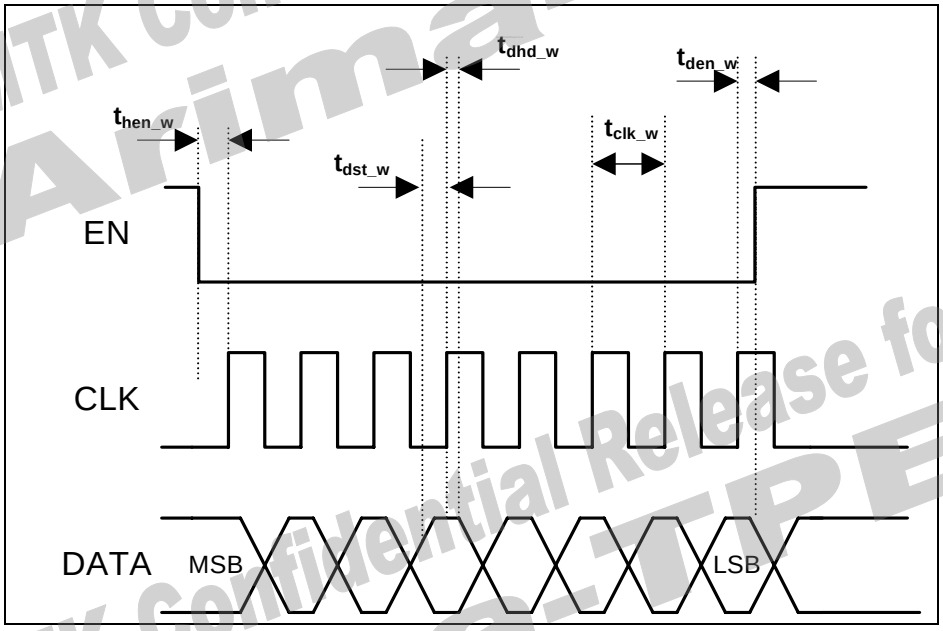
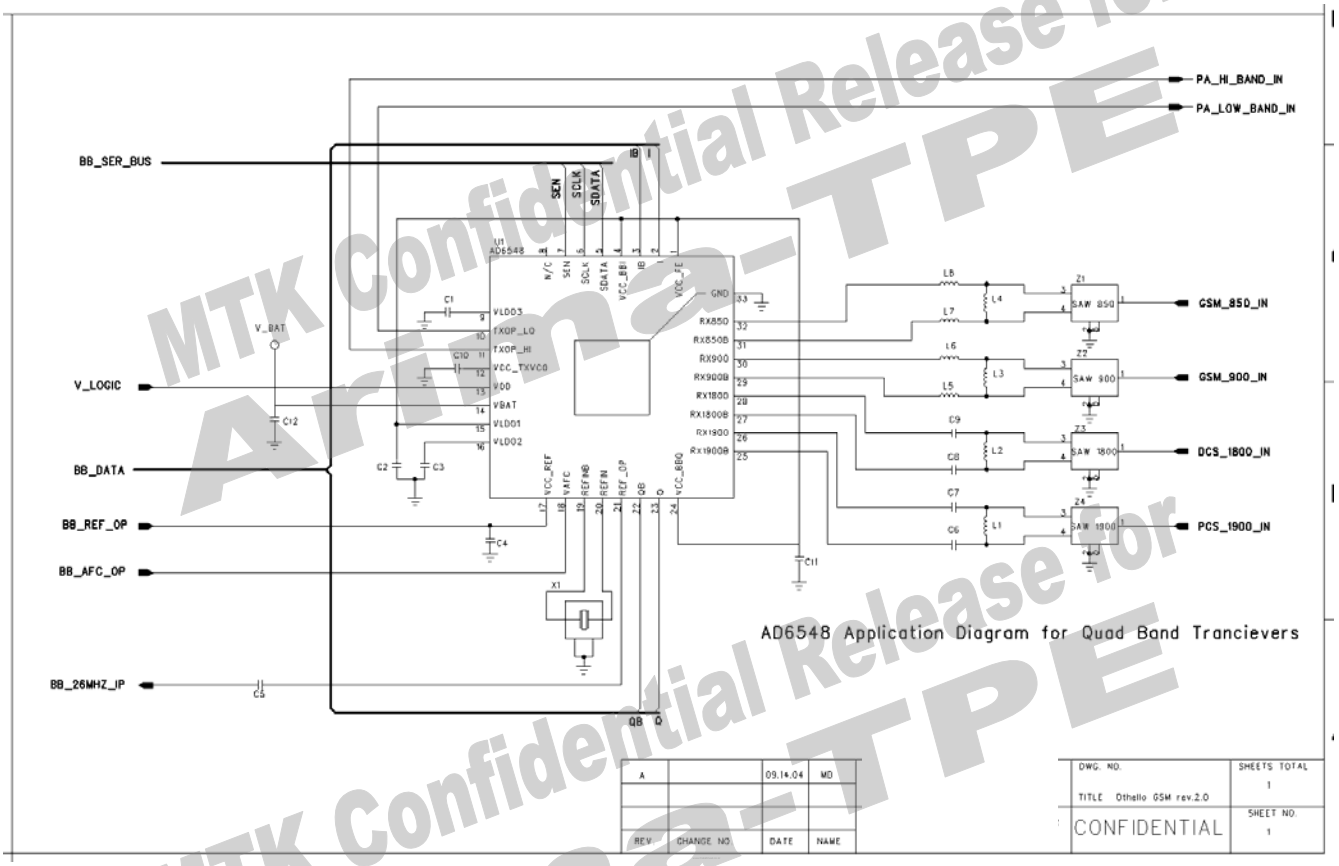


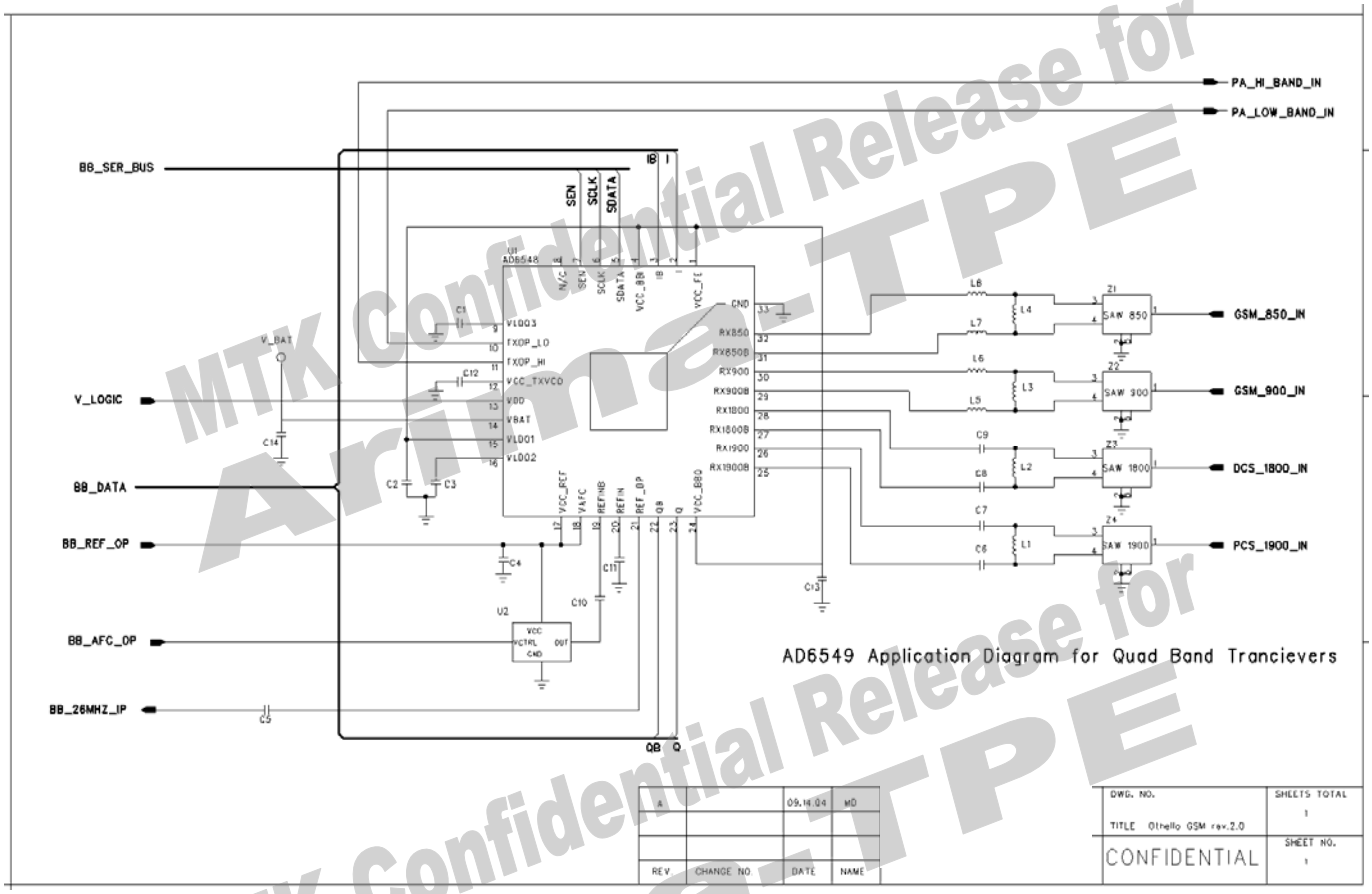
Figure 12 Serial Interface Timing – Write Operation



Ref	Value	Description	Package	Type / Manufacture
C1	33nF	Chip capacitor	0402	Murata, Rohm , TDK
C2 C4 C10 C12	100nF	Chip capacitor	0402	Murata, Rohm , TDK
C3	220nF	Chip Capacitor	0402	Murata, Rohm , TDK
C5	1nF	Chip Capacitor	0402	Murata, Rohm , TDK
C11	39pF	Chip capacitor	0402	Murata, Rohm , TDK
C6,C7	4.7pF	Chip Capacitor[1]	0402	Murata, Rohm , TDK
C8,C9	8.2pF	Chip Capacitor[1]	0402	Murata, Rohm , TDK
L1,L2	5.6nH	Chip Capacitor[1]	0402	Ceramic Multilayer eg Toko, or Murata, or Panasonic,
L3,L4	18nH	Chip Capacitor[1]	0402	Ceramic Multilayer eg Toko, or Murata, or Panasonic,
L5,L6	1.8nH	Chip Inductor[1]	0402	Ceramic Multilayer eg Toko, or Murata, or Panasonic,
L7,L8	2.2nH	Chip Inductor[1]	0402	Ceramic Multilayer eg Toko, or Murata, or Panasonic,
Z1		850 MHz RX SAW	Chip Scale	Murata or EPCOS
Z2		900 MHz RX SAW	Chip Scale	Murata or EPCOS
Z3		1800 MHz RX SAW	Chip Scale	Murata or EPCOS
Z4		1900 MHz RX SAW	Chip Scale	Murata or EPCOS
X1		26 MHz Crystal		NDK or Toyocm, or KSS
U1		AD6548	5x5 LFCSP	MediaTek

Note 1: Matching component: Exact will be affected by SAW specification & PCB layout

Figure 13 AD6548 Typical Applications Diagram & Bill of Materials



Ref	Value	Description	Package	Type / Manufacture
C1	33nF	Chip capacitor	0402	Murata, Rohm , TDK
C2,C12, C14	100nF	Chip capacitor	0402	Murata, Rohm , TDK
C3	220nF	Chip Capacitor	0402	Murata, Rohm , TDK
C4	15pF	Chip Capacitor	0402	Murata, Rohm , TDK
C13	39pF	Chip Capacitor	0402	Murata, Rohm , TDK
C6,C7	4.7pF	Chip Capacitor[1]	0402	Murata, Rohm , TDK
C8,C9	8.2pF	Chip Capacitor[1]	0402	Murata, Rohm , TDK
C5,C10,C11	1 nF	Chip Capacitor	0402	Murata, Rohm , TDK
L1,L2	5.6nH	Chip Capacitor[1]	0402	Ceramic Multilayer eg Toko, or Murata, or Panasonic,
L3,L4	18nH	Chip Capacitor[1]	0402	Ceramic Multilayer eg Toko, or Murata, or Panasonic,
L5,L6	1.8nH	Chip Inductor[1]	0402	Ceramic Multilayer eg Toko, or Murata, or Panasonic,
L7,L8	2.2nH	Chip Inductor[1]	0402	Ceramic Multilayer eg Toko, or Murata, or Panasonic,
Z1		850 MHz RX SAW	Chip Scale	Murata or EPCOS
Z2		900 MHz RX SAW	Chip Scale	Murata or EPCOS
Z3		1800 MHz RX SAW	Chip Scale	Murata or EPCOS
Z4		1900 MHz RX SAW	Chip Scale	Murata or EPCOS
U2		26 MHz VCTCXO		Toyocm, Murata,etc.
U1		AD6549	5x5 LFCSP	MediaTek

Note 1: Matching component: Exact will be affected by SAW specification & PCB layout

Figure 14 AD6549 Typical Applications Diagram & Bill of Materials

PACKAGE DIMENSIONS

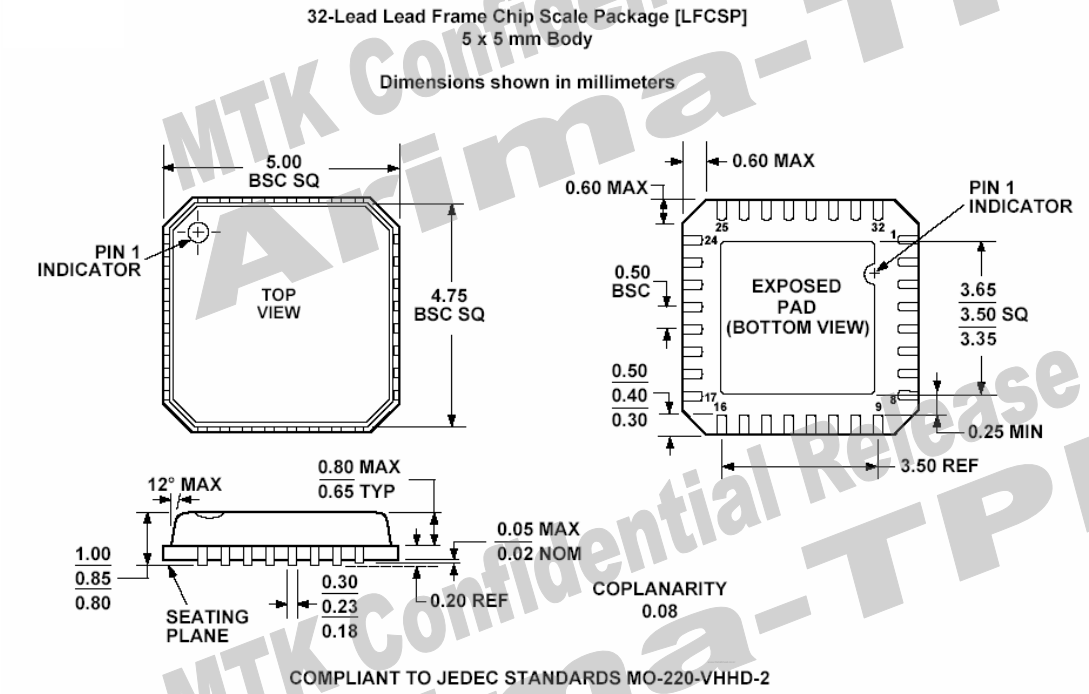


Figure 15 Package Dimensions

CHANGE LIST

Revision	Chapter Title / Page	Description
Rev B	Page 1 & 15……	Vdd voltage increased from 2.9 to 3v
	Page 10 Note 1 & Fig 9…..	Modified LDO off timing
	Page 12 Fig 11 & Part 7 of text…	Modified LDO off timing
	Page 21 (Synth note)	Corrected band references
	Page 22 Reference oscillator Spec	Updated verbiage and added Max start-up time