1-Line To 10-Line Clock Driver With 3-State Outputs

Features

- Low Output Skew, Low Pulse Skew for Clock-Distribution and Clock-Generation Applications.
- Operates at 3.3V Supply Voltage.
- LVTTL-Compatible Inputs and Outputs.
- Supports Mixed-Mode Signal Operation. (5V Input and Output Voltages With 3.3V Supply Voltage).
- Distributes One Clock Input to Ten Outputs.
- Outputs have Internal Series Damping Resistor to Reduce Transmission Line Effects.
- Distributed V_{CC} and Ground Pins Reduce Switching Noise.
- Package Options Include Plastic Small-Outline and Shrink Small-Outline Packages.

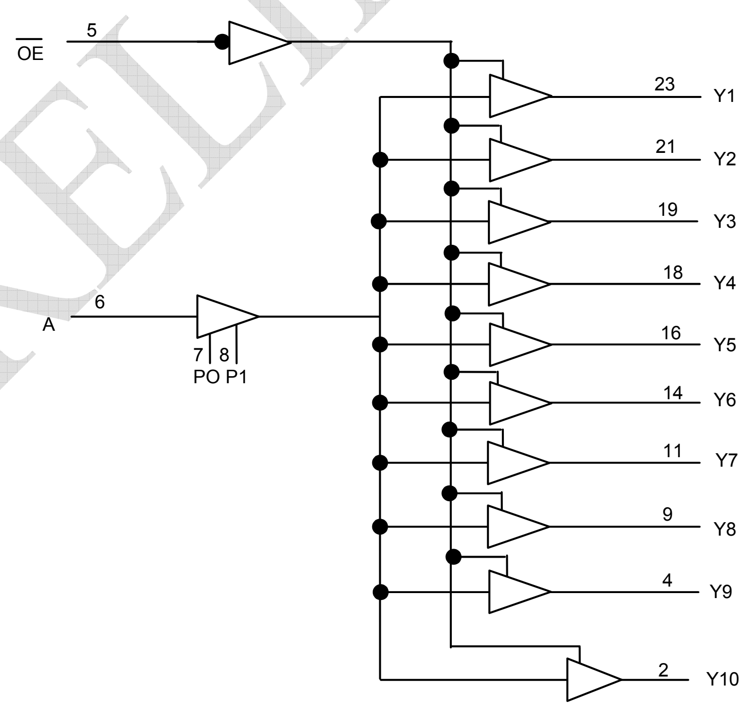
Product Description

The ASM2P2351AH is a high-performance clock-driver circuit that distributes one input (A) to ten outputs (Y) with minimum skew for clock distribution. The output-enable ($\overline{OE}$) input disables the outputs to a high-impedance state. Each output has an internal series damping resistor to improve signal integrity at the load. The ASM2P2351AH operates at nominal 3.3V Supply Voltage.

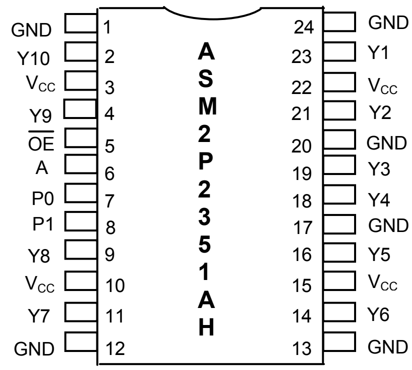
The propagation delays are adjusted at the factory using the P0 and P1 pins. The factory adjustments ensure that the part-to-part skew is minimized and is kept within a specified window. Pins P0 and P1 are not intended for customer use and should be connected to GND.

The ASM2P2351AH is characterized for operation from 0°C to 70°C.

Logic Diagram (Positive Logic)



Pin Configuration



SSOP/ SOIC Packages
TOP VIEW

Pin Description

Pin #	Pin Name	Typ	Description
1	GND	P	Ground Pin
2	Y10	O	Output 10
3	V_{CC}	P	Power Supply Pin
4	Y9	O	Output 9
5	$\overline{OE}$	I	Output Enable Pin. When this pin is low, the outputs Y[1:10] are enabled and when this pin is high , the outputs Y[1:10] are disabled.
6	A	I	Input Clock
7	P0	-	No Connect
8	P1	-	No Connect
9	Y8	O	Output 8
10	V_{CC}	P	Power Supply
11	Y7	O	Output 7
12	GND	P	Ground Pin
13	GND	P	Ground Pin
14	Y6	O	Output 6
15	V_{CC}	P	Power Supply
16	Y5	O	Output 5
17	GND	P	Ground Pin
18	Y4	O	Output 4
19	Y3	O	Output 3
20	GND	P	Ground Pin
21	Y2	O	Output 2
22	V_{CC}	P	Power Supply
23	Y1	O	Output 1
24	GND	P	Ground Pin

Function Table

Inputs		Outputs
A	$\overline{OE}$	In
L	H	Z
H	H	Z
L	L	L
H	L	H

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CC}	Voltage on Supply pin with respect to Ground	-0.5 to +4.6	V
V_{IN}	Voltage on any pin with respect to Ground	-0.5 to +7.0	V
t_{STG}	Storage temperature	-65 to +125	°C
t_A	Operating temperature	0 to 70	°C
t_s	Max. Soldering Temperature (10 sec)	260	°C
t_J	Junction Temperature	150	°C
t_{DV}	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

Recommended operating conditions (see Note 3)

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply voltage	3	3.6	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	5.5	V
I_{OH}	High-level output current		–12	mA
I_{OL}	Low-level output current		12	mA
f_{clock}	Input clock frequency		100	MHz
T_A	Operating free air temperature	0	70	°C

NOTE 3: Unused pins (input or I/O) must be held high or low.

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Electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

Parameter	Test Conditions		Min	Typ	Max	Unit
V_{IK}	V_{CC} = 3 V, I_I = –18 mA				–1.2	V
V_{OH}	V_{CC} = 3 V, I_{OH} = – 12 mA		2			V
V_{OL}	V_{CC} = 3 V, I_{OL} = 12 mA				0.8	V
I_I	V_{CC} = 3.6 V, V_I = V_{CC} or GND				± 1	mA
I_O[1]	V_{CC} = 3.6 V, V_O = 2.5 V		–7		–70	mA
I_{OZ}	V_{CC} = 3.6 V, V_{CC} = 3 V				± 10	mA
I_{CC}	V_{CC} = 3.6 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			0.3	mA
		Outputs low			15	
		Outputs disabled			0.3	
C_i	V_I = V_{CC} or GND, V_{CC} = 3.3 V, f = 10 MHz			4		pF
C_o	V_O = V_{CC} or GND, V_{CC} = 3.3 V, f = 10 MHz			6		pF

Note: 1 Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

Switching Characteristics, C_L = 50 pF (see Figures 1 and 2)

Parameter	From (Input)	To (Output)	ASM2P2351A V_{CC} = 3.3 V, TA = 25°C			ASM2P2351AH V_{CC} = 3 V to 3.6 V, T_A = 0°C to 70°C		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	A	Y	3.8	4.3	4.8			nS
t_{PHL}			3.6	4.1	4.6			
t_{PZH}	$\overline{OE}$	Y	2.4	4.9	6.0	1.8	6.9	nS
t_{PZL}			2.4	4.3	6.0	1.8	6.9	
t_{PHZ}	$\overline{OE}$	Y	2.2	4.4	6.3	2.1	7.1	nS
t_{PLZ}			2.2	4.6	6.3	2.1	7.3	
$t_{sk(o)}$	A	Y		0.3	0.5		0.5	nS
$t_{sk(p)}$	A	Y		0.2	0.8		0.8	nS
$t_{sk(pr)}$	A	Y			1		1	nS
t_r	A	Y					2.5	nS
t_f	A	Y					2.5	nS

Switching Characteristics temperature and V_{CC} coefficients over recommended operating free-air temperature and V_{CC} range (see Note 3)

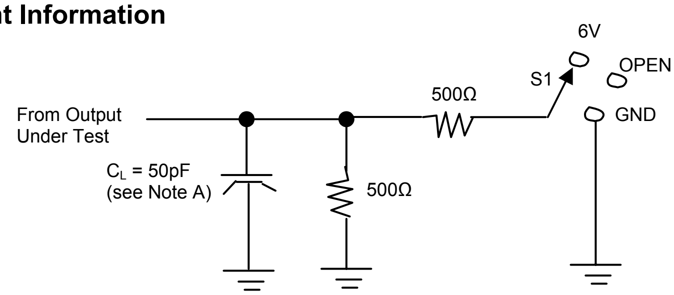
Parameter		From (Input)	To (Output)	Min	Max	Unit
t_{PLH}(T)	Average temperature coefficient of low to high propagation delay	A	Y		85^1	pS/10°C
t_{PHL}(T)	Average temperature coefficient of high to low propagation delay	A	Y		50^1	pS/10°C
$t_{PLH}(V_{CC})$	Average V_{CC} coefficient of low to high propagation delay	A	Y		-145^2	pS/ 100 mV
$t_{PHL}(V_{CC})$	Average V_{CC} coefficient of high to low propagation delay	A	Y		-100^2	pS/ 100 mV

Note: 1 t_{PLH}(T) and t_{PHL}(T) are virtually independent of V_{CC}.

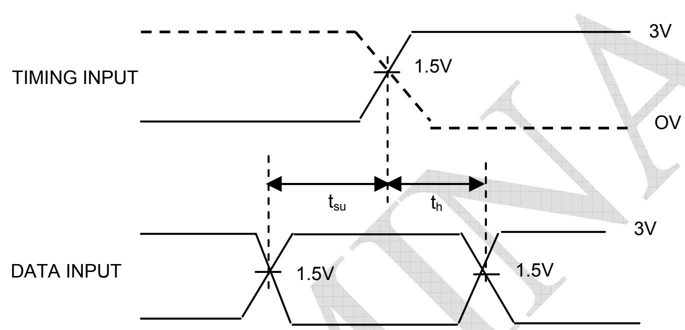
2 $t_{PLH}(V_{CC})$ and $t_{PHL}(V_{CC})$ are virtually independent of temperature.

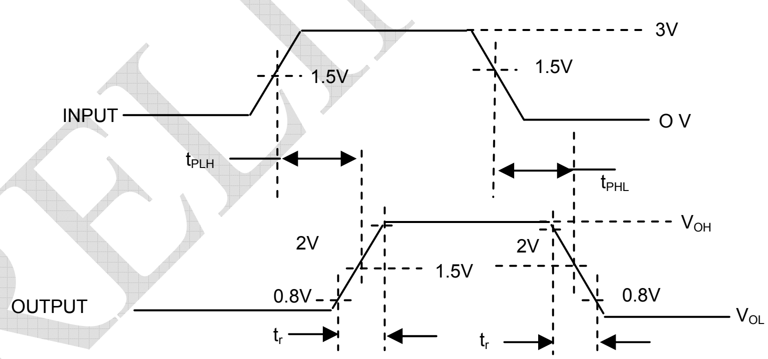
3 This data was extracted from characterization material and are not tested at the factory.

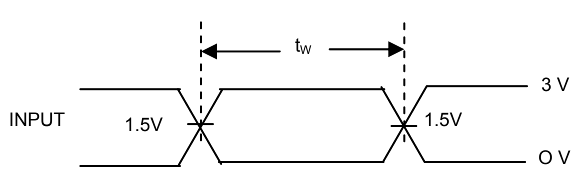
Parameter Measurement Information



LOAD CIRCUIT







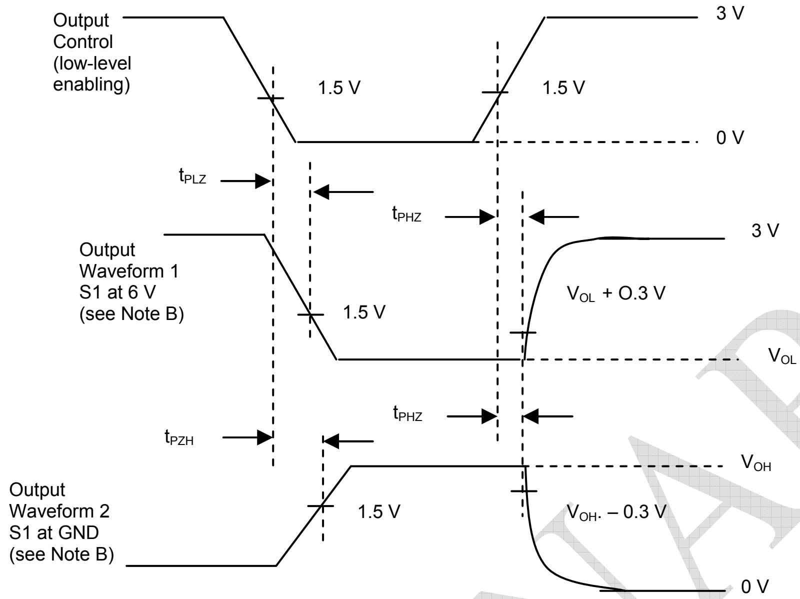


Figure 1. Load Circuit and Voltage Waveforms

NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR 3 10 MHz, ZO = 50Ω, tr 3 2.5 nS, tf 3 2.5 nS.

D. The outputs are measured one at a time with one transition per measurement.

Parameter Measurement Information

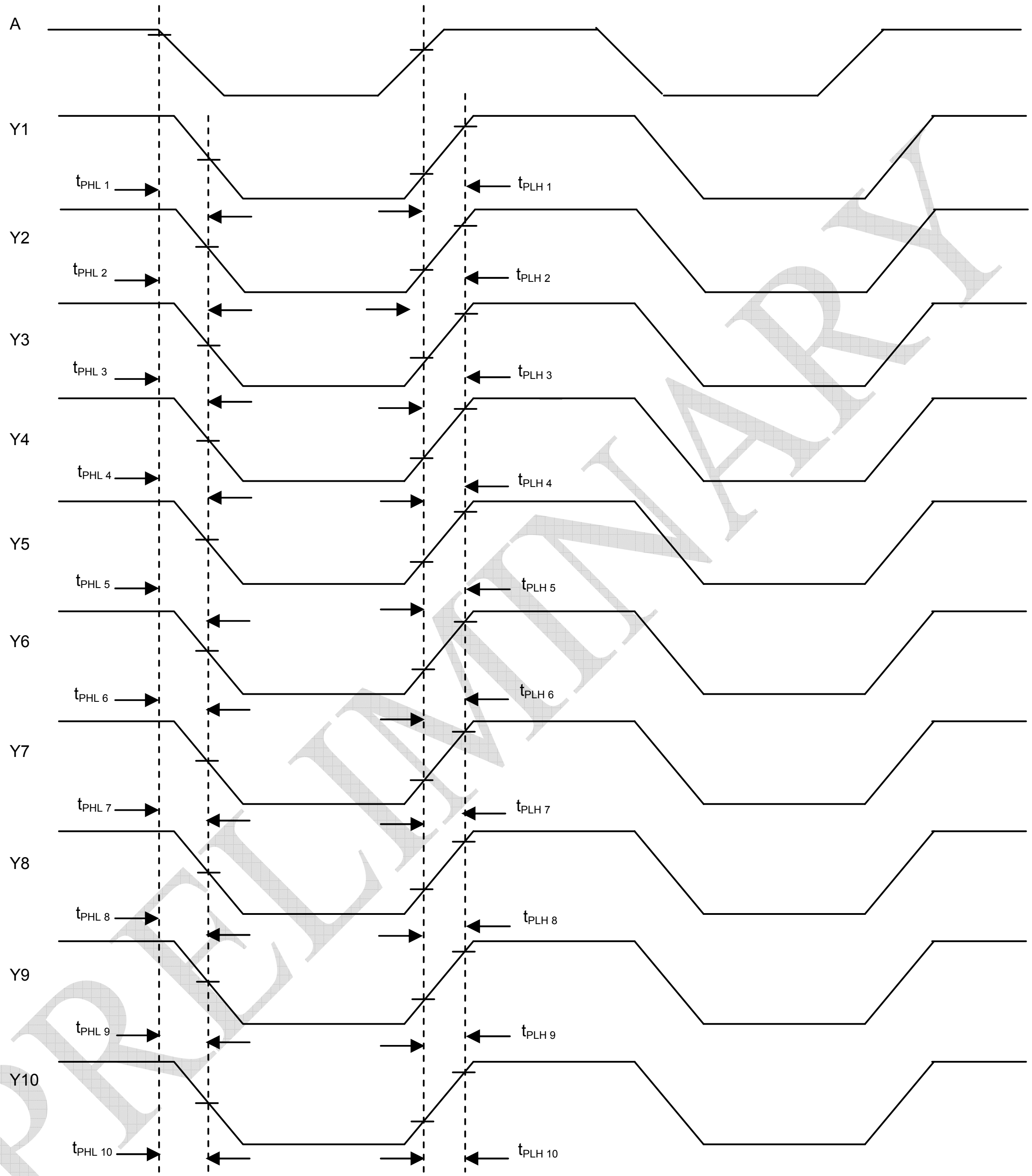


Figure 2. Waveforms for Calculation of $t_{sk(o)}$, $t_{sk(p)}$, $t_{sk(pr)}$

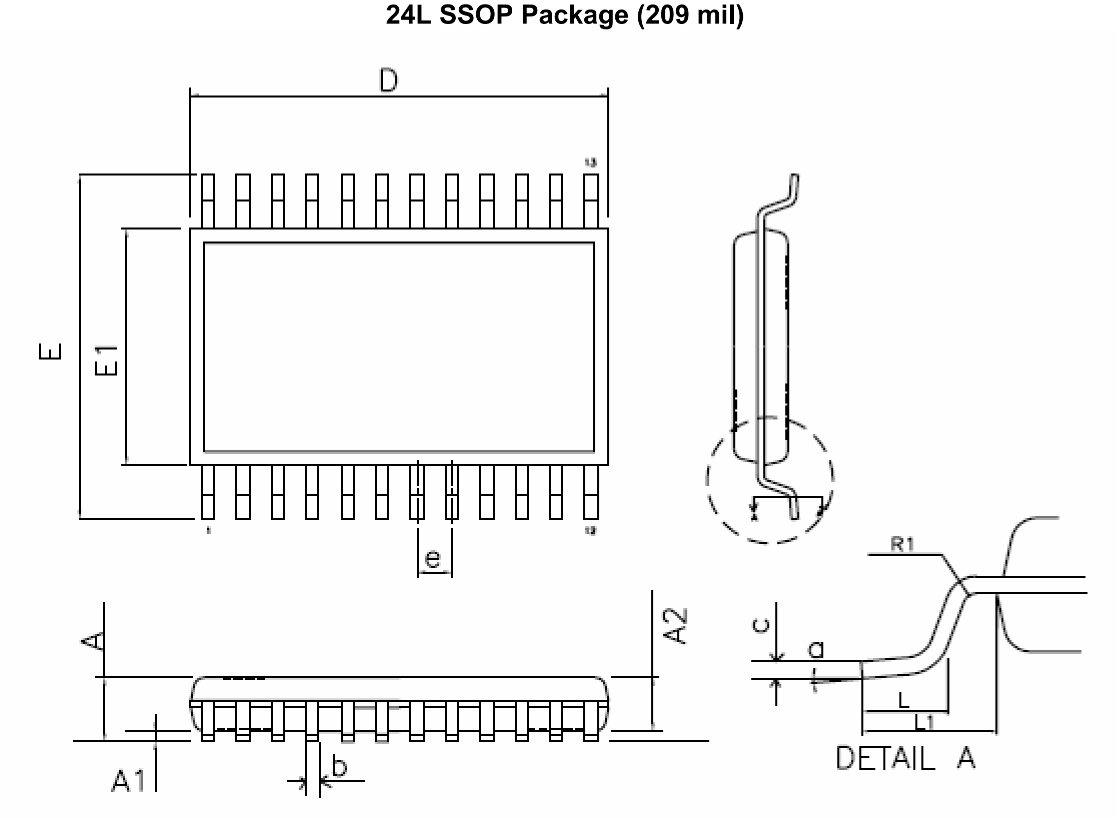
NOTES: A. Output skew, $t_{sk(o),}$ is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10)
- The difference between the fastest and slowest of t_{PHLn} (n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10)

B. Pulse skew, $t_{sk(p)}$, is calculated as the greater of | t_{PLH}n – t_{PHLn} | (n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10).

C. Process skew, $t_{sk(pr)}$, is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10) across multiple devices under identical operating conditions
- The difference between the fastest and slowest of t_{PHLn} (n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10) across multiple devices under identical operating conditions

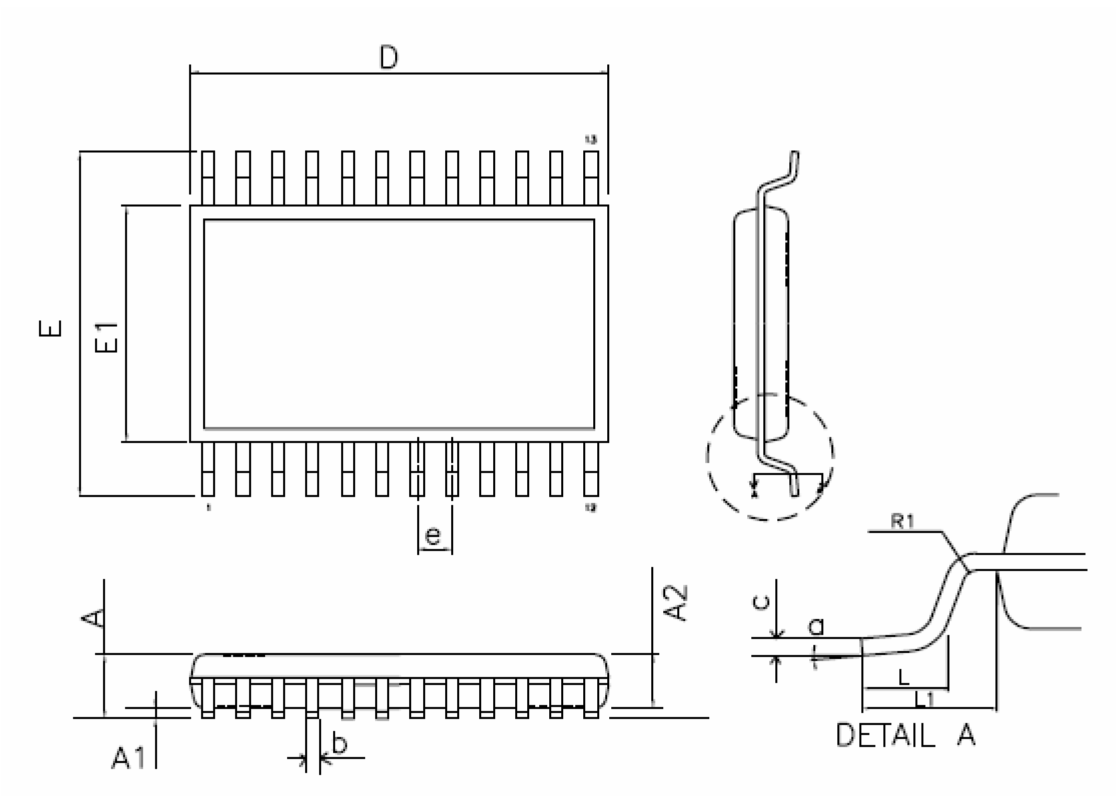
Package Information

24L SSOP Package (209 mil)



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	….	0.079	…	2.0
A1	0.002	…	0.05	…
A2	0.065	0.073	1.65	1.85
D	0.315	0.331	8.00	8.40
L	0.021	0.037	0.55	0.95
E	0.295	0.319	7.50	8.10
E1	0.197	0.220	5.00	5.60
R1	0.004	….	0.09	…..
b	0.009	0.015	0.22	0.38
c	0.004	0.010	0.09	0.25
L1	0.050REF		1.25 REF	
e	0.026 BSC		0.65 BSC	
a	0°	8°	0°	8°

24L SOIC Package (300 mil)



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
A2	0.088	0.094	2.25	2.40
D	0.598	0.614	15.20	15.60
L	0.016	0.050	0.40	1.27
E1	0.291	0.299	7.40	7.60
R1	0.003	….	0.08	…..
b	0.013	0.022	0.33	0.56
c	0.009	0.015	0.23	0.38
E	0.394	0.419	10.00	10.65
e	0.050 BSC		1.27 BSC	
a	0°	8°	0°	8°

Ordering Information

Part Number	Marking	Package Type	Temperature
ASM2P2351AHF-24AR	2P2351AHF	24-Pin SSOP, TAPE & REEL, Pb Free	Commercial
ASM2P2351AHF-24AT	2P2351AHF	24-Pin SSOP, TUBE, Pb Free	Commercial
ASM2P2351AHF -24SR	2P2351AHF	24-Pin SOIC, TAPE & REEL, Pb Free	Commercial
ASM2P2351AHF-24ST	2P2351AHF	24-Pin SOIC, TUBE, Pb Free	Commercial
ASM2P2351AF-24AR	2P2351AF	24-Pin SSOP, TAPE & REEL, Pb Free	Commercial
ASM2P2351AF-24AT	2P2351AF	24-Pin SSOP, TUBE, Pb Free	Commercial
ASM2P2351AF -24SR	2P2351AF	24-Pin SOIC, TAPE & REEL, Pb Free	Commercial
ASM2P2351AF-24ST	2P2351AF	24-Pin SOIC, TUBE, Pb Free	Commercial
ASM2P2351AHG-24AR	2P2351AHG	24-Pin SSOP, TAPE & REEL, Green	Commercial
ASM2P2351AHG-24AT	2P2351AHG	24-Pin SSOP, TUBE, Green	Commercial
ASM2P2351AHG -24SR	2P2351AHG	24-Pin SOIC, TAPE & REEL, Green	Commercial
ASM2P2351AHG-24ST	2P2351AHG	24-Pin SOIC, TUBE, Green	Commercial
ASM2P2351AG-24AR	2P2351AG	24-Pin SSOP, TAPE & REEL, Green	Commercial
ASM2P2351AG-24AT	2P2351AG	24-Pin SSOP, TUBE, Green	Commercial
ASM2P2351AG -24SR	2P2351AG	24-Pin SOIC, TAPE & REEL, Green	Commercial
ASM2P2351AG-24ST	2P2351AG	24-Pin SOIC, TUBE, Green	Commercial
ASM2P2351AH-24AR	2P2351AH	24-Pin SSOP, TAPE & REEL	Commercial
ASM2P2351AH-24AT	2P2351AH	24-Pin SSOP, TUBE	Commercial
ASM2P2351AH -24SR	2P2351AH	24-Pin SOIC, TAPE & REEL	Commercial
ASM2P2351AH-24ST	2P2351AH	24-Pin SOIC, TUBE	Commercial
ASM2P2351A-24AR	2P2351A	24-Pin SSOP, TAPE & REEL	Commercial
ASM2P2351A-24AT	2P2351A	24-Pin SSOP, TUBE	Commercial
ASM2P2351A -24SR	2P2351A	24-Pin SOIC, TAPE & REEL	Commercial
ASM2P2351A-24ST	2P2351A	24-Pin SOIC, TUBE	Commercial

Device Ordering Information

A S M 2 P 2 3 5 1 A H F - 2 4 A R

- R = Tape & reel, T = Tube or Tray
- O = SOT, S = SOIC, T = TSSOP, A = SSOP, V = TVSOP, B = BGA, Q = QFN, U = MSOP, E = TQFP, L = LQFP, U = MSOP, P = PDIP, D = QSOP, X = SC-70
- DEVICE PIN COUNT
- F = LEAD FREE AND RoHS COMPLIANT PART
  G = GREEN PACKAGE
- PART NUMBER
- X= Automotive (-40C to +125C) I= Industrial (-40C to +85C) P or n/c = Commercial (0C to +70C)

  1 = Reserved
  2 = Non PLL based
  3 = EMI Reduction
  4 = DDR support products
  5 = STD Zero Delav Buffer
  6 = Power Management
  7 = Power Management
  8 = Power Management
  9 = Hi Performance
  0 = Reserved
- ALLIANCE SEMICONDUCTOR MIXED SIGNAL PRODUCT

Licensed under US patent Nos 5,488,627 and 5,631,920.

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Advance Information
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Document Version: v0.2

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to Alliance Semiconductor, dated 11-11-2003