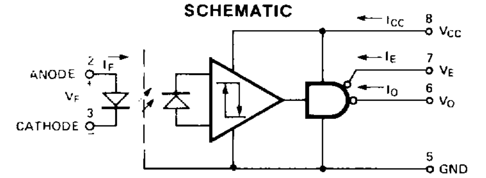
# HEWLETT PACKARD

# 20 M BAUD HIGH CMR LOGIC GATE OPTOCOUPLER

## HCPL-2400
## HCPL-2411

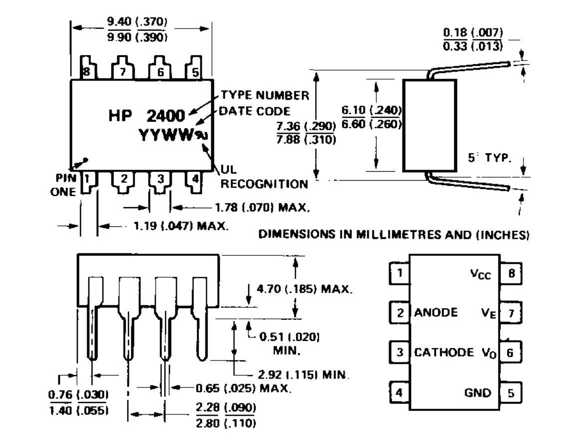
SCHEMATIC




TRUTH TABLE
(POSITIVE LOGIC)

| LED | ENABLE | OUTPUT |
|---|---|---|
| ON | L | L |
| OFF | L | H |
| ON | H | Z |
| OFF | H | Z |

OUTLINE DRAWING




# Features

- **HIGH SPEED: 40 MBd TYPICAL DATA RATE**
- **HIGH COMMON MODE REJECTION**
- **HCPL-2400 = 1kV/μs @ 50 $V_{CM}$**
- **HCPL-2411 = 1kV/μs @ 300 $V_{CM}$**
- **AC PERFORMANCE GUARANTEED OVER TEMPERATURE**
- **COMPATIBLE WITH TTL, STTL, LSTTL, AND HCMOS LOGIC FAMILIES**
- **HIGH SPEED AlGaAs EMITTER**
- **THREE STATE OUTPUT (NO PULL-UP RESISTOR REQUIRED)**
- **HIGH POWER SUPPLY NOISE IMMUNITY**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 2500 Vac, 1 MINUTE**
- **VDE 0883 APPROVAL AVAILABLE**
- **MIL-STD-1772 VERSION AVAILABLE (HCPL-5400/1)**

# Applications

- **ISOLATION OF HIGH SPEED LOGIC SYSTEMS**
- **COMPUTER-PERIPHERAL INTERFACES**
- **ISOLATED BUS DRIVER (NETWORKING APPLICATIONS)**
- **SWITCHING POWER SUPPLIES**
- **GROUND LOOP ELIMINATION**
- **HIGH SPEED DISK DRIVE I/O**
- **DIGITAL ISOLATION FOR A/D, D/A CONVERSION**
- **PULSE TRANSFORMER REPLACEMENT**

# Description

The HCPL-2400/11 high speed optocouplers combine an 820 nm AlGaAs light emitting diode with a high speed photo-detector. This combination results in very high data rate capability and low input current. The three state output eliminates the need for a pull-up resistor and allows for direct drive of data buses. The hysteresis provides differential mode noise immunity and minimizes the potential for output signal chatter. Improved power supply rejection minimizes the need for special power supply bypassing precautions.

The electrical and switching characteristics of the HCPL-2400/11 are guaranteed over the temperature range of 0°C to 70°C.

The HCPL-2400/11 are compatible with TTL, STTL, LSTTL and HCMOS logic families. When Schottky type TTL devices (STTL) are used, a data rate performance of 20 MBd over temperature is guaranteed when using the application circuit of Figure 13. Typical data rates are 40 MBd.

### Recommended Operating Conditions

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 4.75 | 5.25 | Volts |
| Input Current (High) | $I_{F(ON)}$ | 4 | 8 | mA |
| Input Voltage (Low) | $V_{F(OFF)}$ | — | 0.8 | Volts |
| Enable Voltage (Low) | $V_{EL}$ | 0 | 0.8 | Volts |
| Enable Voltage (High) | $V_{EH}$ | 2.0 | $V_{CC}$ | Volts |
| Operating Temperature | $T_A$ | 0 | 70° | °C |
| Fan Out | N | | 5 | TTL Loads |

OPTOCOUPLERS

# Absolute Maximum Ratings

(No derating required up to 85° C)

| Parameter | Symbol | Min. | Max. | Units | Note |
|---|---|---|---|---|---|
| Storage Temperature | $T_S$ | −55 | 125 | °C | |
| Operating Temperature | $T_A$ | −40 | 85 | °C | |
| Lead Solder Temperature | 260° C for 10 s. (1.6 mm below seating plane) | | | | |
| Average Forward Input Current | $I_F$ | | 10.0 | mA | |
| Peak Forward Input Current | $I_{FPK}$ | | 20.0 | mA | 9 |
| Reverse Input Voltage | $V_R$ | | 3.0 | V | |
| Supply Voltage | $V_{CC}$ | 0 | 7.0 | V | |
| Three State Enable Voltage | $V_E$ | −0.5 | 10.0 | V | |
| Average Output Collector Current | $I_O$ | −25.0 | 25.0 | mA | |
| Output Collector Voltage | $V_O$ | −0.5 | 10.0 | V | |
| Output Collector Power Dissipation | $P_O$ | | 40.0 | mW | |

# Electrical Specifications

For $0°C \leq T_A \leq 70°C$, $4.75\ V \leq V_{CC} \leq 5.25\ V$, $4\ mA \leq I_{F(ON)} \leq 8\ mA$, $2.0\ V \leq V_{EH} \leq 5.25$, $0\ V \leq V_{EL} \leq 0.8\ V$, $0\ V \leq V_{F(OFF)} \leq 0.8\ V$ except where noted. All typicals at $T_A = 25°C$, $V_{CC} = 5\ V$, $I_{F(ON)} = 6.0\ mA$, $V_{F(OFF)} = 0\ V$ except where noted. See note 9.

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions | | Figure | Note |
|---|---|---|---|---|---|---|---|---|---|
| Logic Low Output Voltage | $V_{OL}$ | | | 0.5 | Volts | $I_{OL} = 8.0$ mA (5 TTL Loads) | | 1 | |
| Logic High Output Voltage | $V_{OH}$ | 2.4 | | | Volts | $I_{OH} = -4.0$ mA | | 2 | |
| Output Leakage Current | $I_{OHH}$ | | | 100 | μA | $V_O = 5.25$ V | $V_F = 0.8$ V | | |
| Logic High Enable Voltage | $V_{EH}$ | 2.0 | | | Volts | | | | |
| Logic Low Enable Voltage | $V_{EL}$ | | | 0.8 | Volts | | | | |
| Logic High Enable Current | $I_{EH}$ | | | 20 | μA | $V_E = 2.4$ V | | | |
| | | | | 100 | μA | $V_E = 5.25$ V | | | |
| Logic Low Enable Current | $I_{EL}$ | | −0.28 | −0.4 | mA | $V_E = 0.4$V | | | |
| Logic Low Supply Current | $I_{CCL}$ | | 19 | 26 | mA | $V_{CC} = 5.25$ V | | | |
| Logic High Supply Current | $I_{CCH}$ | | 17 | 26 | mA | $V_E = 0$ V | | | |
| High Impedance State Supply Current | $I_{CCZ}$ | | 22 | 28 | mA | $V_{CC} = 5.25$ V<br>$V_E = 5.25$ V | | | |
| High Impedance State Output Current | $I_{OZL}$ | | | 20 | μA | $V_O = 0.4$V | $V_E = 2$ V | | |
| | $I_{OZH}$ | | | 20 | μA | $V_O = 2.4$ V | | | |
| | $I_{OZH}$ | | | 100 | μA | $V_O = 5.25$ V | | | |
| Logic Low Short Circuit Output Current | $I_{OSL}$ | | 52 | | mA | $V_O = V_{CC} = 5.25$ V | $I_F = 8$ mA | | 1 |
| Logic High Short Circuit Output Current | $I_{OSH}$ | | −45 | | mA | $V_{CC} = 5.25$ V | $I_F = 0$ mA,<br>$V_O$ = GND | | 1 |
| Input Current Hysteresis | $I_{HYS}$ | | 0.25 | | mA | $V_{CC} = 5$ V | | 3 | |
| Input Forward Voltage | $V_F$ | 1.1 | 1.3 | 1.5 | Volts | $T_A = 25°C$ | $I_F = 8$ mA | 4 | |
| | | 1.0 | | 1.55 | | | | | |
| Input Reverse Breakdown Voltage | $BV_R$ | 3.0 | 5.0 | | Volts | $T_A = 25°C$ | $I_R = 10\ \mu A$ | | |
| | | 2.0 | | | | | | | |
| Input Diode Temperature Coefficient | $\frac{\Delta V_F}{\Delta T_A}$ | | −1.44 | | mV/°C | $I_F = 6$ mA | | 4 | |
| Input-Output Insulation | $V_{ISO}$ | 2500 | | | $V_{RMS}$ | RH ≤ 50%, t = 1 min.<br>$T_A = 25°C$ | | | 2 |
| Input-Output Resistance | $R_{I-O}$ | | $10^{12}$ | | ohms | $V_{I-O} = 500$ VDC | | | 2 |
| Input-Output Capacitance | $C_{I-O}$ | | 0.6 | | pF | f = 1 MHz, $V_{I-O} = 0$ V dc | | | 2 |
| Input Capacitance | $C_{IN}$ | | 20 | | pF | f = 1 MHz, $V_F = 0$V, Pins 2 and 3 | | | |

# Switching Specifications

$0°C \le T_A \le 70°C$, $4.75\ V \le V_{CC} \le 5.25\ V$, $0.0\ V \le V_{EN} \le 0.8\ V$, $4\ mA \le I_F \le 8.0\ mA$. All typicals $V_{CC} = 5\ V$, $T_A = 25°C$, $I_F = 6.0\ mA$ except where noted.

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions | Figure | Note |
|---|---|---|---|---|---|---|---|---|
| Propagation Delay Time to Logic Low Output Level | $t_{PHL}$ | | | 55 | ns | $I_{F(ON)} = 7.0\ mA$ | 5, 6, 7 | 4 |
| | | 15 | 33 | 60 | ns | | 5, 6, 7 | 3 |
| Propagation Delay Time to Logic High Output Level | $t_{PLH}$ | | | 55 | ns | $I_{F(ON)} = 7.0\ mA$ | 5, 6, 7 | 4 |
| | | 15 | 30 | 60 | ns | | 5, 6, 7 | 3 |
| Pulse Width Distortion | $\lvert t_{PHL} - t_{PLH} \rvert$ | | 2 | 15 | ns | $I_{F(ON)} = 7.0\ mA$ | 5, 8 | 4 |
| | | | 3 | 25 | ns | | 5, 8 | |
| Propagation Delay Skew | $t_{PSK}$ | | | 35 | ns | | 15, 16 | 5 |
| Output Rise Time | $t_r$ | | 20 | | ns | | 5 | |
| Output Fall Time | $t_f$ | | 10 | | ns | | 5 | |
| Output Enable Time to Logic High | $t_{PZH}$ | | 15 | | ns | | 9, 10 | |
| Output Enable Time to Logic Low | $t_{PZL}$ | | 30 | | ns | | 9, 10 | |
| Output Disable Time from Logic High | $t_{PHZ}$ | | 20 | | ns | | 9, 10 | |
| Output Disable Time from Logic Low | $t_{PLZ}$ | | 15 | | ns | | 9, 10 | |
| Logic High Common Mode Transient Immunity | $\lvert CM_H \rvert$ 2400 | 1000 | 10,000 | | V/µs | $V_{CM} = 50\ V$; $T_A = 25°C$, $I_F = 0$ | 11 | 6 |
| | $\lvert CM_H \rvert$ 2411 | 1000 | | | V/µs | $V_{CM} = 300\ V$; $T_A = 25°C$, $I_F = 0$ | 11 | 6 |
| Logic Low Common Mode Transient Immunity | $\lvert CM_L \rvert$ 2400 | 1000 | 10,000 | | V/µs | $V_{CM} = 50\ V$; $T_A = 25°C$, $I_F = 4\ mA$ | 11 | 6 |
| | $\lvert CM_L \rvert$ 2411 | 1000 | | | V/µs | $V_{CM} = 300\ V$; $T_A = 25°C$, $I_F = 4\ mA$ | 11 | 6 |
| Power Supply Noise Immunity | PSNI | | 0.5 | | $V_{p-p}$ | $V_{CC} = 5.0\ V$, $48\ Hz \le F_{AC} \le 50\ MHz$ | | 7 |

# Insulation Related Specifications

| Parameter | Symbol | Value | Units | Conditions |
|---|---|---|---|---|
| Min. External Air Gap (Clearance) | L(IO1) | ≥7 | mm | Measured from input terminals to output terminals |
| Min.External Tracking Path (Creepage) | L(IO2) | ≥7 | mm | Measured from input terminals to output terminals |
| Min. Internal Plastic Gap (Clearance) | | 0.08 | mm | Through insulation distance conductor to conductor |
| Tracking Resistance | CTI | 175 | Volts | DIN IEC 112/VDE 0303 Part 1 |
| Isolation Group (per DIN VDE 0109) | | IIIa | | Material Group DIN VDE 0109 |

**Notes:**

1. Duration of output short circuit time not to exceed 10 ms.
2. Device considered a two terminal device: pins 1–4 shorted together, and pins 5–8 shorted together.
3. $t_{PHL}$ propagation delay is measured from the 50% level on the rising edge of the input current pulse to the 1.5 V level on the falling edge of the output pulse. The $t_{PLH}$ propagation delay is measured from the 50% level on the falling edge of the input current pulse to the 1.5 V level on the rising edge of the output pulse.
4. This specification simulates the worst case operating conditions of the HCPL-2400/11 over the recommended operating temperature and $V_{CC}$ range with the suggested applications circuit of Figure 13.
5. Propagation delay skew is discussed later in this data sheet.
6. $CM_H$ is the maximum slew rate of common mode voltage that can be sustained with the output voltage in the logic high state ($V_{O(MIN)} > 2.0\ V$). $CM_L$ is the maximum slew rate of common mode voltage that can be sustained with the output voltage in the logic low state ($V_{O(MAX)} < 0.8\ V$).
7. Power Supply Noise Immunity is the peak to peak amplitude of the ac ripple voltage on the $V_{CC}$ line that the device will withstand and still remain in the desired logic state. For desired logic high state, $V_{OH(MIN)} > 2.0\ V$, and for desired logic low state, $V_{OL(MAX)} < 0.8$ volts.
8. Peak Forward Input Current pulse width < 50 µs at 1 KHz maximum repetition rate.
9. Use of a 0.1 µF bypass capacitor connected between pins 5 and 8 is recommended.

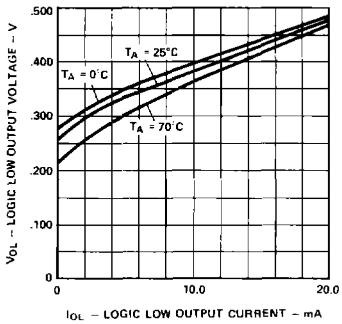



**Figure 1. Typical Logic Low Output Voltage vs. Logic Low Output Current**

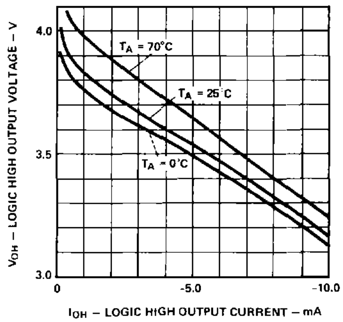



**Figure 2. Typical Logic High Output Voltage vs. Logic High Output Current**

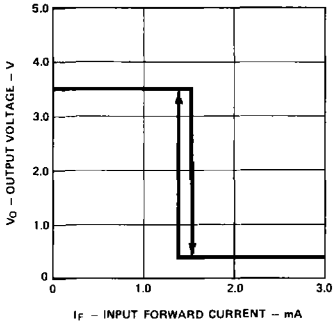



**Figure 3. Typical Output Voltage vs. Input Forward Current**

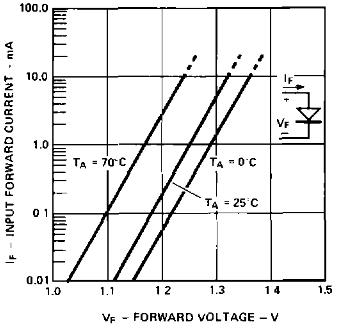



**Figure 4. Typical Diode Input Forward Current Characteristic**

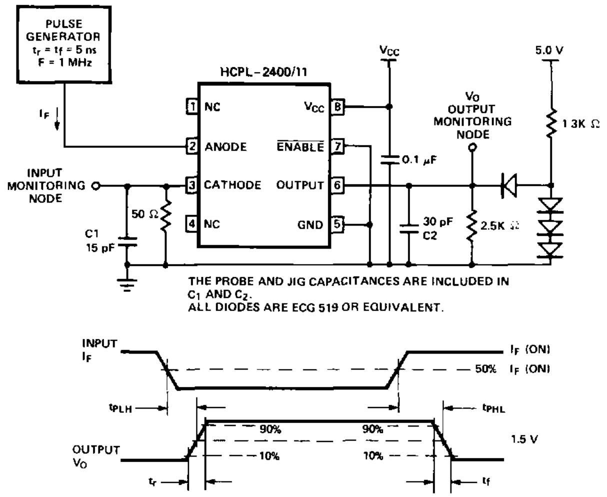



**Figure 5. Test Circuit for $t_{PLH}$, $t_{PHL}$, $t_r$, and $t_f$**

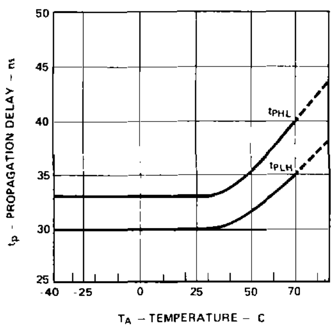



**Figure 6. Typical Propagation Delay vs. Ambient Temperature**

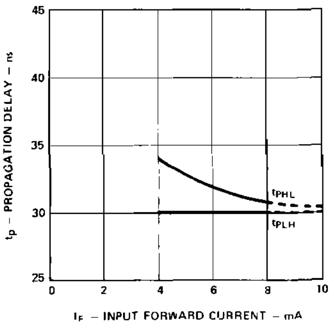



**Figure 7. Typical Propagation Delay vs. Input Forward Current**

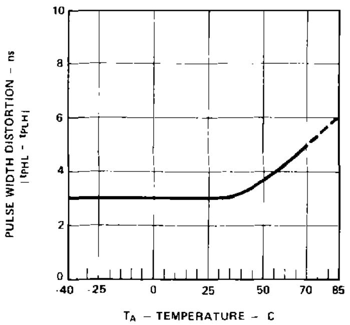
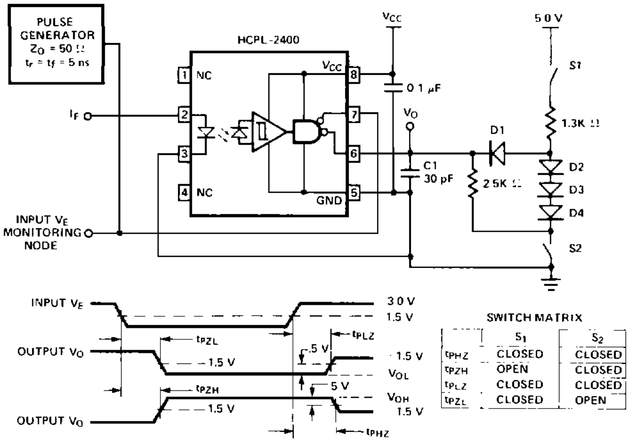



**Figure 8. Typical Pulse Width Distortion vs. Ambient Temperature**




ALL DIODES ARE 1N916 OR EQUIVALENT
C1 = 30 pF INCLUDING PROBE AND JIG CAPACITANCE

**Figure 9. Test Circuit for $t_{PHZ}$, $t_{PZH}$, $t_{PLZ}$ and $t_{PZL}$.**

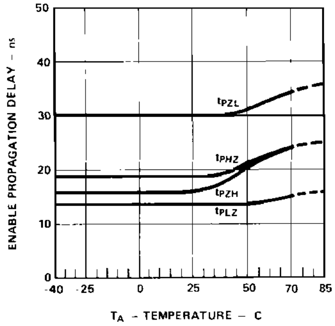
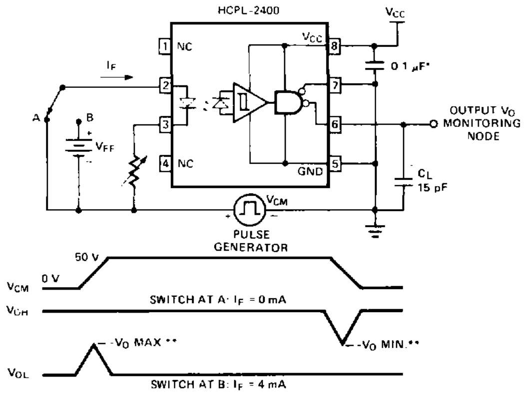



**Figure 10. Typical Enable Propagation Delay vs. Ambient Temperature**




*MUST BE LOCATED 1 cm FROM DEVICE UNDER TEST.
**SEE NOTE 6
† $C_L$ IS APPROXIMATELY 15 pF, WHICH INCLUDES PROBE AND STRAY WIRING CAPACITANCE.

**Figure 11. Test Diagram for Common Mode Transient Immunity and Typical Waveforms**

# Applications

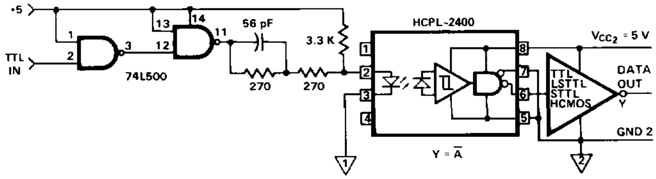



**Figure 13. Recommended 20 MBd HCPL-2400/11 Interface Circuit**

OPTOCOUPLERS

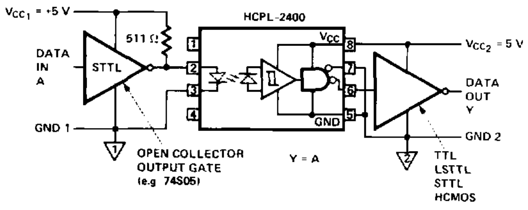



**Figure 14. Alternative HCPL-2400/11 Interface Circuit**

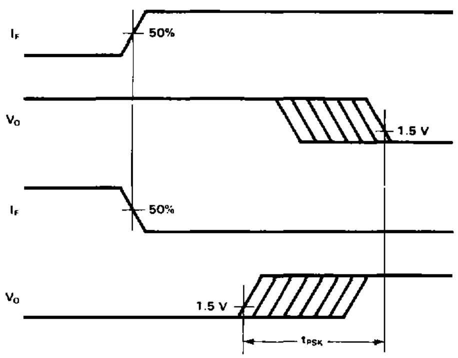



**Figure 15. Illustration of Propagation Delay Skew — $t_{PSK}$.**

# Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew

Propagation delay is a figure of merit which describes how quickly a logic signal propagates through a system. The propagation delay from low to high ($t_{PLH}$) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high. Similarly, the propagation delay from high to low ($t_{PHL}$) is the amount of time required for the input signal to propagate to the output, causing the output to change from high to low (see Figure 5).

Pulse-width distortion (PWD) results when $t_{PLH}$ and $t_{PHL}$ differ in value. PWD is defined as the difference between $t_{PLH}$ and $t_{PHL}$ and often determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD on the order of 20-30% of the minimum pulse width is tolerable; the exact figure depends on the particular application (RS232, RS422, T-1, etc.).

Propagation delay skew, $t_{PSK}$, is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern. If the parallel data is being sent through a group of optocouplers, differences in propagation delays will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delays is large enough, it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either $t_{PLH}$ or $t_{PHL}$, for any given group of optocouplers which are operating under the same conditions (i.e., the same drive current, supply voltage, output load, and operating temperature). As illustrated in Figure 15, if the inputs of a group of optocouplers are switched either ON or OFF at the same time, $t_{PSK}$ is the difference between the shortest propagation delay, either $t_{PLH}$ or $t_{PHL}$, and the longest propagation delay, either $t_{PLH}$ or $t_{PHL}$.

As mentioned earlier, $t_{PSK}$ can determine the maximum parallel data transmission rate. Figure 16 is the timing diagram of a typical parallel data application with both the clock and the data lines being sent through optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. To obtain the maximum data transmission rate, both edges of the clock signal are being used to clock the data; if only one edge were used, the clock signal would need to be twice as fast.

Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler. Figure 16 shows that there will be uncertainty in both the data and the clock lines. It is important that these two areas of uncertainty not overlap, otherwise the clock signal might arrive before all of the data outputs have settled, or some of the data outputs may start to change before the clock signal has arrived. From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice $t_{PSK}$. A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

The HCPL-2400/11 optocouplers offer the advantages of guaranteed specifications for propagation delays, pulse-width distortion, and propagation delay skew over the recommended temperature, input current, and power supply ranges.

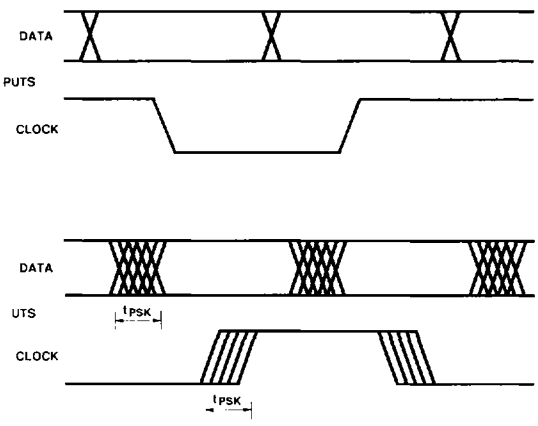



**Figure 16. Parallel Data Transmission Example.**

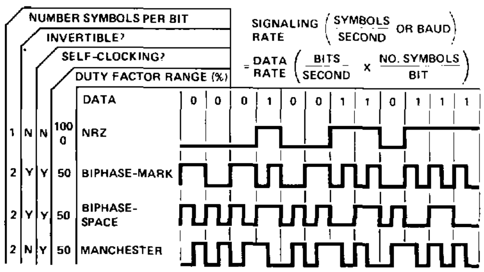



**Figure 17. Modulation Code Selections**

# Application Circuit

A recommended LED drive circuit is shown in Figure 13. This circuit utilizes several techniques to minimize the total pulse-width distortion at the output of the optocoupler. By using two inverting TTL gates connected in series, the inherent pulse-width distortion of each gate cancels the distortion of the other gate. For best results, the two series-connected gates should be from the same package.

The circuit in Figure 13 also uses techniques known as prebias and peaking to enhance the performance of the optocoupler LED. Prebias is a small forward voltage applied to the LED when the LED is off. This small prebias voltage partially charges the junction capacitance of the LED, allowing the LED to turn on more quickly. The speed of the LED is further increased by applying momentary current peaks to the LED during the turn-on and turn-off transitions of the drive current. These peak currents help to charge and discharge the capacitances of the LED more quickly, shortening the time required for the LED to turn on and off.

*Switching performance of the* HCPL-2400/11 *optocouplers* is not sensitive to the TTL logic family used in the recommended drive circuit. The typical and worst-case switching parameters given in the data sheet can be met using common 74LS TTL inverting gates or buffers. Use of faster TTL families will slightly reduce the overall propagation delays from the input of the drive circuit to the output of the optocoupler, but will not necessarily result in lower pulse-width distortion or propagation delay skew. This reduction in overall propagation delays is due to shorter delays in the drive circuit, not to changes in the propagation delays of the optocoupler; optocoupler propagation delays are not affected by the speed of the logic used in the drive circuit.

OPTOCOUPLERS

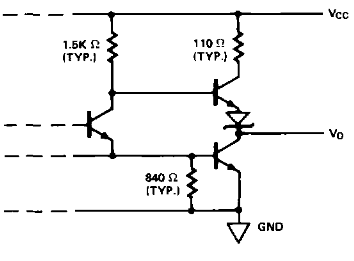



**Figure 18. Typical HCPL-2400/11 Output Schematic**