HM63021 Series

2048-word × 8-bit Line Memory

The HM63021 is a 2048-word × 8-bit static serial access memory (SAM) with separate data inputs and outputs. Since it has an internal address counter, no external address signal is required and internal addresses are scanned serially. Using five different address scan modes, it is applicable to FIFO memories, double-speed conversions, 1H delay lines, and 1H/2H delay lines for digital TV signals. Its minimum cycle times are 28 ns and 34 ns, corresponding to 8 fsc of PAL TV and NTSC TV signals. All inputs and outputs are TTL-compatible.

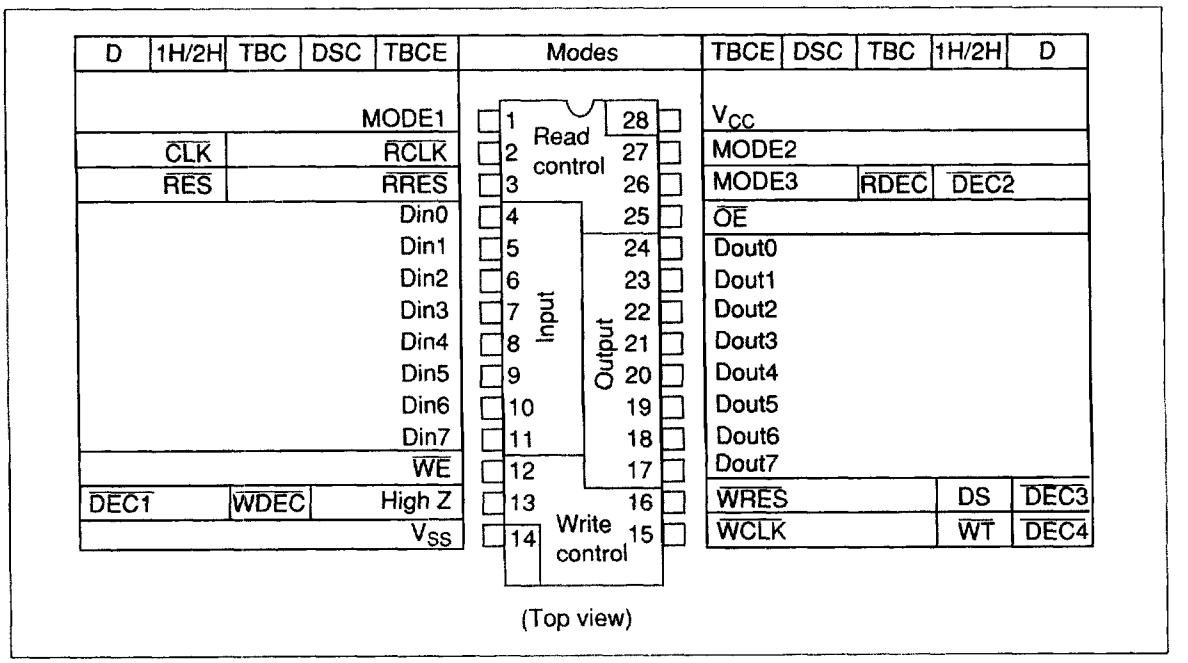
Features

- Five modes for various applications
- Corresponds to digital TV system with 4 fsc sampling (PAL, NTSC)
- Decoder signal output pin (fewer external circuits)
- Asynchronous read/write operation
  - — Separate address counters for read/write
  - — No address input required
- High speed (cycle time 28/34/45 ns (min))
- Completely static memory (no refresh required)
- 8-bit SAM with separate I/O
- Low power (250 mW typ active)
- Single 5 V supply
- TTL compatible

Ordering Information

Type No.	Cycle Time	Package
HM63021P-28	28 ns	300-mil, 28-pin plastic DIP (DP-28N)
HM63021P-34	34 ns	
HM63021P-45	45 ns	
HM63021FP-28	28 ns	28-pin plastic SOP (FP-28DA)
HM63021FP-34	34 ns	
HM63021FP-45	45 ns	

Pin Arrangement



(Top view)

Pin Description

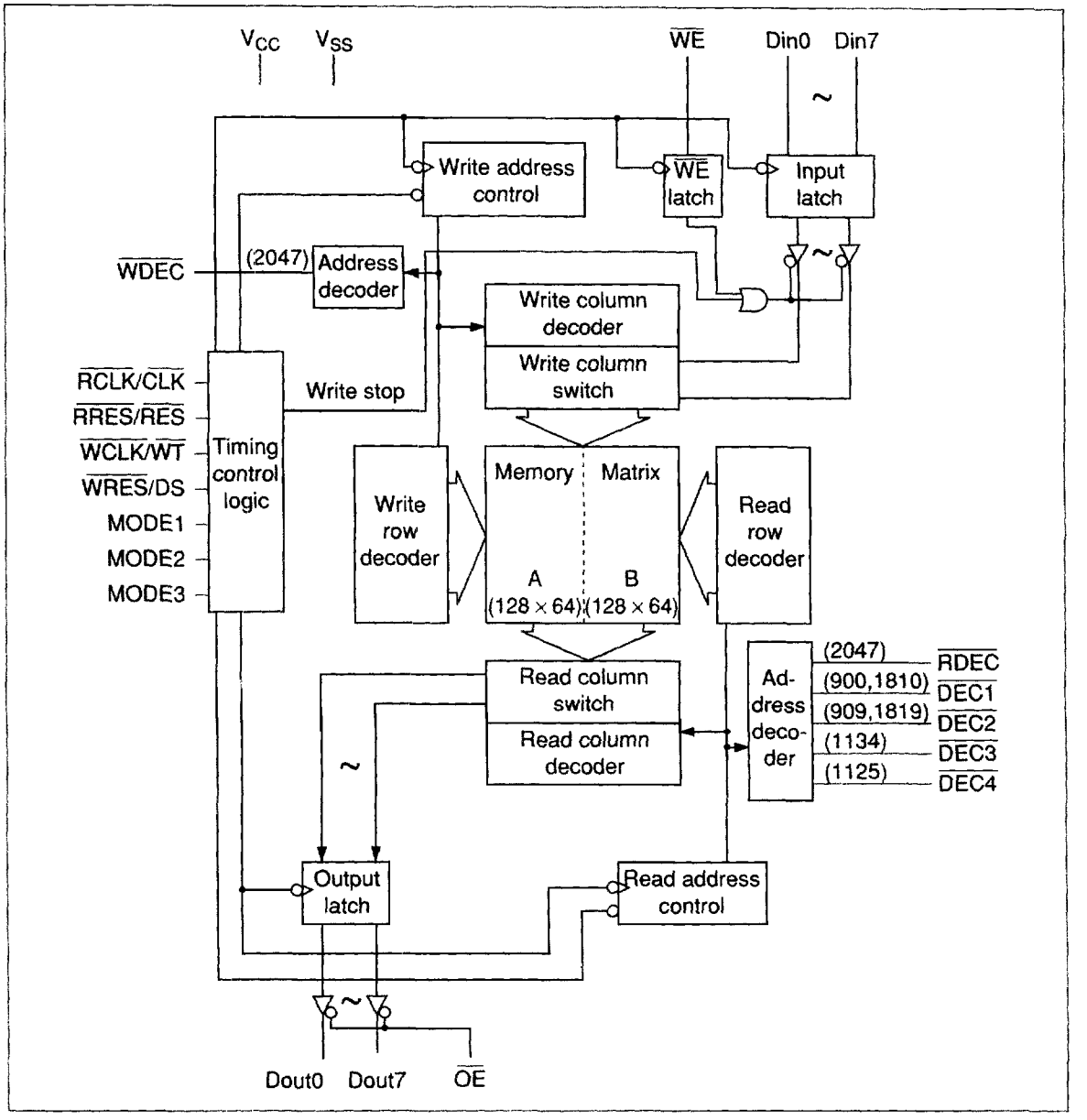
Pin No.	Pin Name	Functions
1	MODE1	Mode input 1 (all modes)
2	$\overline{RCLK}$/CLK	Read clock input (TBCE, DSC, TBC) Clock input (1H/2H, D)
3	$\overline{RRES}$/$\overline{RES}$	Read reset input (TBCE, DSC, TBC) Reset input (1H/2H, D)
4 to 11	Din 0 to Din 7	Data inputs (all modes)
12	$\overline{WE}$	Write enable input (all modes)
13	High-Z/$\overline{WDEC}$/$\overline{DEC1}$	High impedance (TBCE, DSC) Write decode pulse output (TBC) Decode pulse output 1 (1H/2H, D)
14	V_{SS}	Ground (all modes)
15	$\overline{WCLK}$/$\overline{WT}$/$\overline{DEC4}$	Write clock input (TBCE, DSC, TBC) Write timing input (1H/2H) Decode pulse output 4 (D)
16	$\overline{WRES}$/DS/$\overline{DEC3}$	Write reset input (TBCE, DSC, TBC) Delay select input (1H/2H) Decode pulse output 3 (D)
17 to 24	Dout 0 to Dout 7	Data outputs (all modes)
25	$\overline{OE}$	Output enable input (all modes)
26	MODE3/$\overline{RDEC}$/$\overline{DEC2}$	Mode input 3 (TBCE) Read decode pulse output (TBC) Decode pulse output 2 (1H/2H, D)
27	MODE2	Mode input 2 (all modes)
28	V_{CC}	Power supply (+5 V) (all modes)

Mode Table

Mode Signals				
MODE1	**MODE2**	**MODE3**	**Mode**	**Application Example**
H	H	H	Time base compression/expansion (TBCE)	Picture in picture
H	H	L	Double speed conversion (DSC)	Non interlace
H	L	—*1	Time base correction (TBC)	Time base corrector
L	H	—*1	1H/2H delay (1H/2H)	Vertical filter
L	L	—*1	Delay line (D)	Delay line

Note: 1. Decoder output signal ($\overline{RDEC}$, $\overline{DEC2}$)

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_T	−0.5*1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C
Storage temperature under bias	Tbias	−10 to +85	°C

Note: 1. −3.5 V for pulse width ≤ 10 ns.

Recommended DC Operating Conditions (Ta = 0 to +70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.4	—	6.0	V
	V_{IL}	−0.5 *	—	0.8	V

Note: −3.0 V for pulse width ≤ 10 ns.

DC and Operating Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ *1	Max	Unit	Test Condition
Input leakage current	$\|I_{LI}\|$	—	—	10	µA	V_{CC} = 5.5 V Vin = V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	10	µA	$\overline{OE}$ = V_{IH} Vout = V_{SS} to V_{CC}
Operating power supply current	I_{CC}	—	50	90	mA	Min. cycle, Iout*2 = 0 mA
Output voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA *3 Dout 0 to Dout 7, $\overline{DEC}$ output pin
	V_{OH}	2.4	—	—	V	I_{OH} = −4 mA, Dout 0 to Dout 7 pin
		2.4	—	—	V	I_{OH} = −1 mA, $\overline{DEC}$ output pin

Notes: 1. Typical values are at V_{CC} = 5 V, Ta = 25°C and for reference only.
2. Dout and $\overline{DEC}$
3. I_{OL} = 6 mA for 45 ns version.

Capacitance (Ta = 25 °C, f = 1.0 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Output capacitance *2	Cout	—	—	9	pF	Vout = 0 V

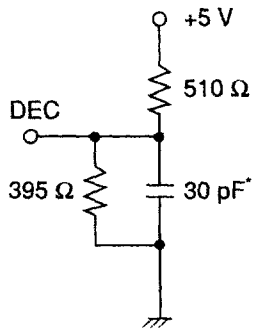
Notes: 1. These parameters are sampled and not 100% tested.
2. 13, 15–24, 26 pin

AC Characteristics (V_{CC} = 5 V ± 10%, T_a = 0 to +70°C, unless otherwise noted)

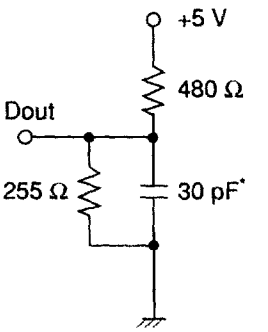
AC Test Conditions:

- Input and output timing reference levels: 1.5 V
- Input pulse levels: V_{SS} to 3 V
- Input rise and fall times: 5 ns

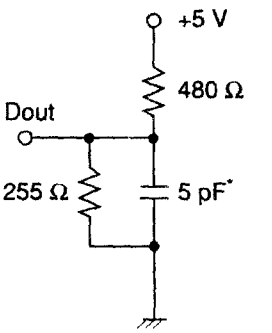
HM63021-28/34 Output Load



DEC output load



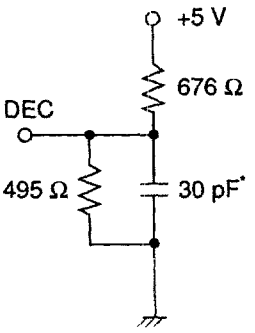
Dout output load (A)



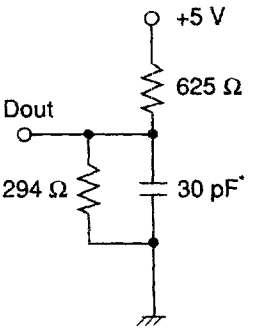
Dout output load (B)
(t_{OLZ}, t_{OHZ})

Note: Including scope and jig.

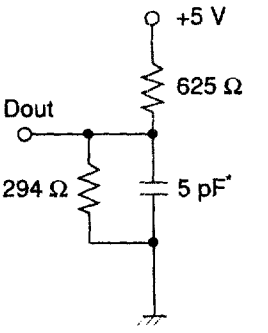
HM63021-45 Output Load



DEC output load



Dout output load (A)



Dout output load (B)
(t_{OLZ}, t_{OHZ})

Note: Including scope and jig.

Read Cycle

Parameter		Symbol	HM63021-28 Min	HM63021-28 Max	HM63021-34 Min	HM63021-34 Max	HM63021-45 Min	HM63021-45 Max	Unit
Read cycle time		t_{RC}	28	—	34	—	45	—	ns
Read clock width		t_{RWL}	10	—	10	—	15	—	ns
		t_{RWH}	10	—	10	—	15	—	ns
Access time	(fall)	t_{AC}	—	20	—	25	—	30	ns
	(rise)	t_{DA1}	—	20	—	25	—	30	ns
Decode output access time		t_{DA2}	—	40	—	50	—	60	ns
Output hold time		t_{OH}	5	—	5	—	5	—	ns
Decode output hold time	(fall)	t_{DOH1}	5	—	5	—	5	—	ns
	(rise)	t_{DOH2}	5	—	5	—	5	—	ns
Output enable access time		t_{OE}	—	20	—	25	—	30	ns
Output disable to output in high Z		t_{OHZ}	0	15	0	20	0	25	ns
Output enable to output in low Z		t_{OLZ}	5	—	5	—	5	—	ns
Input rise and fall time		t_T	3	50	3	50	3	50	ns

Write Cycle

Parameter	Symbol	HM63021-28 Min	HM63021-28 Max	HM63021-34 Min	HM63021-34 Max	HM63021-45 Min	HM63021-45 Max	Unit
Write cycle time	t_{WC}	28	—	34	—	45	—	ns
	t_{WC} (1H/2H Mode)	56	—	68	—	90	—	ns
Write clock width	t_{WWL}	10	—	10	—	15	—	ns
	t_{WWH}	10	—	10	—	15	—	ns
Input data setup time	t_{DS}	5	—	5	—	7	—	ns
Input data hold time	t_{DH}	5	—	5	—	7	—	ns
$\overline{WE}$ setup time	t_{WESL}	5	—	5	—	7	—	ns
	t_{WESH}	5	—	5	—	7	—	ns
$\overline{WE}$ hold time	t_{WEHL}	5	—	5	—	7	—	ns
	t_{WEHH}	5	—	5	—	7	—	ns
$\overline{WT}$ setup time	t_{WTSL}	5	—	5	—	7	—	ns
	t_{WTSH}	5	—	5	—	7	—	ns
$\overline{WT}$ hold time	t_{WTHL}	5	—	5	—	7	—	ns
	t_{WTHH}	5	—	5	—	7	—	ns
Input rise and fall time	t_T	3	50	3	50	3	50	ns

Mode Description

Time Base Compression/Expansion Mode: Turns the HM63021 into a 2048-word × 8-bit FIFO memory with asynchronous input/output. The HM63021 provides 2 clocks ($\overline{RCLK}$, $\overline{WCLK}$) and 2 resets for read and write ($\overline{RRES}$, $\overline{WRES}$). The internal address counters increment by 1 address clock and are reset to address 0. A write-inhibit function of the HM63021 stops writing automatically after the data has been written into all addresses 0 to 2047. The write-inhibit function is released by reset using $\overline{WRES}$, and the HM63021 restarts writing into address 0.

Double-Speed Conversion Mode: Turns the HM63021 into a 1024-word × 8-bit × 2 memory with asynchronous input/output. It is used for generating non-interlaced TV signals. When the original signal and the interpolated signal (1 field delay) of interlaced signals are input to the HM63021, multiplexed per dot, it outputs non-interlaced signals for each line. 8 fsc should be input to $\overline{RCLK}$ and $\overline{WCLK}$. A standard H synchronizing signal and a non-interlace H synchronizing signal are input to $\overline{WRES}$ and $\overline{RRES}$ respectively. A write-inhibit function is provided in this mode, making it applicable to PAL TV, where extra data (1135–1024 = 111 bits) is ignored.

TBC Mode: Turns the HM63021 into 2048-word × 8-bit FIFO memory with asynchronous input/output. The HM63021 provides 2 clocks ($\overline{RCLK}$, $\overline{WCLK}$) and 2 resets ($\overline{RRES}$, $\overline{WRES}$), one each for read and write. The internal address counters increment by 1 address at each clock and are reset to address 0. The internal address counters return to address 0 after they reach address 2047. The HM63021 outputs a write decode pulse from $\overline{WDEC}$, synchronizing it with address 2047 in the write address counter, and read a decode pulse from $\overline{RDEC}$, synchronizing with address 2047 in the read address counter. Using these pulses, the memory area can be extended easily (multiple-HM63021s can be used with ease).

1H/2H Delay Mode: Turns the HM63021 into a 1024-word × 8-bit × 2 delay line with synchronous input/output. Delay time is defined by the reset period of $\overline{RES}$. Since the HM63021 outputs a 901 decode pulse ($\overline{DEC1}$) and a 910 decode pulse ($\overline{DEC2}$), connecting $\overline{DEC2}$ to $\overline{RES}$, for example, outputs 1H- and 2H- delayed signals alternately at an 8-fsc cycle when the original signal is input at a 4-fsc cycle. A write-inhibit function is provided in this mode, making it applicable to PAL TV, where extra data (1135–1024 = 111 bits) is ignored.

Delay Line Mode: Turns the HM63021 into a 2048-word × 8-bit delay line with synchronous input/output. Delay time (3 to 2048 bits) is defined by the reset period of $\overline{RES}$. The delay is 2048 bits when $\overline{RES}$ is fixed high. Signals delayed by 910 bits to 1135 bits for example, can be easily obtained without external circuits by just connecting selected decoded pulses on $\overline{DEC1}$–$\overline{DEC4}$ to $\overline{RES}$.

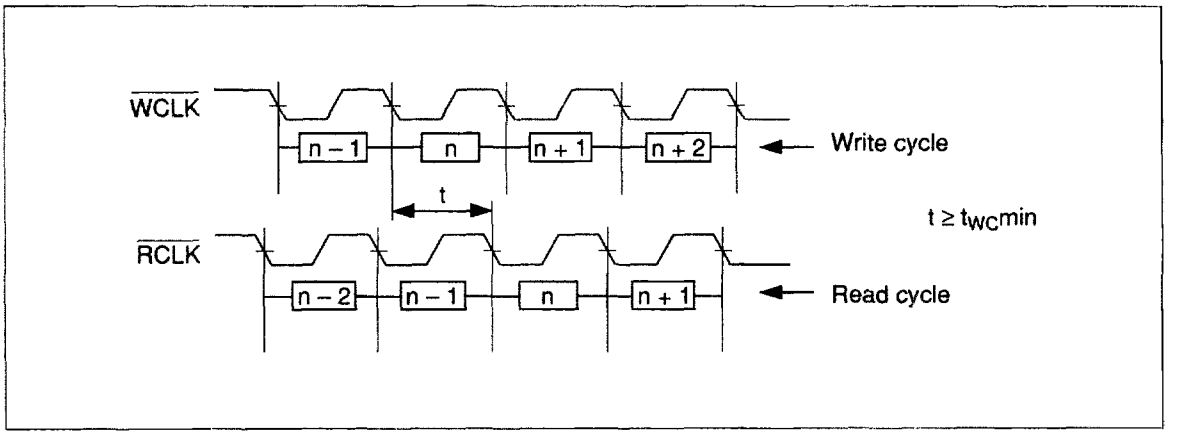
Reset Cycle

		HM63021-28		HM63021-34		HM63021-45		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Reset setup time	t_{RES}	8	—	9	—	10	—	ns
Reset hold time	t_{REH}	5	—	5	—	7	—	ns
Clock setup time before reset	t_{REPS}	8	—	9	—	10	—	ns
Clock hold time before reset	t_{REPH}	5	—	5	—	7	—	ns
Input rise and fall time	t_T	3	50	3	50	3	50	ns

Notes on Using HM63021:

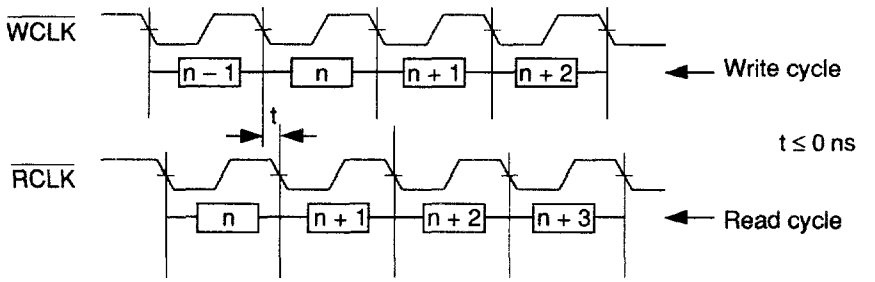
- Hitachi recommends that pin 13 (high impedance) should be fixed by pulling up or down with a resistor (of several kΩ) in TBC or DSC mode.
- Hitachi recommends that the mode signal input pins and DS pin should be fixed by pulling them up or down with a resistor (of several kΩ).
- Data integrity cannot be guaranteed when mode or DS is changed during operation.
- When a read address coincides with a write address in TBCE, TBC, or DSC mode, the data is written correctly but it is not always read correctly.
- At power on, the output of the address counter is not defined. Therefore, operations before the system is reset cannot be guaranteed, and the decode signal output is not defined until after the first reset cycle.
- The decode signal is latched by a decode output latch circuit at the previous address of the internal counter address and is output-synchronized with the next address. For example, $\overline{\text{WDEC}}$ in TBC mode is latched at write address 2046 and is output at write address 2047. If a write reset is performed on address 2047 at this time, the write address becomes 0 and $\overline{\text{WDEC}}$ is output. The same operation is performed in other modes.
- When TBC or DSC or TBCE mode is used, at least one $\overline{\text{RCLK}}$ dummy cycle is required before starting write operation (before executing write pre-reset cycle) after power up.
- Transition time of input level t_T is defined as the rising time from V_{IL} to V_{IH} and the falling time from V_{IH} to V_{IL}.

Read After Write (3 Bit Delay)

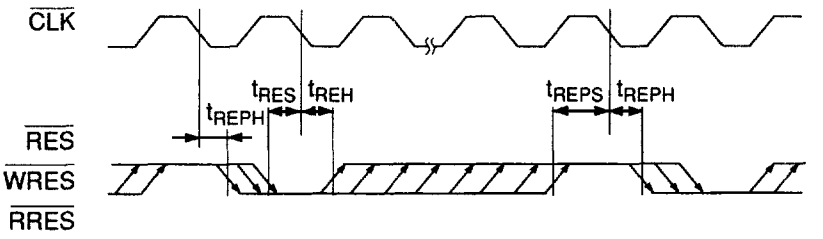


- In the reset cycle, the input levels of $\overline{WRES}$, $\overline{RRES}$, and $\overline{RES}$ are raised to satisfy t_{REH}, and are fixed high until t_{REPH} in the next pre-reset cycle is satisfied. The rise timings of the reset signals ($\overline{RES}$, $\overline{WRES}$, $\overline{RRES}$) are optional provided that the t_{REPS} specification is satisfied. The timings at which $\overline{RES}$, $\overline{WRES}$, and $\overline{RRES}$ fall after pre-reset are also optional, provided that the t_{REPH} and t_{RES} specifications are satisfied.
- Hitachi recommends that t_m (time between mode set and the first cycle (pre-reset)) should be kept for 2 cycle times (56 ns/68 ns/90 ns) or more while the power supply is on.

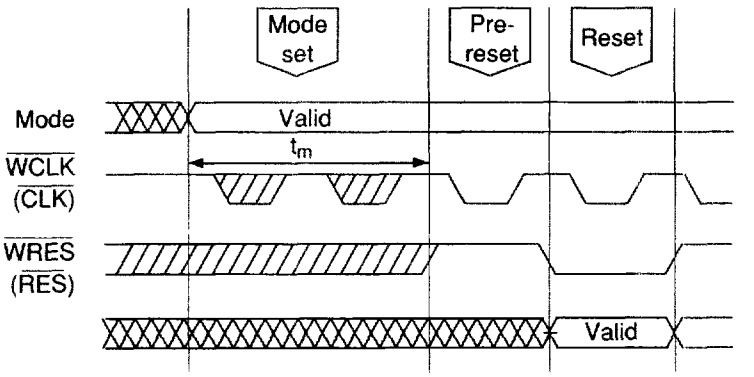
Write After Read (2048 Bit Delay)



Reset Cycle

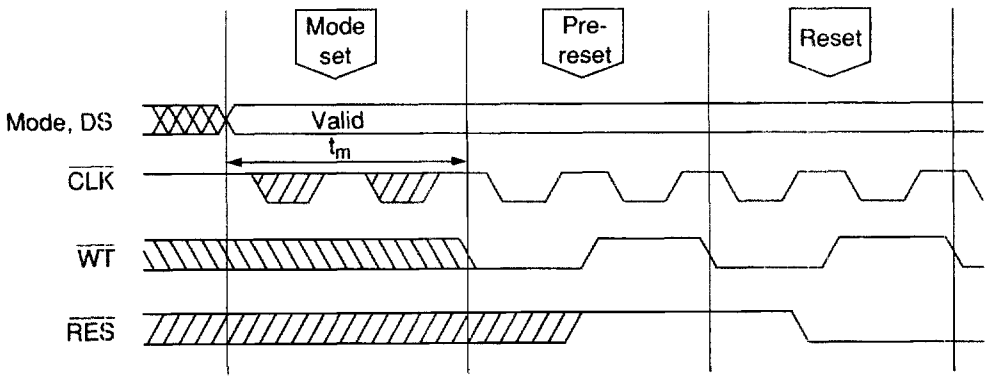


TBCE, TBC, DSC, and Delay Line Mode



Note: When mode pins are fixed with V_{CC} and V_{SS} is in mode set while the power supply is on, t_m spec is not needed.

1H/2H Delay Mode



Note: When mode pins are fixed with V_{CC} and V_{SS} is in mode set while the power supply is on, t_m spec is not needed.

Decode Signal

When internal address counter reaches the specified address as shown below, decode outputs become low.

Mode	Pin No.	Pin Name	Internal Address	Output Signal Timing	Operation
TBC	13	$\overline{WDEC}$	Write 2047	After write 2047	Completion of writing on all bits is detected.
	26	$\overline{RDEC}$	Read 2047	Output of 2046	Completion of reading from all bits is detected.
1H/2H	13	$\overline{DEC1}$	Read 900 (2H)	Output of 900 (1H)	By inputting this signal to pin number 3, a 901/1802-bit delay output is obtained.
	26	$\overline{DEC2}$	Read 909 (2H)	Output of 909 (1R)	By inputting this signal to pin number 3, a 910/1820-bit delay output is obtained.
Delay line	13	$\overline{DEC1}$	Read 900	Output of 899	By inputting this signal to pin number 3, a 901-bit delay output is obtained.
			Read 1810	Output of 1809	By inputting this signal to pin number 3 after the frequency of $\overline{DEC1}$ is divided into two, 1811-bit delay outputs are obtained.
	26	$\overline{DEC2}$	Read 909	Output of 908	By inputting this signal to pin number 3, a 910-bit delay output is obtained.
			Read 1819	Output of 1818	By inputting this signal to pin number 3 after the frequency of $\overline{DEC2}$ is divided into two, 1820-bit delay outputs are obtained.
	16	$\overline{DEC3}$	Read 1134	Output of 1133	By inputting this signal to pin number 3, 1135-bit delay output is obtained.
	15	$\overline{DEC4}$	Read 1125	Output of 1124	By inputting this signal to pin number 3, 1126-bit delay output is obtained.

Note: When the counter is reset by a reset signal ($\overline{RRES}$, $\overline{RES}$, $\overline{WRES}$), the address becomes 0.

Write-Inhibit Function

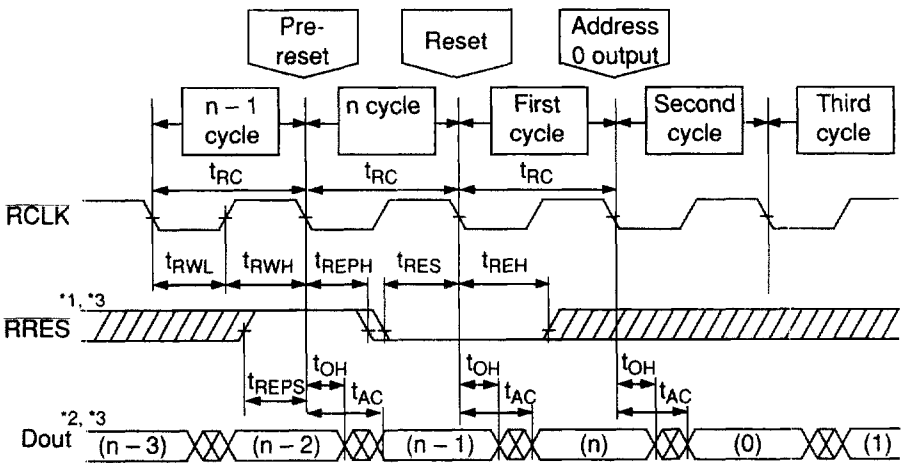
When internal address counter is as follows, writing is inhibited automatically for the next cycle. The write-inhibit function is canceled by reset through $\overline{WRES}$ or $\overline{RES}$.

Mode	Write-Inhibit Function (Internal Counter Address)
TBCE	Write-inhibit after address 2047
DSC	Write-inhibit after address 1023 × 2
TBC	No function
1H/2H	Write-inhibit after address 1023
D	No function

Note: When address counter is reset by $\overline{WRES}$ or $\overline{RES}$, the address becomes 0.

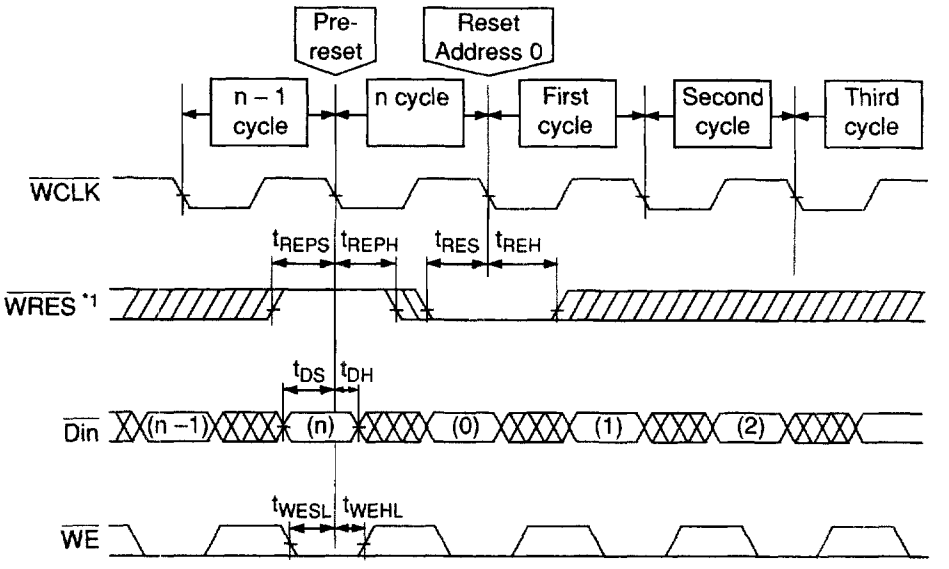
Timing Waveforms

Read Reset Cycle (TBCE, TBC Modes)



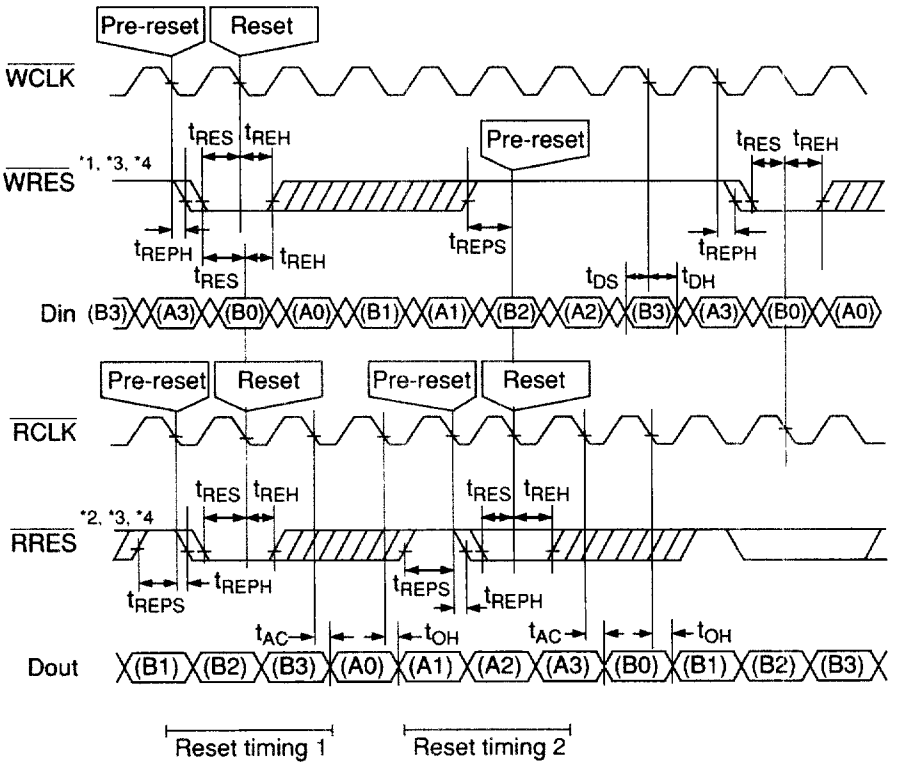
Notes: 1. The read address counter is reset at the first falling edge of $\overline{RCLK}$ after $\overline{RRES}$ falls, meeting the specifications of t_{REPS}, and t_{REPH}, and it is not reset at the next falling edge of $\overline{RCLK}$ even if $\overline{RRES}$ is kept low. When t_{RES}, t_{REH}, t_{REPS}, and t_{REPH} cannot meet the specifications, the reset operation is not guaranteed. In reset operation, both prereset and reset are required.
2. Output is from the read address of the previous cycle.
3. When $\overline{RRES}$ is fixed high, the data at the read address counter is reset after the data of address 2047 is output, and the same operation restarts.

Write Reset Cycle (TBCE, TBC Modes)



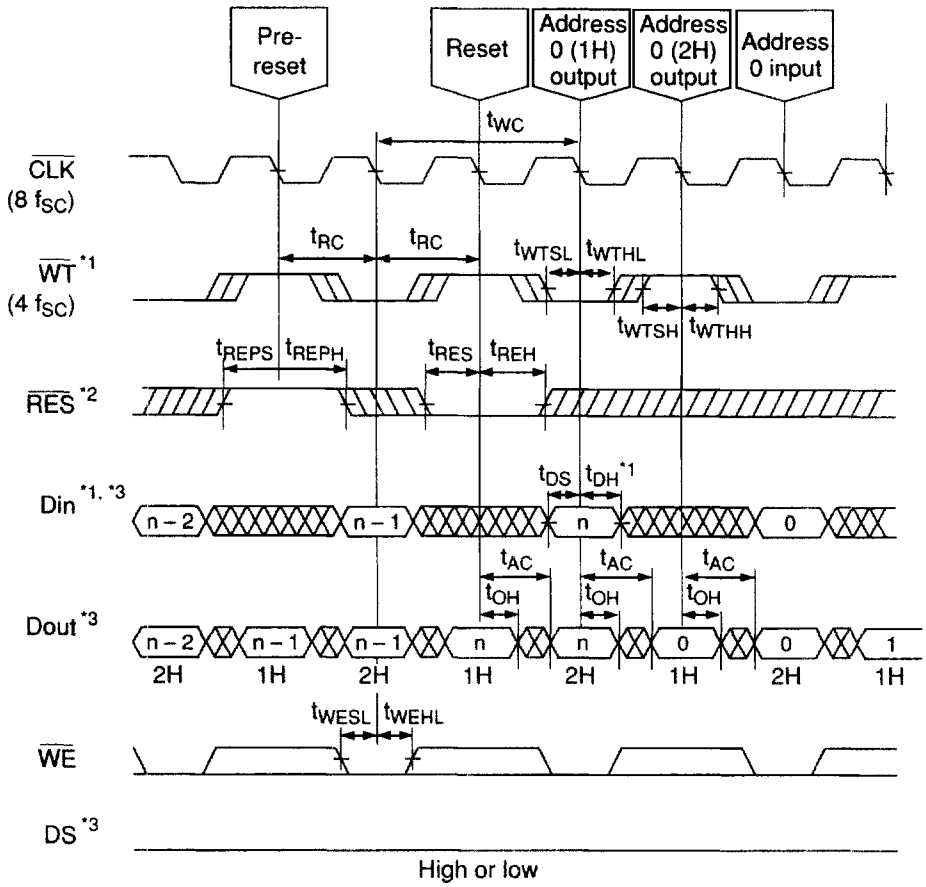
Note: The write address counter is reset at the first falling edge of WCLK after WRES falls, meeting the specifications of t_{REPS} and t_{REPH}, and it is not reset at the next falling edge of WCLK even if WRES is kept low. When t_{RES}, t_{REH}, t_{REPS}, and t_{REPH} cannot meet the specifications, the reset operation is not guaranteed. In reset operation, both prereset and reset are required.

Reset Cycle (DSC Modes)



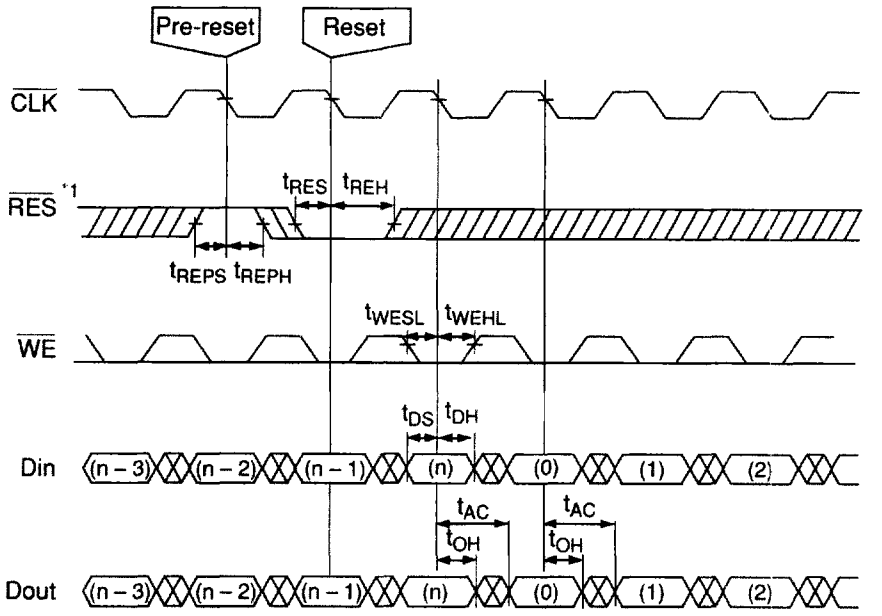
Notes:
1. The write address counter is reset at the first falling edge of $\overline{WCLK}$ after $\overline{WRES}$ falls, meeting the specifications of t_{REPS} and t_{REPH}, and is not reset at the next falling edge of $\overline{WCLK}$ even if $\overline{WRES}$ is kept low. When t_{RES}, t_{REH}, and t_{REPH} cannot meet the specifications, the reset operation is not guaranteed.
2. The read address counter is reset at the first falling edge of $\overline{RCLK}$ after $\overline{RRES}$ falls, meeting the specifications of t_{REPS} and t_{REPH}, and it is not reset at the next falling edge of $\overline{RCLK}$ even if $\overline{RRES}$ is kept low. When t_{RES}, t_{REH}, t_{REPS}, and t_{REPH} cannot meet the specifications, reset operation is not guaranteed.
3. When t_{REPH}, t_{RES}, t_{REH} ($\overline{WRES}$ to $\overline{WCLK}$), t_{RES}, t_{REH}, ($\overline{WRES}$ to $\overline{RCLK}$) or t_{REPS}, t_{REPH}, t_{RES}, t_{REH} ($\overline{RRES}$ to $\overline{RCLK}$) cannot meet the specifications, the output of video signal A is not guaranteed (reset timing 1).
4. When t_{REPS} ($\overline{WRES}$ to $\overline{RCLK}$), or t_{RES}, t_{REH}, t_{REPS}, t_{REPH} ($\overline{RRES}$ to $\overline{RCLK}$) cannot meet the specifications, the interpolation signal B is not guaranteed (reset timing 2).

Reset Cycle (1H/2H Modes)



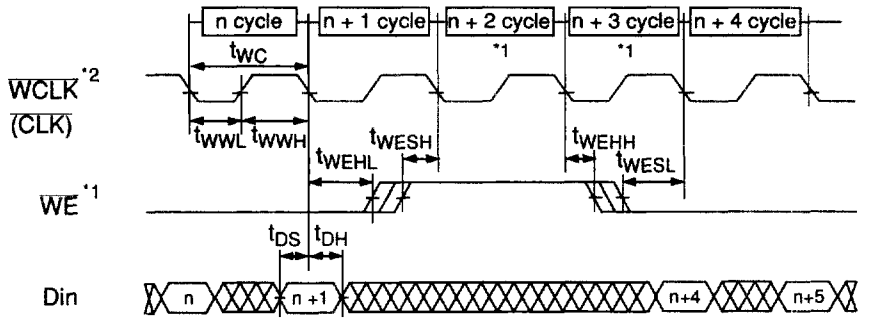
Notes:
1. $\overline{WT}$ is the input during half cycle of $\overline{CLK}$, meeting the specifications of t_{WTSL}, t_{WTHL}, t_{WTSH}, and t_{WTHH}. Data is written when $\overline{WT}$ is low. Reset is possible when $\overline{WT}$ is high.
2. Read address counter is reset at the first falling edge of $\overline{CLK}$ after $\overline{RES}$ falls, meeting the specifications of t_{REPS} and t_{REPH}, and it is not reset at the next falling edge of $\overline{CLK}$ even if $\overline{RES}$ is kept low. When t_{RES}, t_{REH}, t_{REPS}, and t_{REPH} cannot meet the specifications, the reset operation is not guaranteed. In reset operation, both prereset and reset are required.
3. When $\overline{DS}$ is fixed high, 1H output date is delayed by n bits and 2H output data is delayed by 2n bits where 2n is the reset cycle of $\overline{RES}$. When $\overline{DS}$ is fixed low, 1H output data is delayed by n-5 bits and 2H output data is delayed by 2n-5 bits.

Reset Cycle (D Modes)



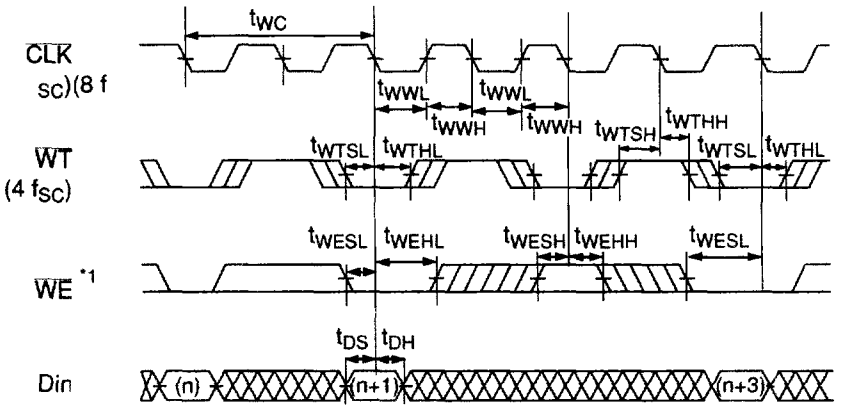
Note: The read address counter is reset at the first falling edge of $\overline{CLK}$ after $\overline{RES}$ falls, meeting the specifications of t_{REPS} and t_{REPH}, and it is not reset at the next falling edge of $\overline{CLK}$ even if $\overline{RES}$ is kept low. When t_{RES}, t_{REH}, t_{REPS}, and t_{REPH} cannot meet the specifications, the reset operation is not guaranteed. In reset operation, both prereset and reset are required.

Write Enable (TBCE, DSC, TBC, D Modes)



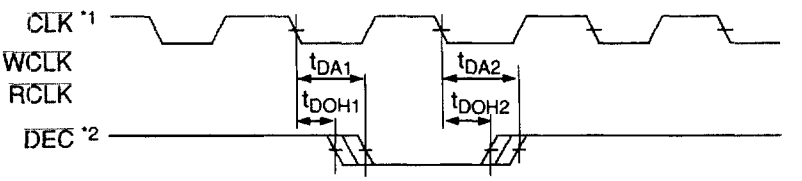
Notes: 1. When t_{WEHL}, t_{WESH}, t_{WEHH}, and t_{WESL} cannot meet this specifications, the write enable operation is not guaranteed.
2. In the delay line mode, $\overline{CLK}$ takes the place of $\overline{WCLK}$.

Write Enable (1H/2H Mode)



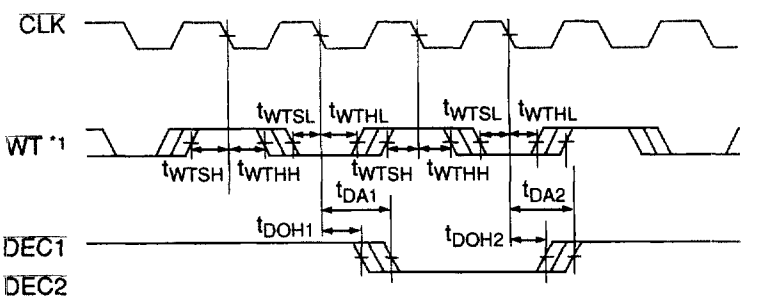
Note: When t_{WTSL}, t_{WTHL}, t_{WEHZ}, and t_{WEHH} cannot meet the specifications, the write enable operation is not guaranteed.

Decode Output (TBC, D Modes)



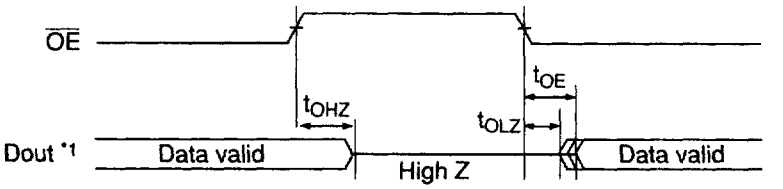
Notes: 1. In TBC mode, $\overline{WCLK}$ or $\overline{RCLK}$ takes the palce of $\overline{CLK}$.
2. $\overline{DEC}$ is $\overline{WDEC}$ or $\overline{RDEC}$ in $\overline{TBC}$, $\overline{DEC1}$, $\overline{DEC2}$, $\overline{DEC2}$, or $\overline{DEC4}$ in D mode.

Decode Output (1H/2H Modes)



Note: When t_{WTSL}, t_{WTHL}, t_{WTSH}, and t_{WTHH} cannot meet the specifications, the decode output operation is not guaranteed.

Output Enable (All Modes)



Note: Transition of t_{OHZ} and t_{WLZ} is measured ±200 mV from steady state voltage with output load B. These parameters are sampled and not 100% tested.