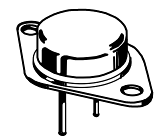
MJ10020
MJ10021

SWITCHMODE™ Series NPN Silicon Power Darlington Transistors with Base-Emitter Speedup Diode

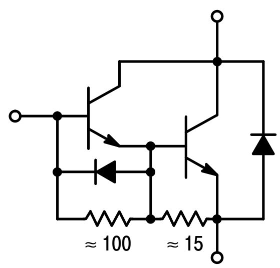
60 AMPERE
NPN SILICON
POWER DARLINGTON
TRANSISTORS
200 AND 250 VOLTS
250 WATTS



CASE 197A–05
TO–204AE (TO–3)

The MJ10020 and MJ10021 Darlington transistors are designed for high–voltage, high–speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated SWITCHMODE applications such as:

- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn–Off Times
  - 150 ns Inductive Fall Time at 25°C (Typ)
  - 750 ns Inductive Storage Time at 25°C (Typ)
- Operating Temperature Range –65 to +200°C
- 100°C Performance Specified for:
  - Reversed Biased SOA with Inductive Loads
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents



MAXIMUM RATINGS

Rating	Symbol	MJ10020	MJ10021	Unit
Collector–Emitter Voltage	V_{CEO}	200	250	Vdc
Collector–Emitter Voltage	V_{CEV}	300	350	Vdc
Emitter Base Voltage	V_{EB}	8.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	60 100		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	20 30		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	250 143 1.43		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	MJ10020 MJ10021	$V_{CEO(sus)}$	200 250	— —	— —	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEV}	— —	— —	0.25 5.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	—	—	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 2.0 V, I_C = 0)		I_{EBO}	—	—	175	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$		See Figure 13		
Clamped Inductive SOA with Base Reverse Biased		RBSOA		See Figure 14		
ON CHARACTERISTICS (2)						
DC Current Gain (I_C = 15 Adc, V_{CE} = 5.0 V)		h_{FE}	75	—	1000	—
Collector–Emitter Saturation Voltage (I_C = 30 Adc, I_B = 1.2 Adc) (I_C = 60 Adc, I_B = 4.0 Adc) (I_C = 30 Adc, I_B = 1.2 Adc, T_C = 100°C)		$V_{CE(sat)}$	— — —	— — —	2.2 4.0 2.4	Vdc
Base–Emitter Saturation Voltage (I_C = 30 Adc, I_B = 1.2 Adc) (I_C = 30 Adc, I_B = 1.2 Adc, T_C = 100°C)		$V_{BE(sat)}$	— —	— —	3.0 3.5	Vdc
Diode Forward Voltage (I_F = 30 Adc)		V_f	—	2.5	5.0	Vdc
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)		C_{ob}	175	—	700	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 175 Vdc, I_C = 30 A, I_{B1} = Adc, $V_{BE(off)}$ = 5.0 V, t_p = 25 µs Duty Cycle ≤ 2.0%).	t_d	—	0.02	0.2	µs
Rise Time		t_r	—	0.30	1.0	µs
Storage Time		t_s	—	1.0	3.5	µs
Fall Time		t_f	—	0.07	0.5	µs
Inductive Load, Clamped (Table 1)						
Storage Time	I_{CM} = 30 A(pk), V_{CEM} = 200 V, I_{B1} = 1.2 A, $V_{BE(off)}$ = 5 V, T_C = 100°C)	t_{sv}	—	1.2	3.5	µs
Crossover Time		t_c	—	0.45	2.0	µs
Storage Time	(I_{CM} = 30 A(pk), V_{CEM} = 200 V, I_{B1} = 1.2 A, $V_{BE(off)}$ = 5 V, T_C = 25°C)	t_{sv}	—	0.75	—	µs
Crossover Time		t_c	—	0.25	—	µs
Fall Time		t_{fi}	—	0.15	—	µs

(1) Pulse Test: PW = 300 µs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

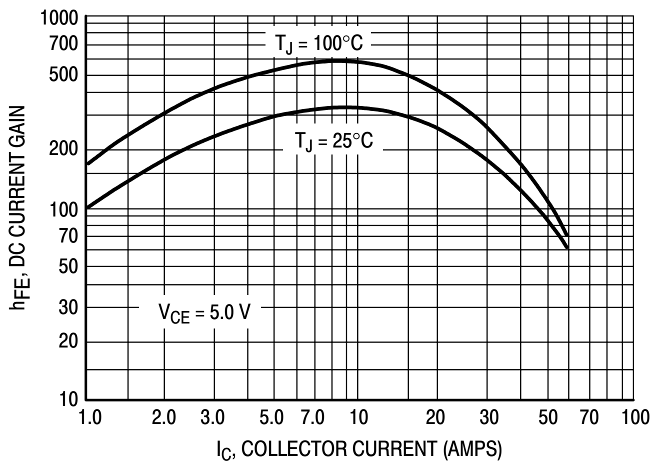


Figure 1. DC Current Gain

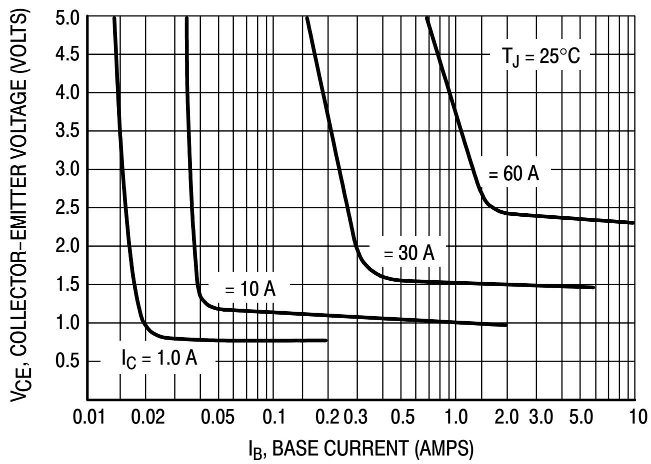


Figure 2. Collector Saturation Region

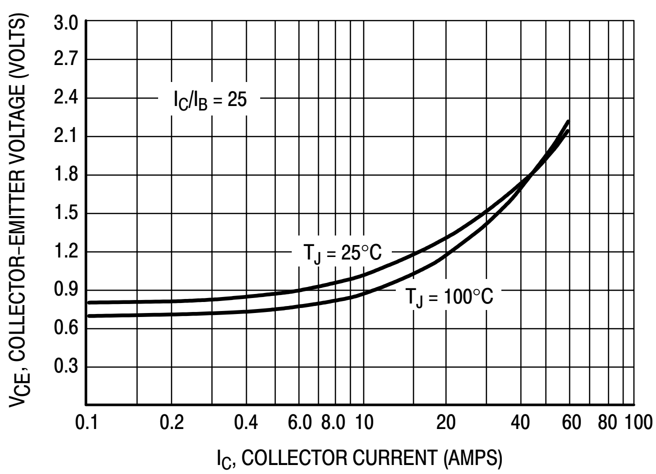


Figure 3. Collector–Emitter Saturation Voltage

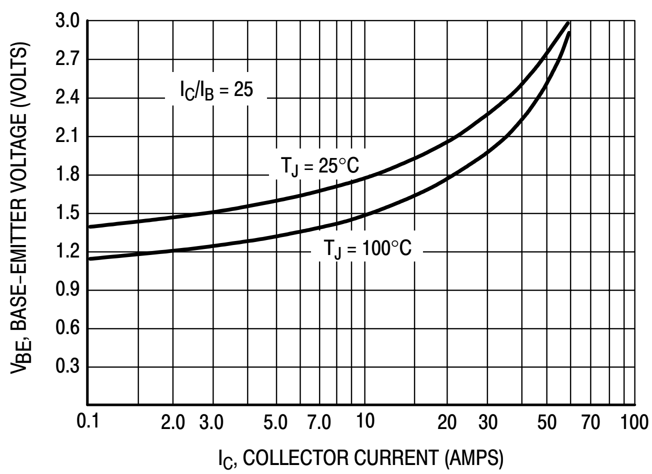


Figure 4. Base–Emitter Voltage

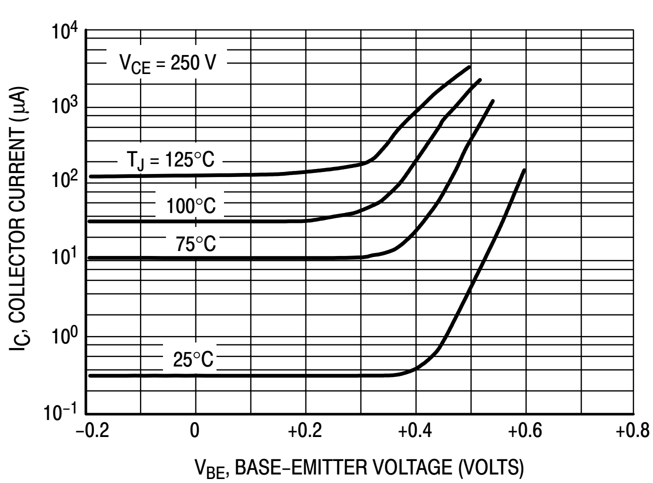


Figure 5. Collector Cutoff Region

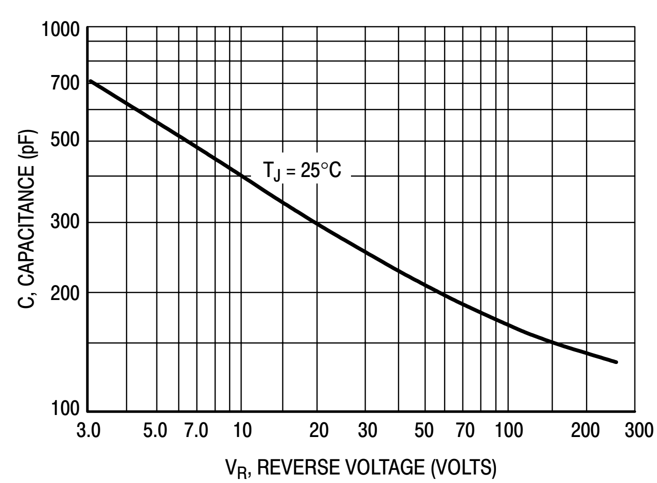
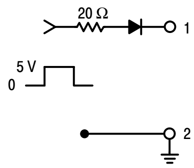
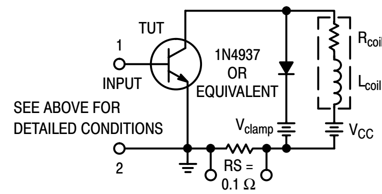
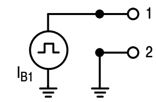
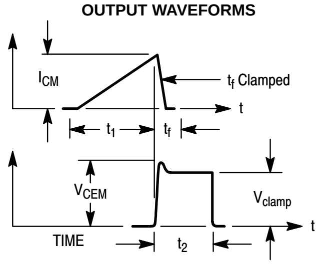
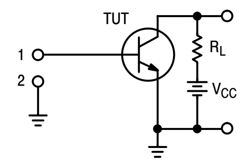


Figure 6. Output Capacitance

Table 1. Test Conditions for Dynamic Performance

<table>
<tr><th></th><th>$V_{CEO(sus)}$</th><th>RBSOA AND INDUCTIVE SWITCHING</th><th>RESISTIVE SWITCHING</th></tr>
<tr><td>INPUT CONDITIONS</td><td>
PW Varied to Attain
I_C = 100 mA</td><td>INDUCTIVE TEST CIRCUIT
</td><td>TURN–ON TIME

I_{B1} adjusted to
obtain the forced
h_{FE} desired
TURN–OFF TIME
Use inductive switching
driver as the input to
the resistive test circuit.</td></tr>
<tr><td>CIRCUIT VALUES</td><td>L_{coil} = 10 mH, V_{CC} = 10 V
R_{coil} = 0.7 Ω
V_{clamp} = $V_{CEO(sus)}$</td><td>L_{coil} = 180 μH
R_{coil} = 0.05 Ω
V_{CC} = 20 V</td><td>V_{CC} = 175 V
R_L = 5.6 Ω
Pulse Width = 25 μs</td></tr>
<tr><td>TEST CIRCUITS</td><td colspan="2">OUTPUT WAVEFORMS

t_1 Adjusted to
Obtain I_C
$t_1 \approx \frac{L_{coil}(I_{CM})}{V_{CC}}$
$t_2 \approx \frac{L_{coil}(I_{CM})}{V_{Clamp}}$
Test Equipment
Scope — Tektronix
475 or Equivalent</td><td>RESISTIVE TEST CIRCUIT
</td></tr>
</table>

*Adjust –V such that $V_{BE(off)}$ = 5 V except as required for RBSOA (Figure 14).

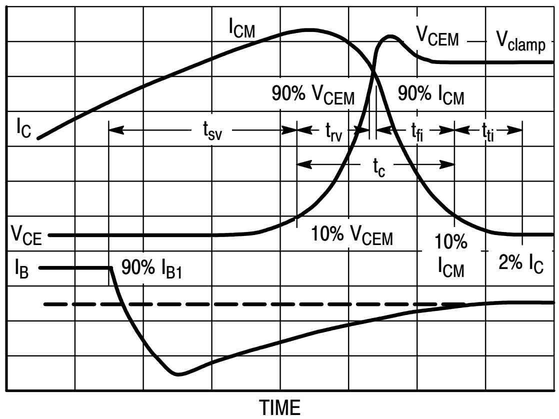


Figure 7. Inductive Switching Measurements

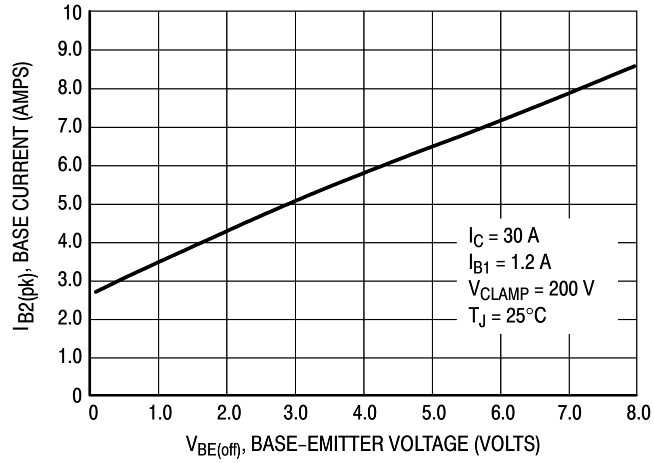


Figure 8. Typical Peak Reverse Base Current

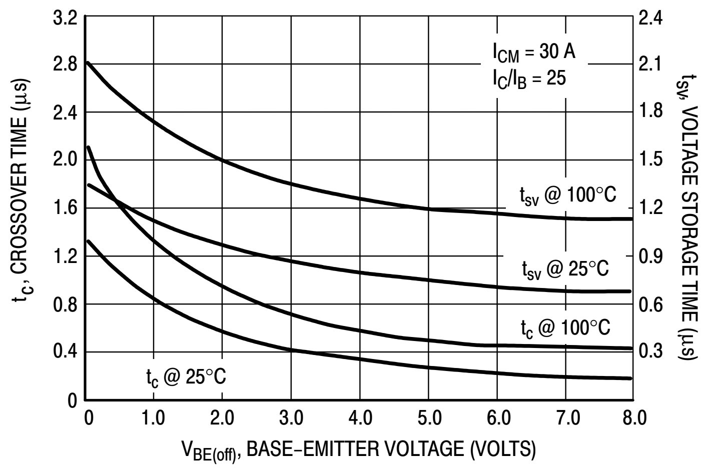


Figure 9. Typical Inductive Switching Times

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}
t_{rv} = Voltage Rise Time, 10–90% V_{CEM}
t_{fi} = Current Fall Time, 90–10% I_{CM}
t_{ti} = Current Tail, 10–2% I_{CM}
t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN–222A:

$$P_{SWT} = 1/2\ V_{CC}\ I_C\ (t_c)\ f$$

In general, $t_{rv} + t_{fi} \cong t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING

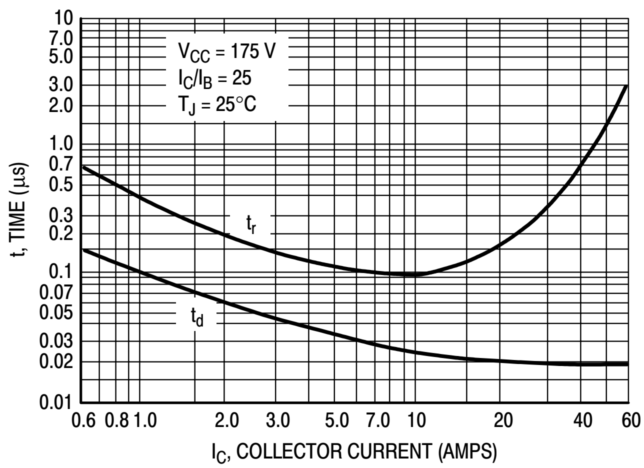


Figure 10. Typical Turn–On Switching Times

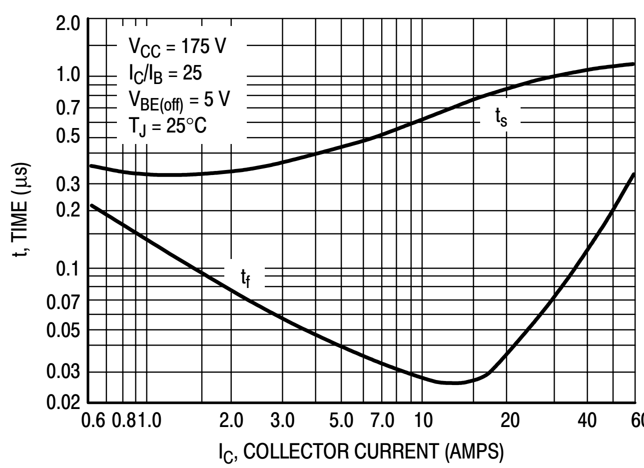


Figure 11. Typical Turn–Off Switching Times

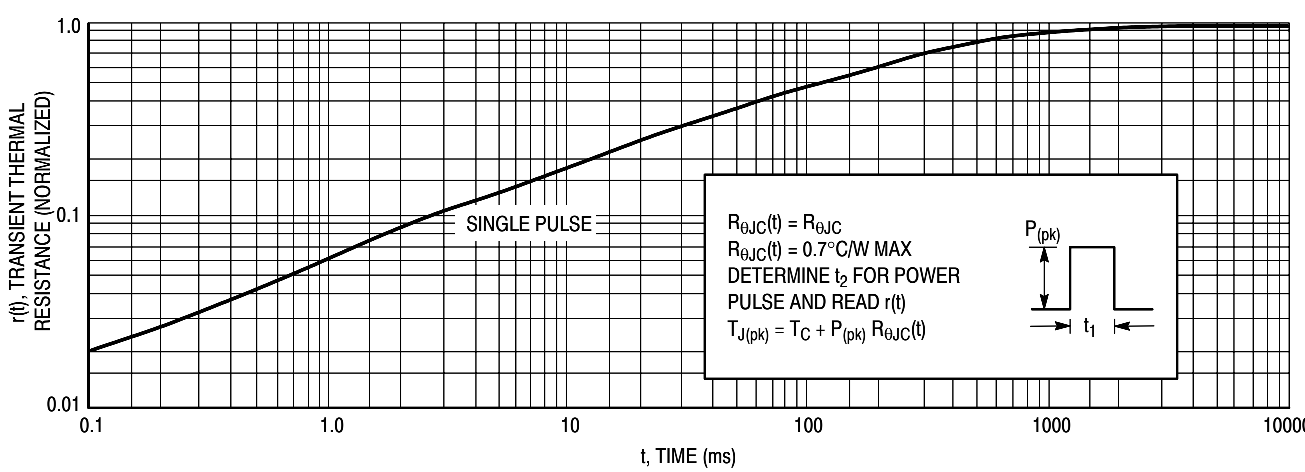


Figure 12. Thermal Response

The Safe Operating Area figures shown in Figures 13 and are specified for these devices under the test conditions shown.

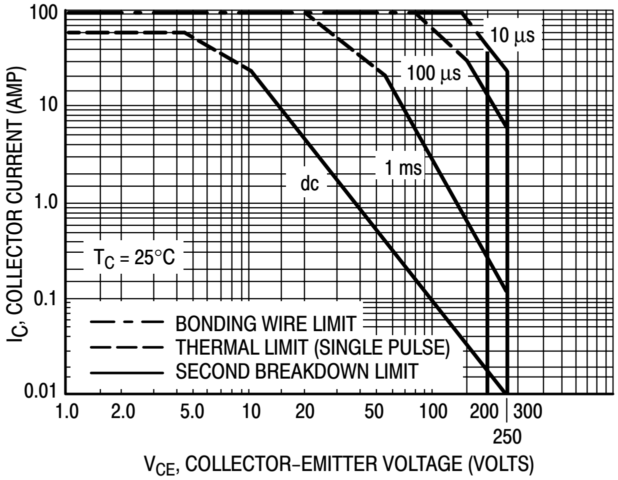


Figure 13. Maximum Forward Bias Safe Operating Area

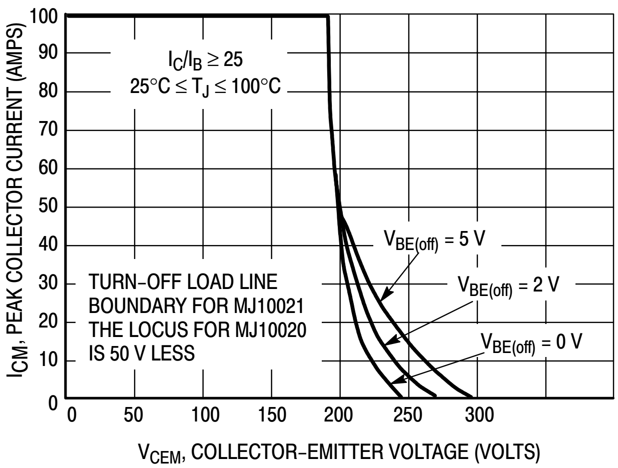


Figure 14. Maximum RBSOA, Reverse Bias Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C – V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 13 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_{J(pk)}$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For Inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage–current condition allowable during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives the RBSOA characteristics.

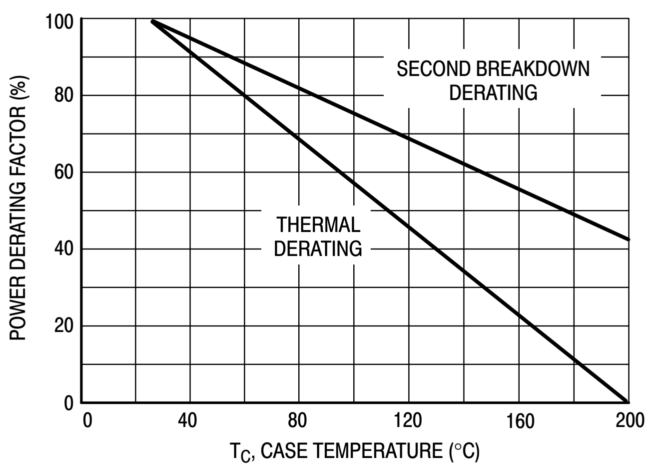
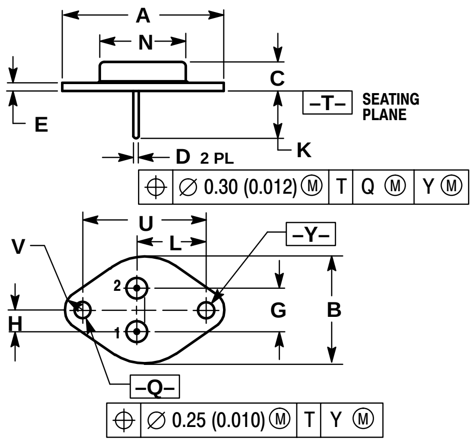


Figure 15. Power Derating

PACKAGE DIMENSIONS

CASE 197A–05
TO–204AE (TO–3)
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.530 REF		38.86 REF	
B	0.990	1.050	25.15	26.67
C	0.250	0.335	6.35	8.51
D	0.057	0.063	1.45	1.60
E	0.060	0.070	1.53	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	0.760	0.830	19.31	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

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