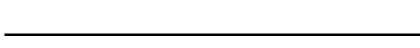
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April 1<sup>st</sup>, 2010 Renesas Electronics Corporation

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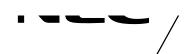


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#### **DATA SHEET**



# MOS FIELD EFFECT TRANSISTOR NP100P06PDG

# SWITCHING P-CHANNEL POWER MOSFET

#### **DESCRIPTION**

The NP100P06PDG is P-channel MOS Field Effect Transistor designed for high current switching applications.

#### <R> ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE	
NP100P06PDG-E1-AY Note		Tara 000 alaad	TO 000 (MD 057D)	
NP100P06PDG-E2-AY Note	Pure Sn (Tin)	Tape 800 p/reel	TO-263 (MP-25ZP)	

Note Pb-free (This product does not contain Pb in external electrode.)

#### **FEATURES**

• Super low on-state resistance

 $R_{DS(on)1} = 6.0 \text{ m}\Omega \text{ MAX}. \text{ (V}_{GS} = -10 \text{ V}, I_{D} = -50 \text{ A})$ 

 $R_{DS(on)2} = 7.8 \text{ m}\Omega \text{ MAX.} \text{ (V}_{GS} = -4.5 \text{ V}, I_{D} = -50 \text{ A})$ 

• High current rating: I<sub>D(DC)</sub> = ∓100 A

#### ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (Ves = 0 V)	VDSS	-60	V
Gate to Source Voltage (VDS = 0 V)	Vgss	∓20	V
Drain Current (DC) (Tc = 25°C)	I <sub>D(DC)</sub>	∓100	Α
Drain Current (pulse) Note1	D(pulse)	∓300	Α
Total Power Dissipation (Tc = 25°C)	P <sub>T1</sub>	200	W
Total Power Dissipation (T <sub>A</sub> = 25°C)	P <sub>T2</sub>	1.8	W
Channel Temperature	Tch	175	°C
Storage Temperature	T <sub>stg</sub>	-55 to +175	°C
Single Avalanche Current Note2	las	64	Α
Single Avalanche Energy Note2	Eas	420	mJ

**Notes 1.** PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1%

2. Starting T<sub>ch</sub> = 25°C, V<sub>DD</sub> = -30 V, R<sub>G</sub> = 25  $\Omega$ , V<sub>GS</sub> = -20  $\rightarrow$  0 V

#### THERMAL RESISTANCE

Channel to Case Thermal Resistance	Rth(ch-C)	0.75	°C/W
Channel to Ambient Thermal Resistance	Rth(ch-A)	83.3	°C/W

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(TO-263)





#### **ELECTRICAL CHARACTERISTICS (TA = 25°C)**

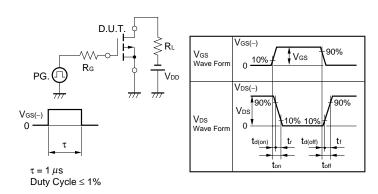
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V <sub>DS</sub> = -60 V, V <sub>GS</sub> = 0 V			-10	μΑ
Gate Leakage Current	Igss	V <sub>GS</sub> = ∓20 V, V <sub>DS</sub> = 0 V			∓100	nA
Gate to Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1 mA	-1.0	-1.6	-2.5	V
Forward Transfer Admittance Note	<b>y</b> fs	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -50 A	43	86		S
Drain to Source On-state Resistance Note	RDS(on)1	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -50 A		4.4	6.0	mΩ
	RDS(on)2	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -50 A		5.0	7.8	mΩ
Input Capacitance	Ciss	V <sub>DS</sub> = -10 V,		15000		pF
Output Capacitance	Coss	V <sub>GS</sub> = 0 V,		1810		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		840		pF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = -30 V, I <sub>D</sub> = -45 A,		28		ns
Rise Time	tr	V <sub>GS</sub> = -10 V,		35		ns
Turn-off Delay Time	t <sub>d(off)</sub>	R <sub>G</sub> = 0 Ω		275		ns
Fall Time	tr			100		ns
Total Gate Charge	Q <sub>G</sub>	$V_{DD} = -48 \text{ V},$		300		nC
Gate to Source Charge	Qgs	V <sub>GS</sub> = -10 V,		35		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = -100 A		85		nC
Body Diode Forward Voltage Note	V <sub>F(S-D)</sub>	I <sub>F</sub> = -100 A, V <sub>GS</sub> = 0 V		0.92	1.5	V
Reverse Recovery Time	trr	I <sub>F</sub> = -100 A, V <sub>GS</sub> = 0 V,		67		ns
Reverse Recovery Charge	Qrr	di/dt = -100 A/μs		135		nC

**Note** Pulsed test PW  $\leq$  350  $\mu$ s, Duty Cycle  $\leq$  2%

#### **TEST CIRCUIT 1 AVALANCHE CAPABILITY**

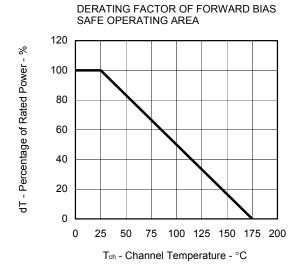
# $V_{GS} = -20 \rightarrow 0 \text{ V}$ $V_{DD}$ $V_{DD}$

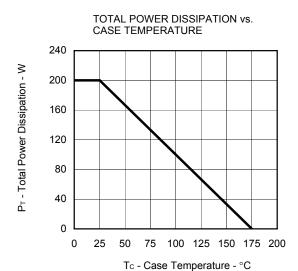
#### TEST CIRCUIT 2 SWITCHING TIME



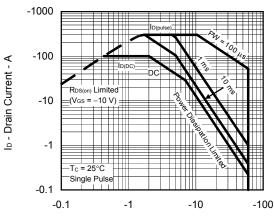
#### **TEST CIRCUIT 3 GATE CHARGE**

#### TYPICAL CHARACTERISTICS (TA = 25°C)



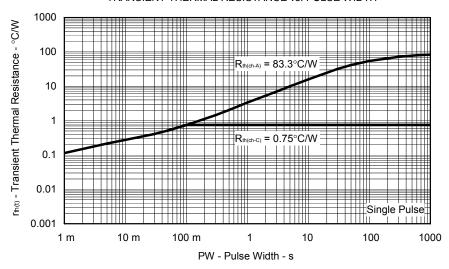


#### FORWARD BIAS SAFE OPERATING AREA



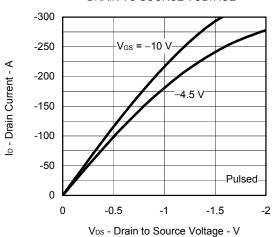
V<sub>DS</sub> - Drain to Source Voltage - V

#### TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

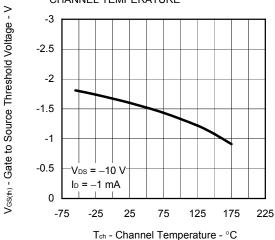


3

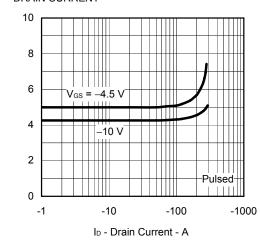




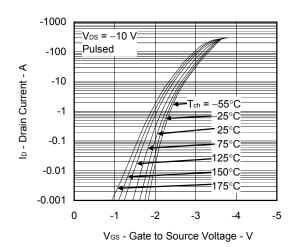
# GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



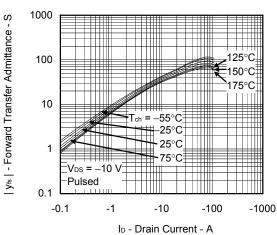
# DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



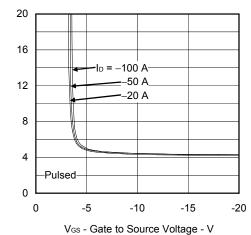
#### FORWARD TRANSFER CHARACTERISTICS



### FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

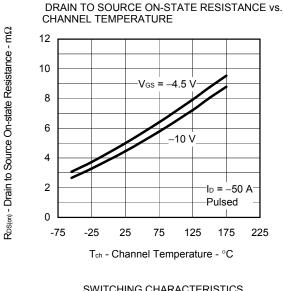


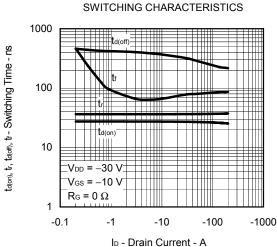
# DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

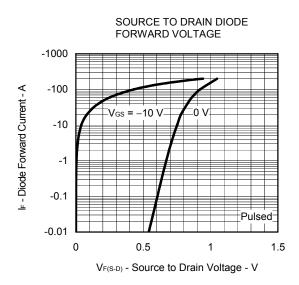


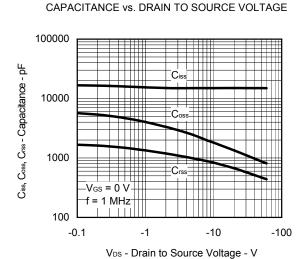
 $\mathsf{Res}_{(\mathsf{on})}$  - Drain to Source On-state Resistance -  $m\Omega$ 

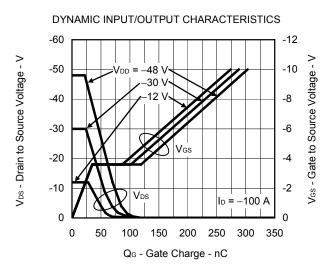
RDS(ση) - Drain to Source On-state Resistance - mΩ

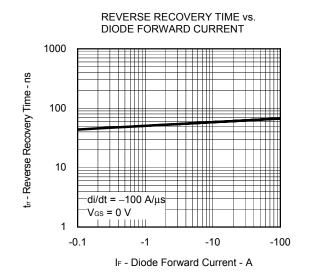






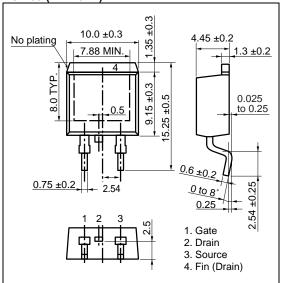




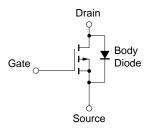


#### PACKAGE DRAWING (Unit: mm)

#### TO-263 (MP-25ZP)



#### **EQUIVALENT CIRCUIT**



**Remark** Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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