

NP180N04TUJ

MOS FIELD EFFECT TRANSISTOR

R07DS0180EJ0100 Rev.1.00 Dec 17, 2010

Description

The NP180N04TUJ is N-channel MOS Field Effect Transistor designed for high current switching applications.

Features

- Low on-state resistance
 - --- $R_{DS(on)}$ = 1.5 mΩ MAX. (V_{GS} = 10 V, I_D = 90 A)
- Low Ciss: Ciss = 9500 pF TYP. $(V_{DS} = 25 \text{ V})$
- Designed for automotive application and AEC-Q101 qualified

Ordering Information

Part No.	LEAD PLATING	PACKING	Package
NP180N04TUJ -E1-AY *1	Pure Sn (Tin)	Tape 800 p/reel	TO-263-7pin, Taping (E1 type)
NP180N04TUJ -E2-AY *1			TO-263-7pin, Taping (E2 type)

Note: *1. Pb-free (This product does not contain Pb in the external electrode.)

Absolute Maximum Ratings $(T_A = 25^{\circ}C)$

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V _{GS} = 0 V)	V _{DSS}	40	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS}	±20	V
Drain Current (DC) (T _C = 25°C)	I _{D(DC)}	±180	Α
Drain Current (pulse) *1	I _{D(pulse)}	±720	Α
Total Power Dissipation (T _C = 25°C)	P _{T1}	348	W
Total Power Dissipation (T _A = 25°C) *2	P _{T2}	1.8	W
Channel Temperature	T _{ch}	175	°C
Storage Temperature	T _{stg}	-55 to +175	°C
Repetitive Avalanche Current *3	I _{AR}	72	Α
Repetitive Avalanche Energy *3	E _{AR}	518	mJ

Thermal Resistance

Channel to Case Thermal Resistance $R_{th(ch-C)}$ 0.43 °C/W Channel to Ambient Thermal Resistance *2 $R_{th(ch-A)}$ 83.3 °C/W

Notes: *1. T_C = 25°C, PW \leq 10 μ s, Duty Cycle \leq 1%

*2. Mounted on glass epoxy substrate of 40 mm x 40 mm x 0.8 mmt

*3. $T_{ch(peak)} \le 150^{\circ}C$, $R_G = 25 \Omega$

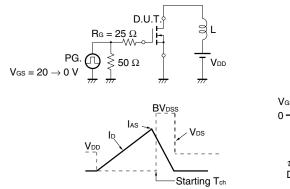
Electrical Characteristics (T_A = 25°C)

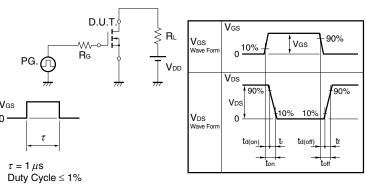
Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I _{DSS}			1	μΑ	V _{DS} = 40 V, V _{GS} = 0 V
Gate Leakage Current	I _{GSS}			±100	nA	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$
Gate to Source Threshold Voltage	$V_{GS(th)}$	2.0	3.0	4.0	V	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$
Forward Transfer Admittance *1	y _{fs}	65	130		S	$V_{DS} = 5 \text{ V}, I_{D} = 90 \text{ A}$
Drain to Source On-state Resistance *1	R _{DS(on)}		1.2	1.5	mΩ	V _{GS} = 10 V, I _D = 90 A
Input Capacitance	C _{iss}		9500	14250	pF	$V_{DS} = 25 V$,
Output Capacitance	Coss		1250	1880	pF	$V_{GS} = 0 V$,
Reverse Transfer Capacitance	C _{rss}		410	740	pF	f = 1 MHz
Turn-on Delay Time	t _{d(on)}		45	100	ns	$V_{DD} = 20 \text{ V}, I_D = 90 \text{ A},$
Rise Time	t _r		22	60	ns	$V_{GS} = 10 \text{ V},$
Turn-off Delay Time	$t_{d(off)}$		100	200	ns	$R_G = 0 \Omega$
Fall Time	t _f		15	40	ns	
Total Gate Charge	Q _G		150	230	nC	V _{DD} = 32 V,
Gate to Source Charge	Q _{GS}		35		nC	$V_{GS} = 10 \text{ V},$
Gate to Drain Charge	Q_{GD}		50		nC	I _D = 180 A
Body Diode Forward Voltage *1	V _{F(S-D)}		0.9	1.5	V	I _F = 180 A, V _{GS} = 0 V
Reverse Recovery Time	t _{rr}		68		ns	I _F = 180 A, V _{GS} = 0 V,
Reverse Recovery Charge	Q _{rr}		135		nC	di/dt = 100 A/μs

Note: *1. Pulsed

TEST CIRCUIT 1 AVALANCHE CAPABILITY

TEST CIRCUIT 2 SWITCHING TIME



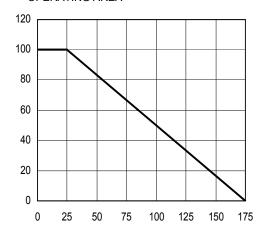


TEST CIRCUIT 3 GATE CHARGE

dT - Percentage of Rated Power - %

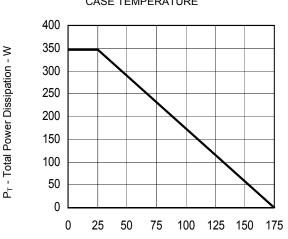
Typical Characteristics ($T_A = 25^{\circ}C$)

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



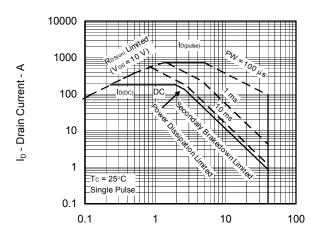
T_C - Case Temperature - °C

TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



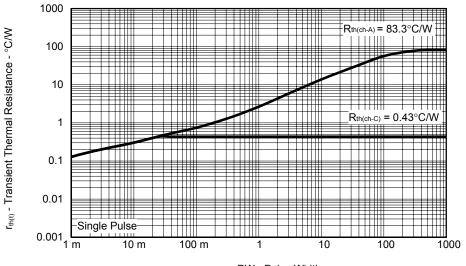
 T_{C} - Case Temperature - $^{\circ}\text{C}$

FORWARD BIAS SAFE OPERATING AREA



 $V_{\text{\scriptsize DS}}$ - Drain to Source Voltage - V

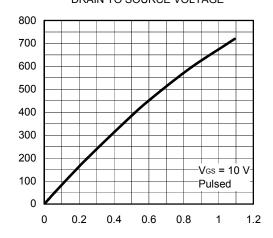
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



PW - Pulse Width - s

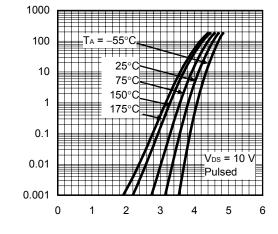
I_D - Drain Current - A

DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



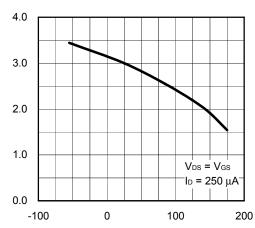
V_{DS} - Drain to Source Voltage - V

FORWARD TRANSFER CHARACTERISTICS



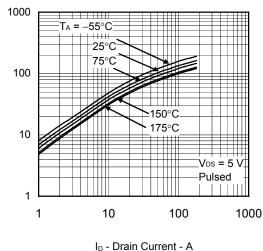
V_{GS} - Gate to Source Voltage - V

GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE

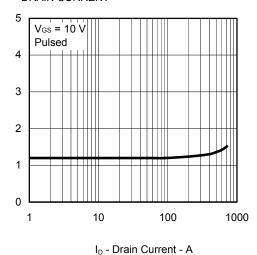


T_{ch} - Channel Temperature - °C

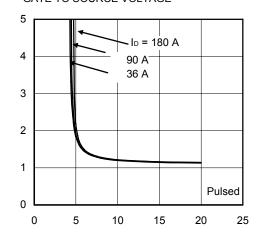
FORWARD TRANSFER ADMITTANCE vs. DRAIN **CURRENT**



DRAIN TO SOURCE ON-STATE RESISTANCE vs. **DRAIN CURRENT**



DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



V_{GS} - Gate to Source Voltage - V

 $R_{\text{DS(on)}}$ - Drain to Source On-state Resistance - $m\Omega$

Ip - Drain Current - A

y_{fs} | - Forward Transfer Admittance - S

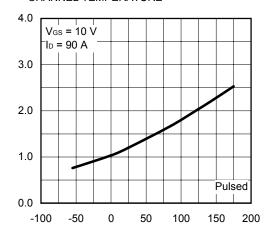
 $V_{\text{GS}(\text{th})}\text{-}$ Gate to Source Threshold Voltage - V

 $\mathsf{R}_{\mathsf{DS}(\mathsf{on})}$ - Drain to Source On-state Resistance - $m\Omega$

t_{d(on)}, t_r, t_{d(off)}, t_f - Switching Time - ns

I_F - Diode Forward Current - A

DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



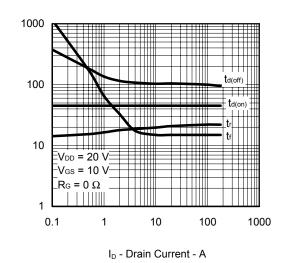
T_{ch} - Channel Temperature - $^{\circ}C$

100000 Ld 90 10000 Coss 10000 Vos = 0 V f = 1 MHz 100 0.1 1 10 100

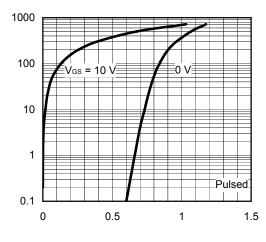
V_{DS} - Drain to Source Voltage - V

CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

SWITCHING CHARACTERISTICS

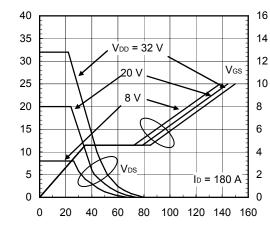


SOURCE TO DRAIN DIODE FORWARD VOLTAGE



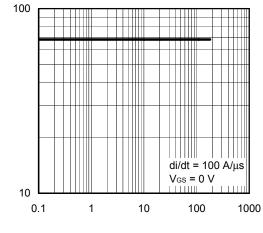
 $V_{F(S-D)}$ - Source to Drain Voltage - V

DYNAMIC INPUT/OUTPUT CHARACTERISTICS



Q_G - Gate Charge - nC

REVERSE RECOVERY TIME vs. DRAIN CURRENT



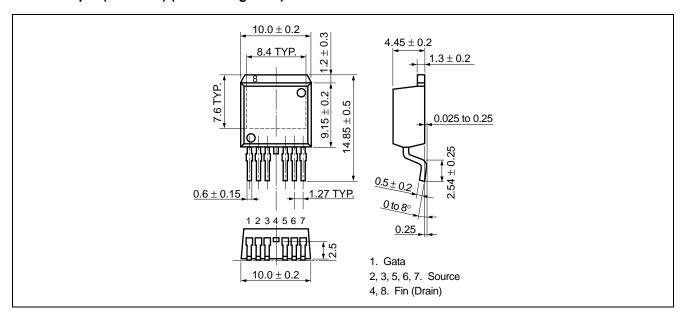
I_F - Drain Current - A

V_{DS} - Drain to Source Voltage - V

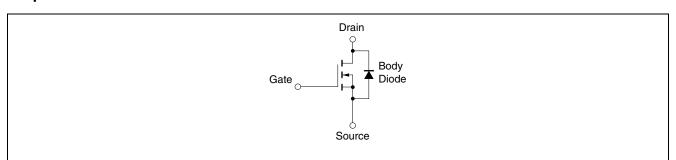
t_{rr} - Reverse Recovery Time - ns

Package Drawings (Unit: mm)

TO-263-7pin (MP-25ZT) (Mass: 1.5 g TYP.)



Equivalent Circuit



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Revision History

NP180N04TUJ Data Sheet

		Description		
Rev.	Date	Page	Summary	
1.00	Dec 17, 2010	_	First Edition Issued	

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