Accelerator Series FPGAs – ACT 3 PCI Compliant Family

Feature Set

- Up to 10,000 Gate Array equivalent gates
- Up to 250 MHz on-chip performance
- 7.5 ns Clock-to-Output
- Up to 1,153 dedicated flip-flops
- Up to 228 user-programmable I/O pins
- PCI compliant I/O drivers
- Four High-Speed, Low Skew clocks
- Highly predictable, synthesis friendly architecture supports high-level design methodologies
- 100% module utilization with automatic place and route tools
- Deterministic, user-controllable timing via DirectTime software tools

Actel enhanced the popular ACT 3 Accelerator Series of FPGAs to include PCI compliant I/O drivers. ACT 3 FPGAs are based upon Actel's proprietary PLICE antifuse technology and state-of-the-art 0.6-micron CMOS process. ACT 3 devices offer a high performance, PCI compliant programmable solution. The ACT 3 PCI Compliant family delivers 250 MHz on-chip operation and 7.5 nanosecond clock-to-output performance with capacities spanning from 4,000 to 10,000 gate array equivalent gates. The PCI compliant ACT 3 devices are denoted with a "P" designator and are shown in the chart below.

The ACT 3 PCI Compliant devices were specifically designed to be 100 percent compliant with PCI Local Bus Specification (version 2.1). Combining PCI-compliance with the industry's most synthesis friendly architecture provides the fastest PCI solution of any FPGA, regardless of whether you're designing a PCI interface from scratch or using a third-party synthesizable "core."

Actel's ACT 3 PCI Compliant devices provide a high capacity, synthesis friendly programmable solution to PCI applications. The following headings detail the pertinent PCI Local Bus Specifications along with the corresponding ACT 3 parameters. The section numbers in the notes denote the pertinent section in the PCI Local Bus Specification (version 2.1). ACT 3 devices comply 100% to the electrical and timing specifications detailed in the PCI specification. However, as with all programmable logic devices, the performance of the final product depends upon the user's design and optimization techniques. The electrical and timing specifications are specified as in version 2.1 of the PCI Specification. Used in conjunction with the PCI Local Bus Specification, ACT 3 devices can offer a cost effective, high performance PCI solution.

ACT 3 PCI-Compliant Devices

Device	A1440BP	A1460BP	A14100BP
Logic Gates	4,000	6,000	10,000
Logic Modules	564	848	1,377
Sequential Modules	288	432	697
Combinatorial Modules	276	416	680
Dedicated Flip-Flops[1]	568	768	1,153
User I/Os (maximum)	140	168	228
Packages (by pin count)			
PQFP	160	160, 208	
RQFP			208
TQFP	176	176	
BGA		225	313

Note:

1. One flip-flop/S-Module, two flip-flops/IO-Module

Electrical Specifications

The PCI bus specifies I/O drivers in terms of the DC and AC characteristics. However, since the PCI bus drivers spend a relatively large proportion of time transitioning from one power rail to the other, PCI drivers are primarily characterized by their V/I curves (Tables 1 and 2).

Output Drive Characteristics for 5.0 V Signaling

ACT 3 PCI device I/O drivers were designed specifically for high-performance PCI systems. Figures 1 and 2 show the typical output drive characteristics of the 5.0 V ACT 3 devices. ACT 3 output drivers are compliant with the PCI Local Bus Specification.

Table 1 • DC Specification for 5.0V Signaling[1]

			PCI			ACT 3	
Symbol	**Parameter**	**Condition**	**Minimum**	**Maximum**	**Units**	**Minimum**	**Maximum**
V_{CC}	Supply Voltage		4.75	5.25	V	4.75	5.25[2]
V_{IH}	Input High Voltage		2	Vcc + 0.5	V	2	Vcc + 0.5
V_{IL}	Input Low Voltage		–0.5	0.8	V	–0.3	0.8
I_{IH}	Input High Current	Vin = 2.7		70	uA	—	10
I_{IL}	Input Low Current	Vin=0.5		–70	uA	—	–10
V_{OH}	Output High Voltage	Iout = –2 mA	2.4		V	3.7	
V_{OL}	Output Low Voltage	Iout = 3 mA, 6 mA		0.55	V	—	0.33
C_{IN}	Input pin capacitance			10	pF	—	10
C_{CLK}	CLK pin capacitance		5	12	pF	—	10
L_{PIN}	Pin inductance			20	nH	—	< 8 nH[3]

Notes:

1. PCI Local Bus Specification section 4.2.1.1.

2. Maximum rating for Vcc: –0.5V to 7.0V. Refer to Accelerator Series FPGAs ACT 3 Family data sheet.

3. Dependent upon the chosen package. PCI recommends QFP packaging to reduce pin inductance and capacitance.

Table 2 • AC Specifications for 5.0V Signaling[1]

			PCI			ACT 3	
Symbol	**Parameter**	**Condition**	**Minimum**	**Maximum**	**Units**	**Minimum**	**Maximum**
I_{CL}	Low Clamp Current	–5 < Vin ≤ –1	–25 + (Vin +1) /0.015		mA	–50	–10
Slew (r)	Output rise slew rate	0.4V to 2.4V load	1	5	V/ns	1.8	2.8
Slew (f)	Output fall slew rate	2.4V to 0.4V load	1	5	V/ns	2.8	4.3

Note:

1. PCI Local Bus Specification section 4.2.1.2.

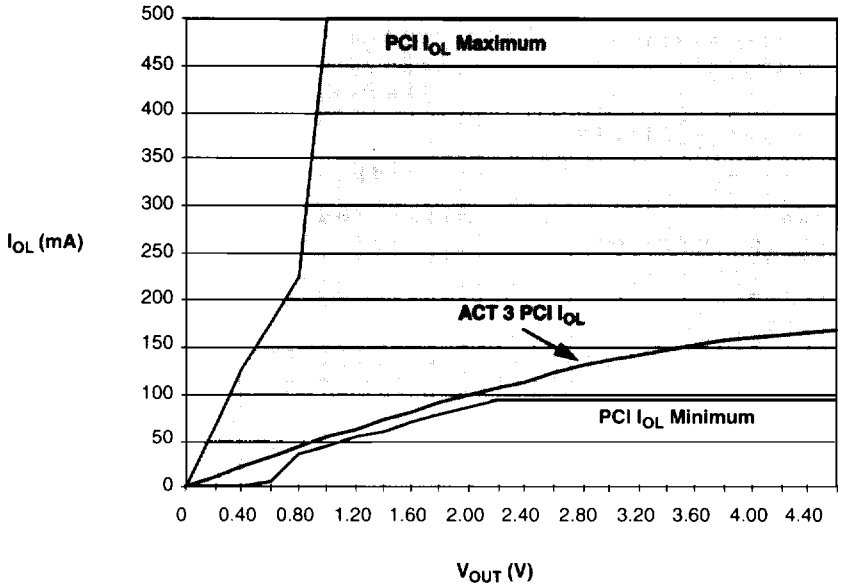

Figure 1 • Typical Output Drive Characteristics (Based upon simulation data)

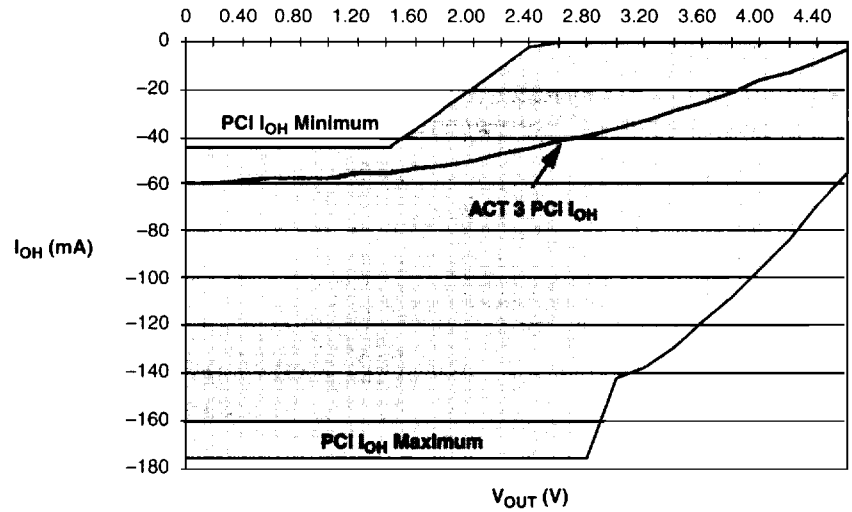

Figure 2 • Typical Output Drive Characteristics (Based upon simulation data)

System Timing Specification

The following heading lists the critical PCI timing parameters and the corresponding timing parameter for the ACT 3 PCI compliant devices. See Tables 3 and 4.

PCI Models

Actel will provide synthesizable VHDL and Verilog models for a PCI target interface, a PCI master interface and a PCI-PCI bridge interface. Consult your local Actel sales representative for more details.

Table 3 • Clock Specification for 33 MHz PCI[1]

		PCI			ACT 3	
Symbol	**Parameter**	**Minimum**	**Maximum**	**Units**	**Minimum**	**Maximum**
T_{CYC}	CLK Cycle Time	30	—	ns	4.0	—
T_{HIGH}	CLK High Time	11	—	ns	1.9	—
T_{LOW}	CLK Low Time	11	—	ns	1.9	—
—	CLK Skew	1	4	V/ns	—	4.0

Note:

1. PCI Local Bus Specification Section 4.2.3.1.

Table 4 • Timing Parameters for 33 MHz PCI[1]

		PCI			ACT 3	
Symbol	**Parameter**	**Minimum**	**Maximum**	**Units**	**Minimum**	**Maximum**
T_{VAL}	CLK to Signal Valid—bussed Signals	2	11	ns	2.0	7.5
$T_{VAL(PTP)}$	CLK to Signal Valid—point to point	2	12	ns	2.0	7.5
T_{ON}	Float to active	2		ns	2.0	4.0
T_{OFF}	Active to Float		28	ns	—	7.4[2]
T_{SU}	Input Setup time to CLK—bussed signals	7		ns	1.5	—
$T_{SU(PTP)}$	Input Setup time to CLK—point to point	10, 12		ns	1.5	—
T_H	Input Hold to CLK	0		ns	—	0

Notes:

1. Based upon simulation data for internal timing parameters. PCI Local Bus Specification Section 4.2.3.2.

2. Toff is system dependent. ACT 3 PCI devices have 7.4 ns turn-off time, reflection is typically an additional 10 ns.