ACT-DP16K32A
512K Dual-Port SRAM Module

Preliminary

AEROFLEX
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Features

- **High-density 512K CMOS Dual-Port SRAM module**
- **Fast access times**
  - **Commercial: 30, 35ns**
  - **Military: 40, 45ns**
- **MIL-PRF-38534 Compliant MCMs Available**
- **Fully asynchronous read/write operation from either port**
- **Easy to expand data bus width to 64 bits or more using the Master / Slave function**
- **Separate byte read/write signals for byte control**
- **On-chip port arbitration logic**
- **INT flag for port-to-port communication**
- **Full on-chip hardware support of semaphore signaling between ports**
- **Single 5V (±10%) power supply**
- **Inputs/outputs directly TTL-compatible**
- **Internal Decoupling Capacitors**
- **-55°C to +125°C Operating Temperature**
- **Packaging – Hermetic**
  - **121 Pin PGA Package, 1.35" x 1.35" x .175"**

AEROFLEX LABS INC. ISO 9001 CERTIFIED

Description

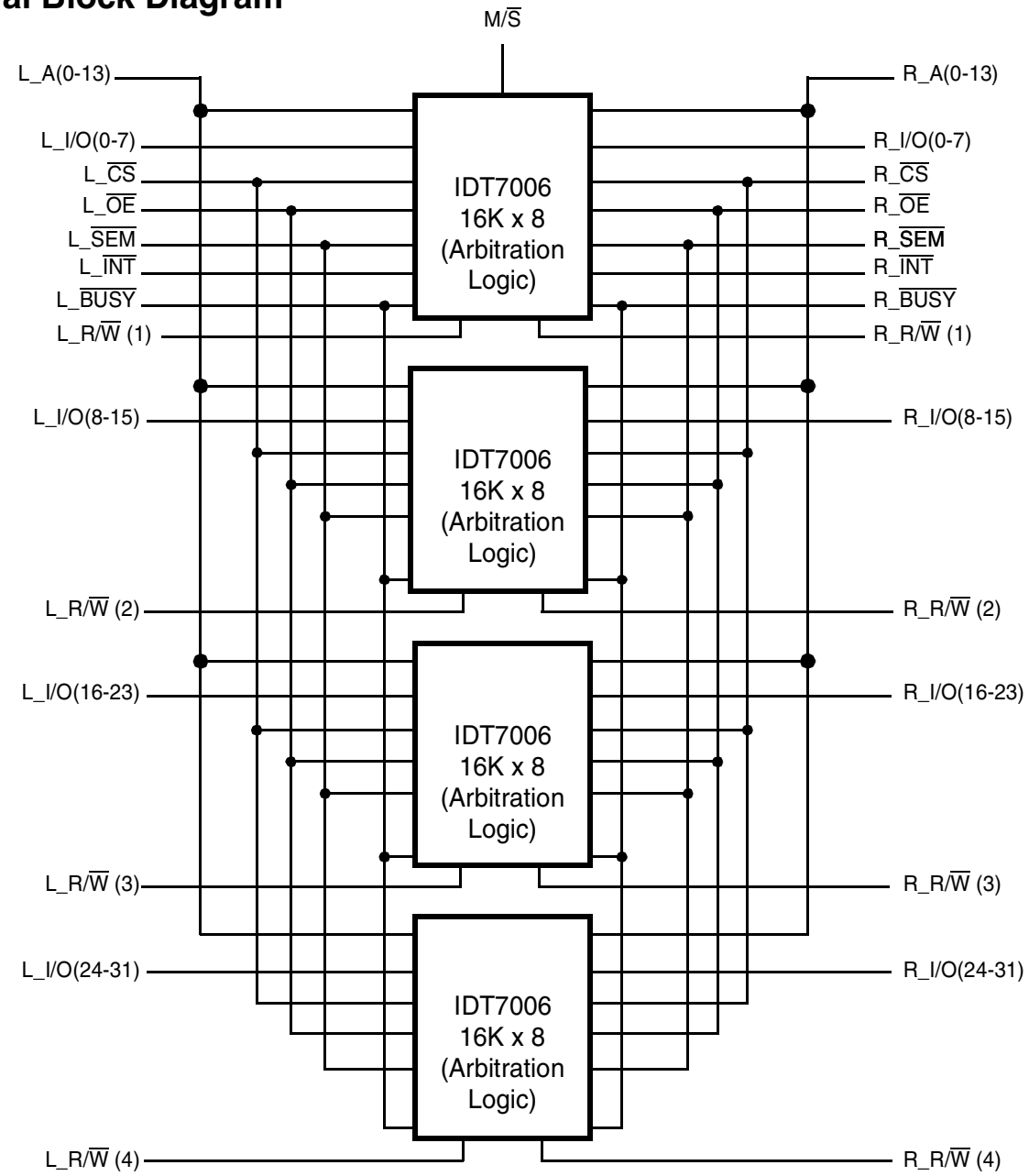
The Aeroflex ACTDP16K32A is a 16K x 32 high-speed CMOS Dual-Port Static RAM Module constructed on a co-fired ceramic 121 pin PGA (Pin Grid Array) 1.35 inches using four 16K x 8 (IDT7006 Die) Dual-Port Static RAMs. The ACTDP16K32A module is designed to be used as stand-alone 512K Dual-Port RAM or as a combination Master/Slave Dual-Port RAM for 64-bit or more word width systems. Using the Master/Slave approach in such system applications results in full-speed, error free operation without the need for additional discrete logic.

The module provides two independent ports with separate control, address, and I/O pins that permit independent and asynchronous access for reads or writes to any location in memory. System performance is enhanced by facilitating port-to-port communication via additional control signals $\overline{\text{SEM}}$ and $\overline{\text{INT}}$.

Maximum access times as fast as 30ns are available over the commercial temperature range and 40ns over the military temperature range.

The ACT-DP16K32A is manufactured in Aeroflex's 80,000 square foot MIL-PRF-38534 certified facility in Plainview, N.Y.

Functional Block Diagram



Pin Names

Left Port	Right Port	Description
L_A (0–13)	R_A (0–13)	Address Inputs
L_I/O (0–31)	R_I/O (0–31)	Data Inputs/Outputs
L_R/W (1–4)	R_R/W (1–4)	Read/Write Enables
L_CS	R_CS	Chip Select
L_OE	R_OE	Output Enable
L_BUSY	R_BUSY	Busy Flag
L_INT	R_INT	Interrupt Flag
L_SEM	R_SEM	Semaphore Control
M/S		Master/Slave Control
Vcc		Power
GND		Ground

Absolute Maximum Ratings[1]

Symbol	Rating	Commercial	Military	Units
T_{TERM}	Terminal Voltage with respect to GND	-0.5 to 7	-0.5 to 7	V
T_C	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

Notes:
1. Stresses above those listed under "Absolute Maximums Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Temperature and Supply Voltage[1]

Grade	Case Temperature	GND	Vcc
Military	-55 to +125°C	0V	5.0V±10%
Commercial	0 to +70°C	0V	5.0V±10%

Notes:
1. This is the parameter Tc.

Recommended DC Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units
V_{CC}	Supply Voltage	+4.5	+5.5	V
GND	Supply Voltage	0	0	V
V_{IH}	Input High Voltage	2.2	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	0.8	V

Notes:
1. $V_{IL} \geq$ -3.0V for pulse width less than 20ns.

DC Electrical Characteristics

(V_{CC} = 5.0V±10%, Tc = -55°C to +125°C or 0°C to +70°C)

Parameter	Sym	Conditions	Commercial		Military		Units
			Min	Max	Min	Max	
Output Low Voltage	V_{OL}	V_{CC} = Min, I_{OL} = 4 mA	-	0.4	-	0.4	V
Output High Voltage	V_{OH}	V_{CC} = Min, I_{OH} = -4 mA	2.4	-	2.4	-	V
Input Leakage Current (Address & Control)	I_{LI}	V_{CC} = Max, V_{IN} = GND to Vcc	-	40	-	40	µA
Input Leakage Current (Data)	I_{LI}	V_{CC} = Max, V_{IN} = GND to Vcc	-	10	-	10	µA
Output Leakage Current (Data)	I_{LO}	V_{CC} = Max, $\overline{CS} \geq V_{IH}$, Vout = GND to Vcc	-	10	-	10	µA
Dynamic Operating Current (Both Ports Active)	I_{CC2}	V_{CC} = Max, $\overline{CS} \leq V_{IL}$, $\overline{SEM}$ = Don't Care, Outputs Open, f = f_{MAX}	-	1360	-	1600	mA
Standby Suppy Current (Both Ports Active)	I_{SB}	V_{CC} = Max, L_$\overline{CS}$ and R_$\overline{CS} \geq V_{IH}$ Outputs Open, f = f_{MAX}	-	280	-	340	mA
Standby Suppy Current (One Port Active)	I_{SB1}	V_{CC} = Max, L_$\overline{CS}$ and R_$\overline{CS} \geq V_{IH}$ Outputs Open, f = f_{MAX}	-	1000	-	1160	mA
Standby Suppy Current (Both Ports Inactive)	I_{SB2}	L_$\overline{CS}$ and R_$\overline{CS} \geq V_{CC}$ – 0.2V, $V_{IN} > V_{CC}$ – 0.2V or < 0.2V L_$\overline{SEM}$ and R_$\overline{SEM} \geq V_{CC}$ – 0.2V	-	60	-	120	mA

Capacitance [1]

(Tc = +25°C, f = 1.0MHz)

Sym	Parameter	Conditions	Max	Units
C_{IN}(1)	Input Capacitance ($\overline{CS}$, $\overline{OE}$, $\overline{SEM}$, Address)	V_{IN} = 0V	40	pF
C_{IN}(2)	Input Capacitance (R/$\overline{W}$, I/O, $\overline{INT}$)	V_{IN} = 0V	12	pF
C_{IN}(3)	Input Capacitance ($\overline{BUSY}$, M/$\overline{S}$)	V_{IN} = 0V	45	pF
C_{OUT}	Output Capacitance (I/O)	V_{OUT} = 0V	12	pF

NOTE:
1. This parameter is guaranteed by design but not tested.

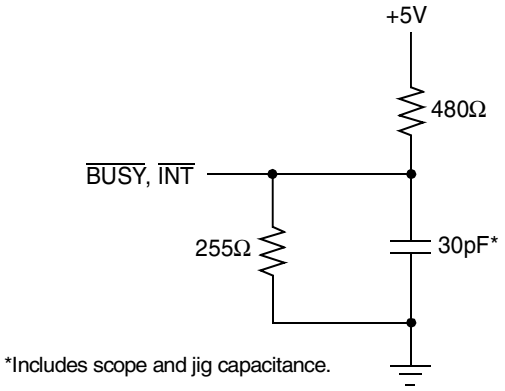


Figure 1 – Output Load

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

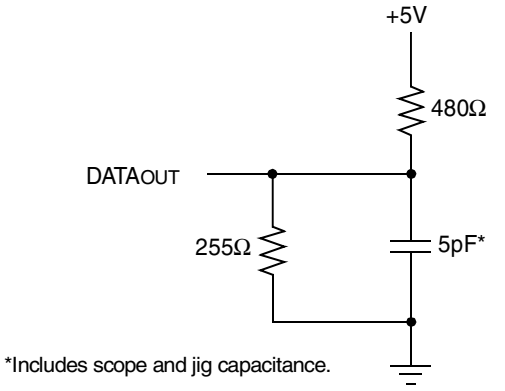


Figure 2 – Output Load
(For tchz, tclz, tohz, tolz, twhz, tow)

AC Characteristics

(V_{CC} = 5.0V ±10%, Tc = -55°C to +125°C or 0°C to +70°C)

Parameter	Sym	Commercial				Military				Units
		–030		–035		–040		–045		
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle										
Read Cycle Time	t_{RC}	30	-	35	-	40	-	45	-	ns
Address Access Time	t_{AA}	-	30	-	35	-	40	-	45	ns
Chip Select Access Time	t_{ACS}2	-	35	-	35	-	35	-	35	ns
Output Enable Access Time	t_{OE}	-	17	-	20	-	22	-	25	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	3	-	ns
Output to Low-Z	t_{LZ}1	3	-	3	-	3	-	5	-	ns
Output to High-Z	t_{HZ}1	-	15	-	15	-	17	-	20	ns
Chip Select to Power Up Tim	t_{PU}1	0	-	0	-	0	-	0	-	ns
Chip Deselect to Power Up Time	t_{PD}1	-	50	-	50	-	50	-	50	ns
Sem. Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	t_{SOP}	15	-	15	-	15	-	15	-	
Write Cycle										
Write Cycle Time	t_{WC}	30	-	35	-	40	-	45	-	ns
Chip Enable to End of Write	t_{CW}2	25	-	30	-	35	-	40	-	ns
Address Valid to End of Write	t_{AW}	25	-	30	-	35	-	40	-	ns
Address Set-Up Time	t_{AS}	0	-	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	25	-	30	-	35	-	40	-	ns

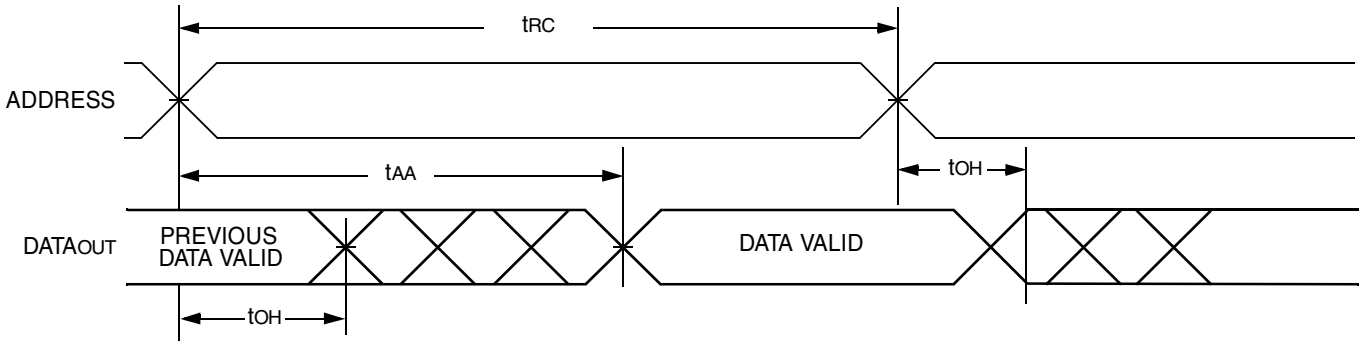
AC Characteristics (con't)

(V_{CC} = 5.0V ±10%, Tc = -55°C to +125°C or 0°C to +70°C)

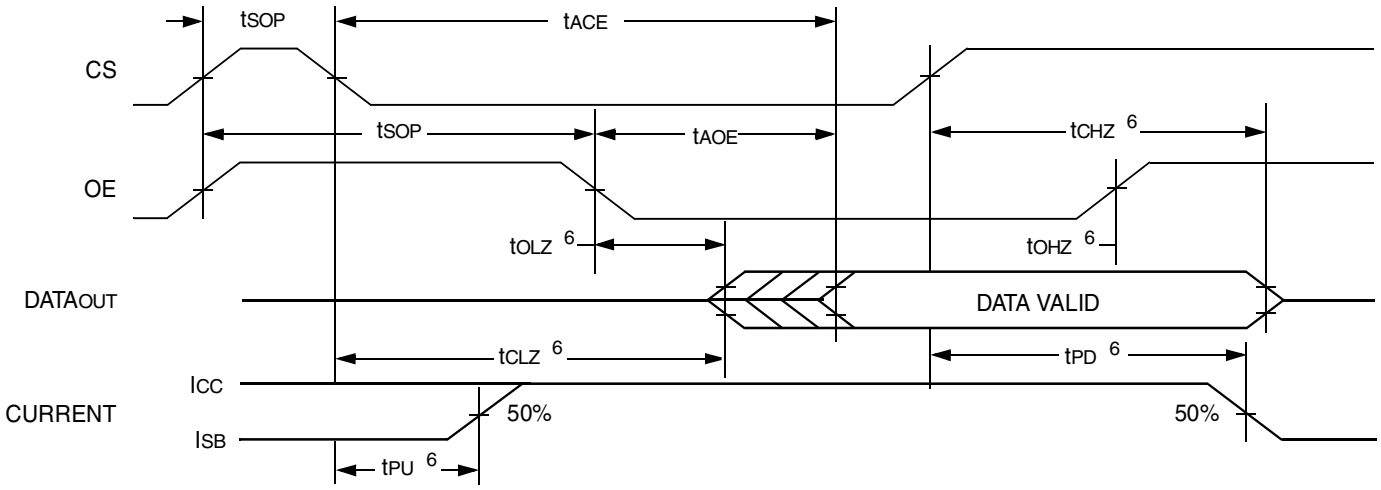
Parameter	Sym	Commercial				Military				Units
		–030		–035		–040		–045		
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Recovery Time	t_{WR}	0	-	0	-	0	-	0	-	ns
Data Valid to End-of-Write	t_{DW}	22	-	25	-	25	-	25	-	ns
Data Hold Time	t_{DH}	0	-	0	-	0	-	0	-	ns
Output to High-Z	t_{HZ}1	-	15	-	15	-	17	-	20	ns
Output Active from End of Write	t_{OW}1	0	-	0	-	0	-	0	-	ns
SEM Flag Write to Read Time	t_{SWRD}	10	-	10	-	10	-	10	-	ns
SEM Flag Contention Window	t_{SPS}	10	-	10	-	10	-	10	-	ns
Busy Cycle-Master Mode [3]										
BUSY Access Time to Address	t_{BAA}	-	30	-	35	-	35	-	35	ns
BUSY Disable Time to Address	t_{BDA}	-	25	-	30	-	30	-	30	ns
BUSY Access Time to Chip Select	t_{BAC}	-	25	-	30	-	30	-	30	ns
BUSY Disable Time to Chip Deselect	t_{BDC}	-	25	-	25	-	25	-	25	ns
Write Pulse to Data Delay	t_{WDD}5	-	55	-	60	-	65	-	70	ns
Write Data Valid to Read Data Delay	t_{DDD}	-	40	-	45	-	50	-	55	ns
Arbitration Priority Set-Up Time	t_{APS}6	5	-	5	-	5	-	5	-	ns
BUSY Disable to Valid Time	t_{BDD}	-	Note 9	-	Note 9	-	Note 9	-	Note 9	ns
Busy Cycle-Slave Mode [4]										
Write to BUSY Input	t_{WB}7	0	-	0	-	0	-	0	-	ns
Write Hold after BUSY	t_{WH}8	25	-	25	-	25	-	25	-	ns
Write Pulse to Data Delay	t_{WDD}5	-	55	-	60	-	65	-	70	ns
Interrupt Timing										
Address Set-Up Time	t_{AS}	0	-	0	-	0	-	0	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	0	-	ns
Interrupt Set Time	t_{INS}	-	25	-	30	-	32	-	35	ns
Interrupt Reset Time	t_{INR}	-	25	-	30	-	32	-	35	ns

NOTES:
1. This parameter is guaranteed by design but not tested.
2. To access RAM, $\overline{CS} \le V_{IL}$ and $\overline{SEM} \ge V_{IH}$. To access semaphore, $\overline{CS} \ge V_{IH}$ and $\overline{SEM} \le V_{IL}$.
3. When the module is being used in the Master Mode ($M/\overline{S} \ge V_{IH}$).
4. When the module is being used in the Slave Mode ($M/\overline{S} \le V_{IL}$).
5. Port-to-Port delay through the RAM cells from the writing port to the reading port.
6. To ensure that the earlier of the two ports wins.
7. To ensure that the write cycle is inhibited during contention.
8. To ensure that a write cycle is completed after contention.
9. t_{BDD} is a calculated parameter and is the greater of 0, t_{WDD} - t_{WP} (actual), or t_{DDD} - t_{WP} (actual).

Timing Waveform of Read Cycle No. 1, Either Side [1,2,4]

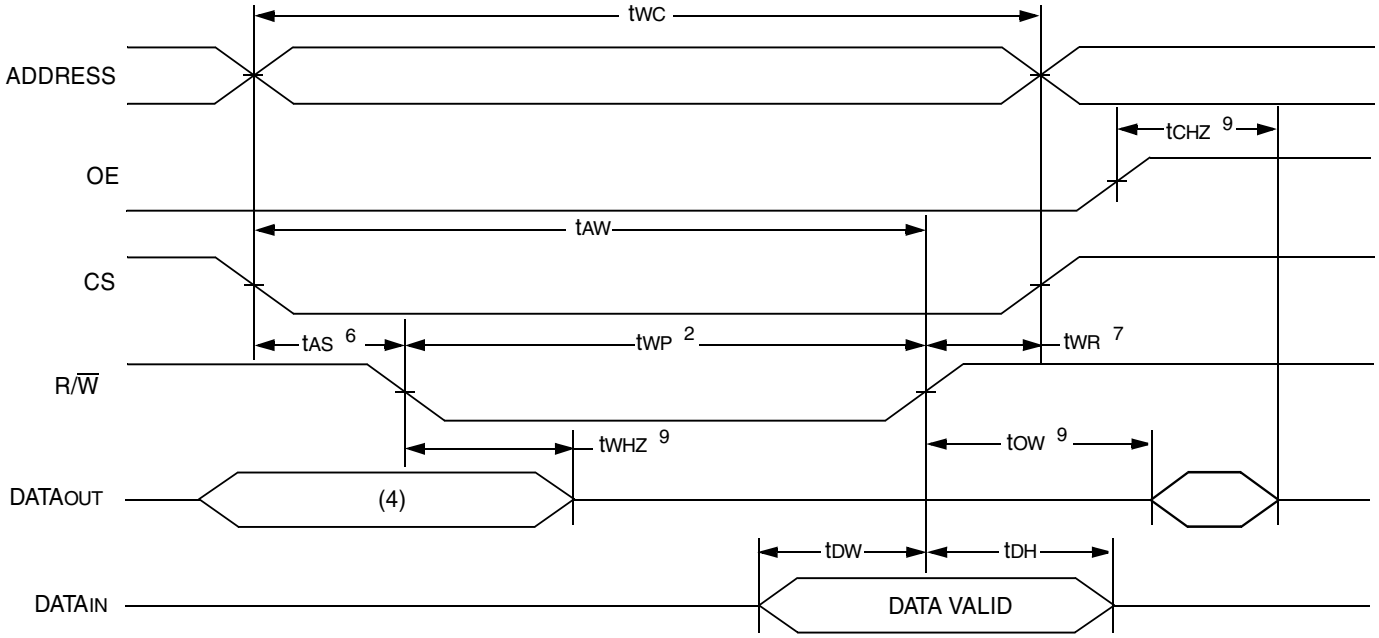


Timing Waveform of Read Cycle No. 2, Either Side [1,3,5]

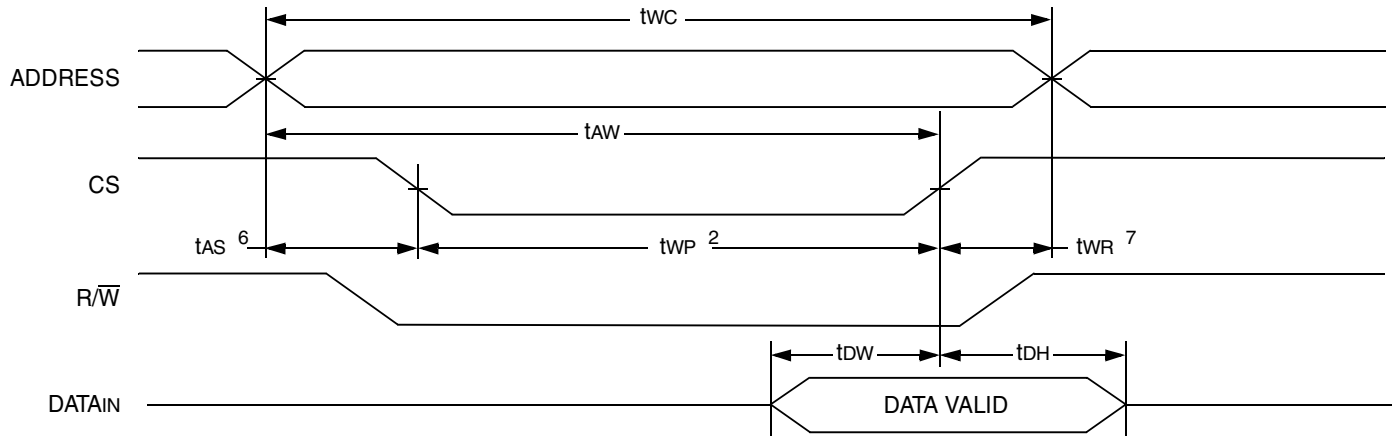


NOTES:
1. R/$\overline{W}$ is HIGH for Read Cycles
2. Device is continuously enabled $\overline{CS} \leq V_{IL}$. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition LOW.
4. $\overline{OE} \leq V_{IL}$
5. To access RAM, $\overline{CS} \leq V_{IL}$ and $\overline{SEM} \geq V_{IH}$. To access semaphore, $\overline{CS} \geq V_{IH}$ and $\overline{SEM} \leq V_{IL}$.
6. This parameter is guaranteed by design but not tested.

Timing Waveform of Write Cycle No. 1 (R/$\overline{W}$ Controlled Timing)[1,2,4]

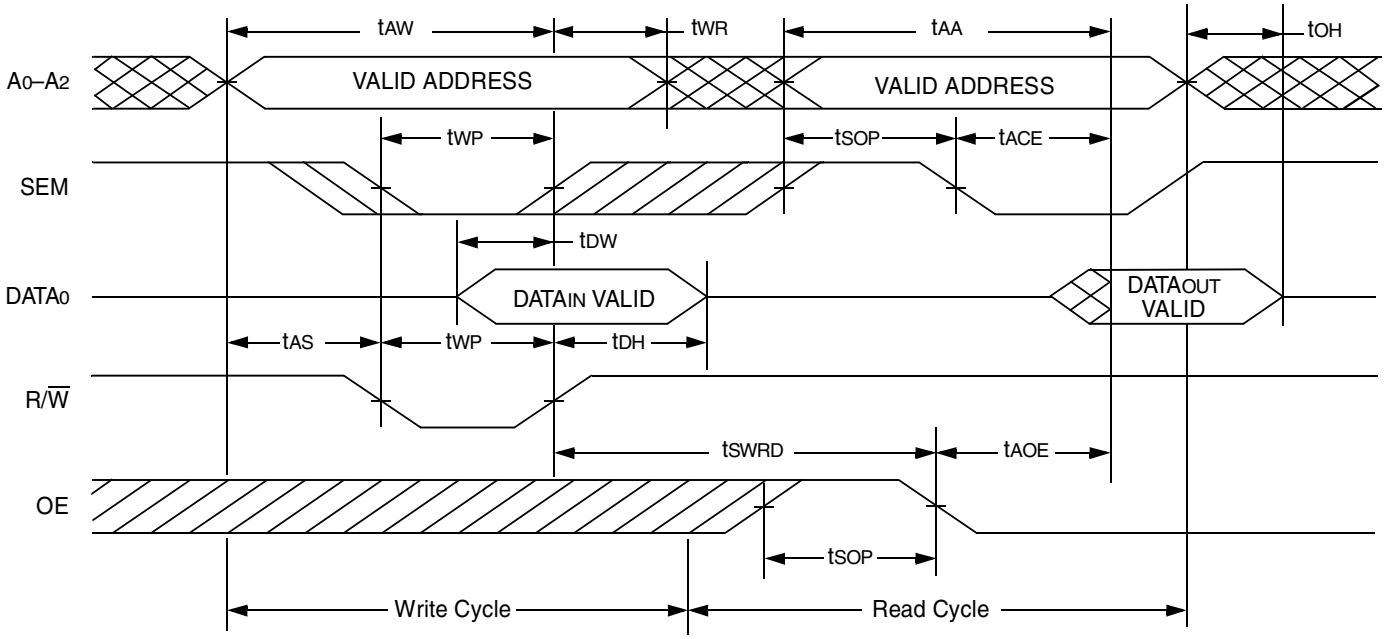


Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled Timing)[1,2,4]



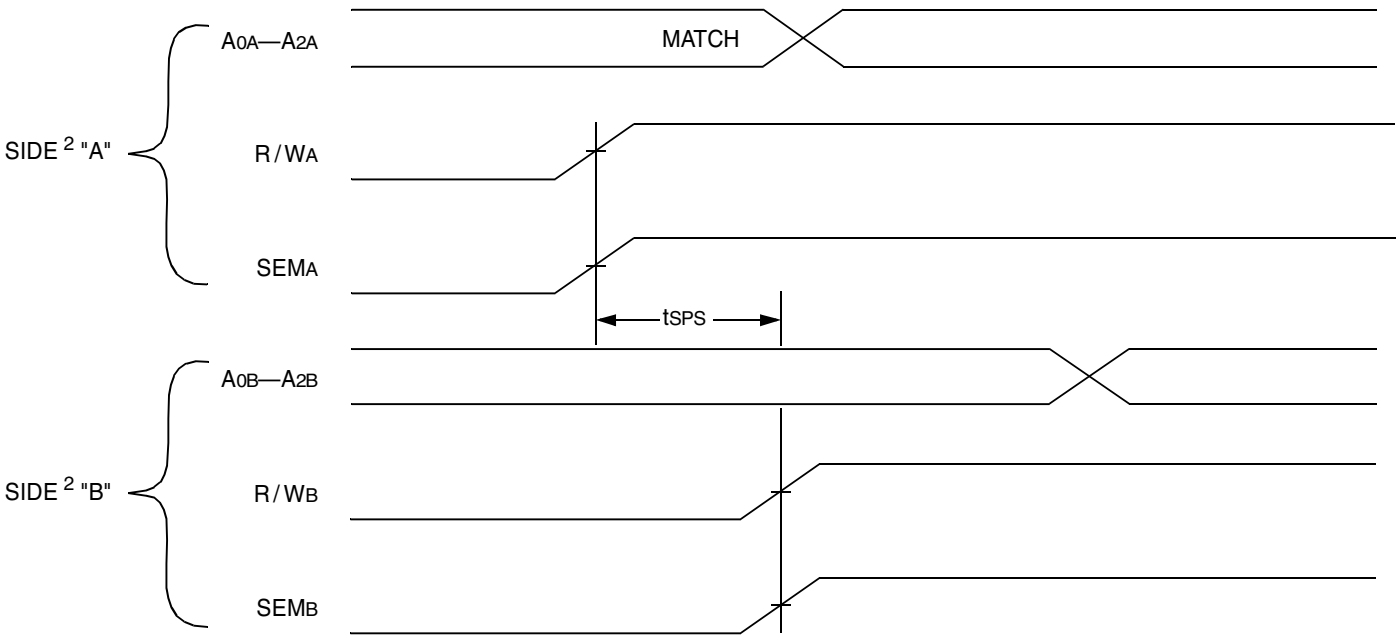
NOTES:
1. R/$\overline{W}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a LOW $\overline{CS}$ and a LOW R/$\overline{W}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going HIGH to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must be applied.
5. If the $\overline{CS}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last.
7. Timing depends on which enable signal is de-asserted first.
8. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

Timing Waveform of Semaphore Read after Write, Either Side[1]



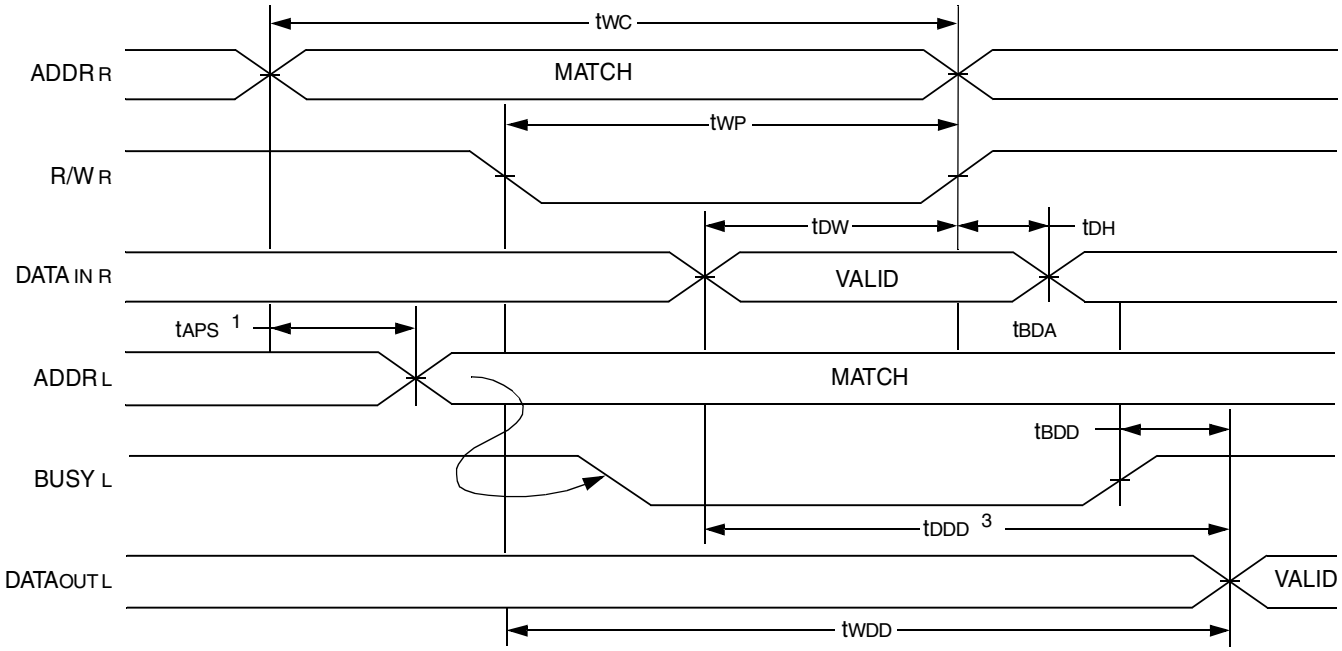
NOTE:
1. $\overline{CS} \geq V_{IH}$ for the duration of the above timing (both write and read cycle).

Timing Waveform of Semaphore Contention[1,3,4]



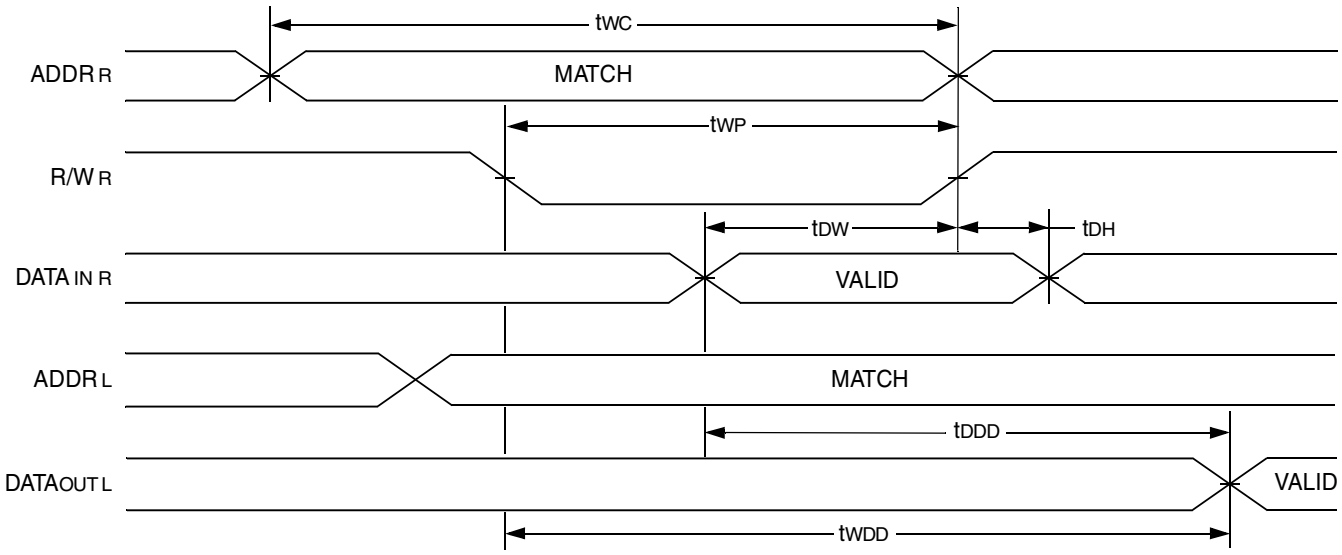
NOTES:
1. $D_{OR} = D_{OL} \leq V_{IL}$, (L_ $\overline{CS}$ = R_ $\overline{CS}$) $\geq V_{IH}$ Semaphore Flag is released from both sides (reads as ones from both sides) at cycle start.
2. "A" may be either left or right port. "B" is the opposite port from "A".
3. This parameter is measured from R/$\overline{W}_A$ or $\overline{SEM}_A$ going HIGH to R/$\overline{W}_B$ or $\overline{SEM}_B$ going HIGH.
4. If tSPS is violated, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

Timing Waveform of Read with $\overline{BUSY}$ (M/$\overline{S}$ ≥ VIH)[2]



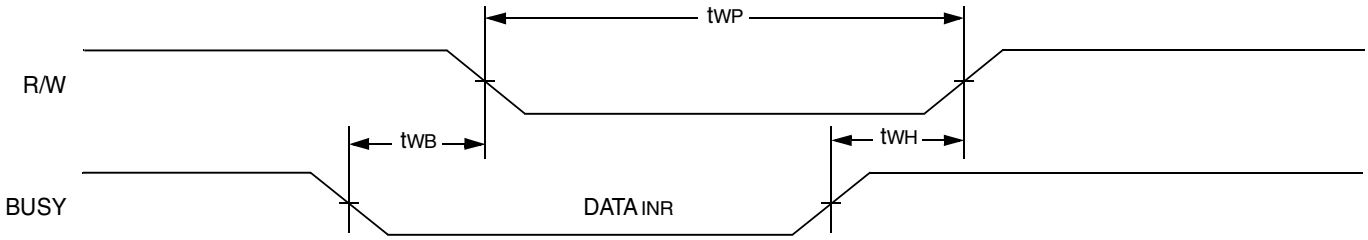
NOTES:
1. To ensure that the earlier of the two ports wins.
2. (L_ $\overline{CS}$ = R_ $\overline{CS}$) ≤ VIL.
3. $\overline{OE}$ ≤ VIL for the reading port.

Timing Waveform of Write with Port-to-Port Delay (M/$\overline{S}$ ≤ VIH)[1,2]

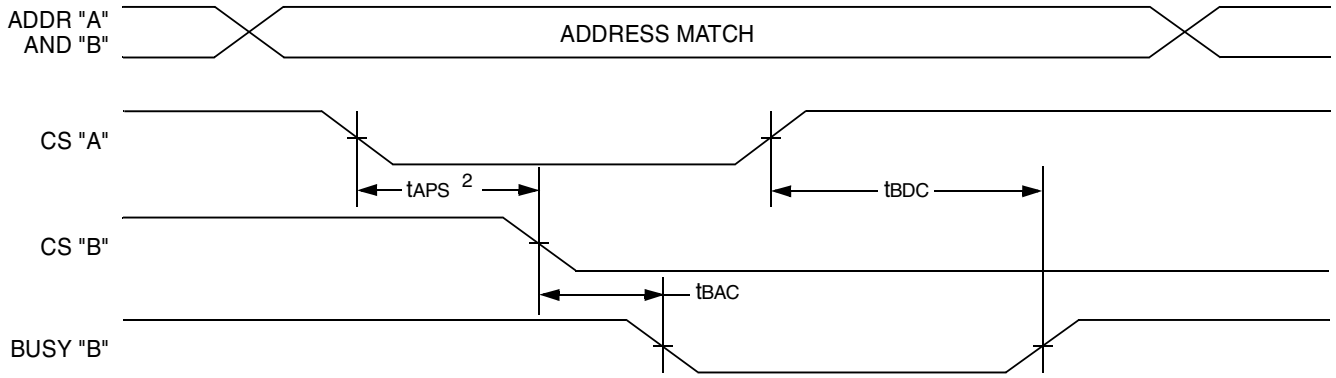


NOTES:
1. $\overline{BUSY}$ input equals HIGH for the writing port.
2. (L_ $\overline{CS}$ = R_ $\overline{CS}$) ≤ VIL.

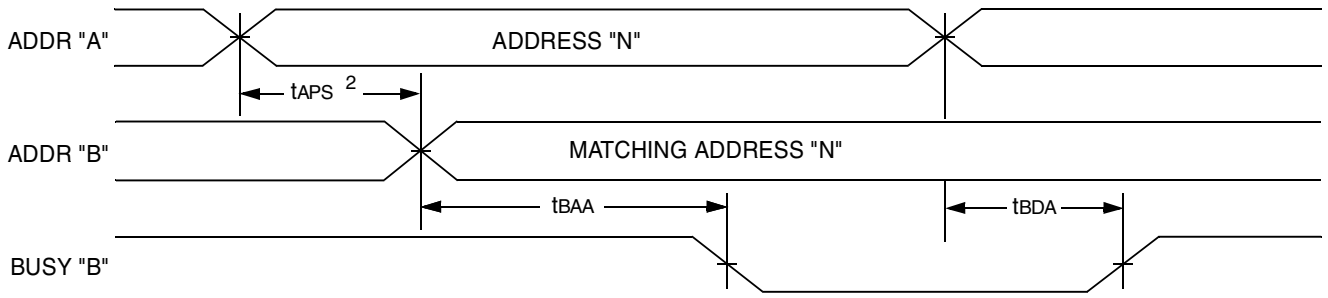
Timing Waveform of Write with $\overline{BUSY}$ Input (M/$\overline{S}$ ≤ VIL)



Timing Waveform of BUSY Arbitration ($\overline{CS}$ Controlled Timing) [1]

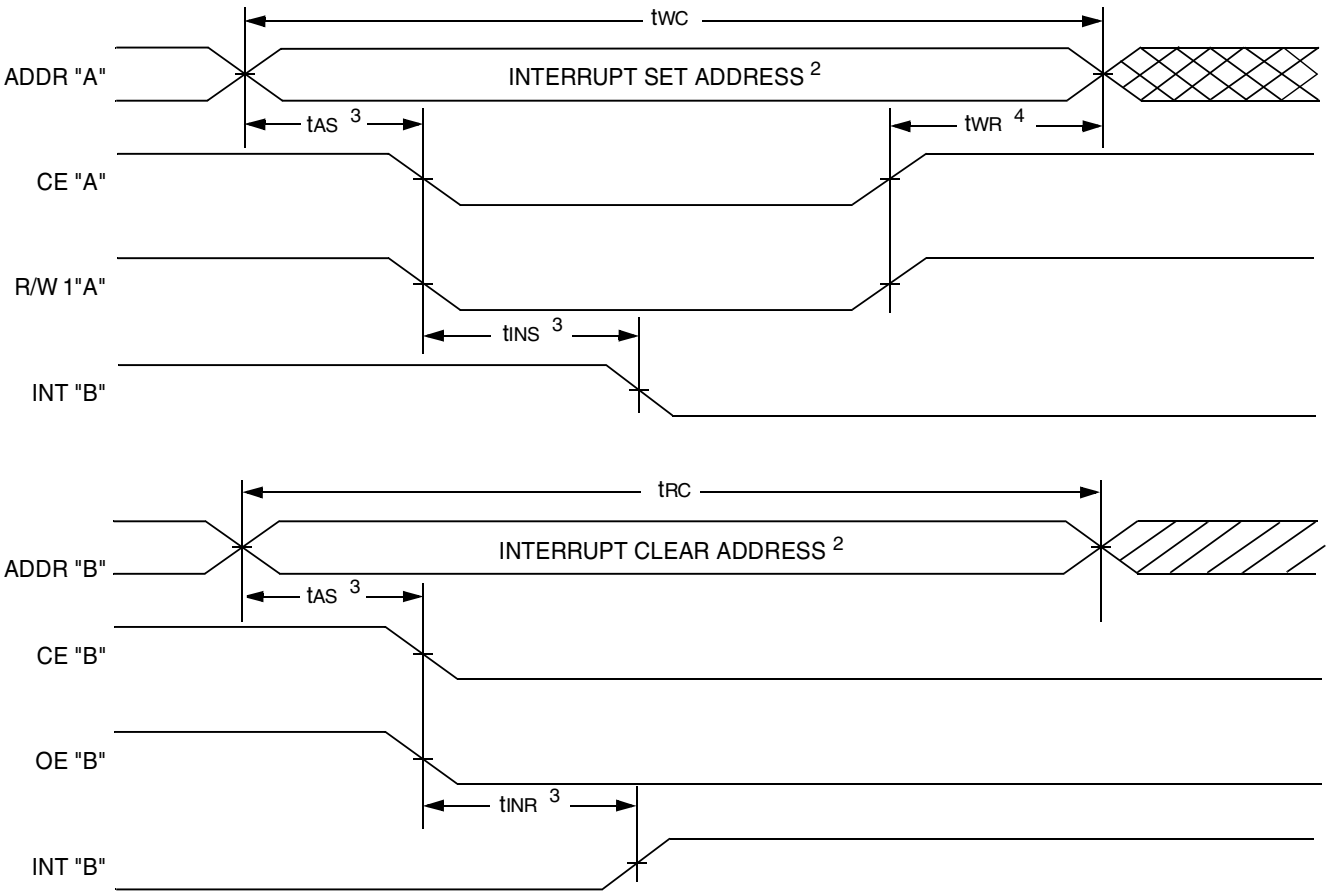


Timing Waveform of BUSY Arbitration (Controlled by Address Match Timing) [1]



NOTES:
1. All timing is the same for the left and right ports. Port “A” may be either the left or right port. Port “B” is the port opposite from “A”.
2. If tAPS is violated, the busy signal will be asserted on one side or another but there is no guarantee on which side busy will be asserted.

Timing Waveform of Interrupt Cycle [1]



NOTES:
1. All timing is the same for left and right ports. Port “A” may be either the left or right port. Port “B” is the port opposite from “A”.
2. See Interrupt truth table.
3. Timing depends on which enable signal is asserted last.
4. Timing depends on which enable signal is de-asserted first.

Truth Table I – Non-Contention Read/Write Control [1]

Inputs				Outputs	Mode
$\overline{CS}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O	Description
H	X	X	H	High-Z	Deselected or Power Down
L	L	X	H	Data_In	Write
L	H	L	H	Data_OUT	Read
X	X	H	X	High-Z	Outputs Disabled

NOTE:
1. The conditions for non-contention are L_A (0–13) ≠ R_A (0–13).
2. ⌐↑ denotes a LOW to HIGH waveform transition.

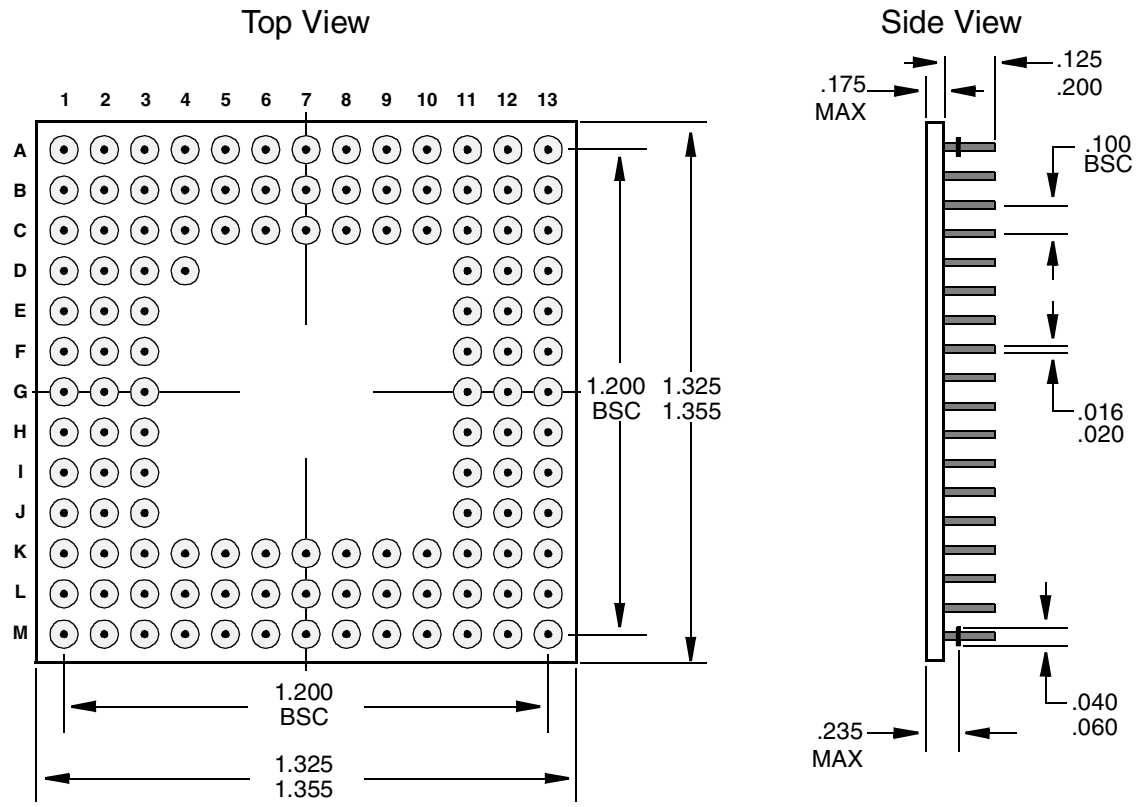
Truth Table II – Semaphore Read/Write Control

Inputs[2]				Outputs	Mode
$\overline{CS}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O	Description
H	H	L	L	Data_OUT	Read Data in Semaphore Flag
L	⌐↑	X	L	Data_In	Write Data_IN (0, 8, 16, 24)
L	X	X	L	-	Not Allowed

Pin Numbers & Functions

121 Pins — PGA					
Pin #	**Function**	**Pin #**	**Function**	**Pin #**	**Function**
A1	L_IO24	D3	L_A4	K1	L_IO11
A2	L_IO26	D4	GND	K2	M/S
A3	L_IO28	D11	R_A4	K3	GND
A4	L_IO30	D12	R_IO20	K4	L_A10
A5	L_CS	D13	R_IO19	K5	L_A11
A6	L_OE	E1	L_IO17	K6	L_A12
A7	L_RW3	E2	L_IO18	K7	GND
A8	R_OE	E3	L_A5	K8	R_A12
A9	R_CS	E11	R_A5	K9	R_A11
A10	R_IO30	E12	R_IO18	K10	R_A10
A11	R_IO28	E13	R_IO17	K11	VCC
A12	R_IO26	F1	L_SEM	K12	GND
A13	R_IO24	F2	L_IO16	K13	R_IO11
B1	L_IO23	F3	L_A6	L1	L_IO10
B2	L_IO25	F11	R_A6	L2	L_IO8
B3	L_IO27	F12	R_IO16	L3	L_IO6
B4	L_IO29	F13	R_SEM	L4	L_IO4
B5	L_IO31	G1	L_BUSY	L5	L_IO2
B6	L_A0	G2	L_INT	L6	L_A13
B7	L_RW4	G3	GND	L7	R_RW4
B8	R_A0	G11	GND	L8	R_A13
B9	R_IO31	G12	R_INT	L9	R_IO2
B10	R_IO29	G13	R_BUSY	L10	R_IO4
B11	R_IO27	H1	L_RW1	L11	R_IO6
B12	R_IO25	H2	L_RW2	L12	R_IO8
B13	R_IO23	H3	L_A7	L13	R_IO10
C1	L_IO21	H11	R_A7	M1	L_IO9
C2	L_IO22	H12	R_RW2	M2	L_IO7
C3	VCC	H13	R_RW1	M3	L_IO5
C4	L_A3	I1	L_IO15	M4	L_IO3
C5	L_A2	I2	L_IO14	M5	L_IO1
C6	L_A1	I3	L_A8	M6	L_IO0
C7	GND	I11	R_A8	M7	R_RW3
C8	R_A1	I12	R_IO14	M8	R_IO0
C9	R_A2	I13	R_IO15	M9	R_IO1
C10	R_A3	J1	L_IO13	M10	R_IO3
C11	GND	J2	L_IO12	M11	R_IO5
C12	R_IO22	J3	L_A9	M12	R_IO7
C13	R_IO21	J11	R_A9	M13	R_IO9
D1	L_IO19	J12	R_IO12		
D2	L_IO20	J13	R_IO13		

Package Outline — 121 Pin PGA "P12"



Specification subject to change without notice

Sample Ordering Information

Model Number	Speed	Package
ACT–DP16K32A–030P12C	30ns	1.35 SQ PGA
ACT–DP16K32A–035P12C	35ns	1.35 SQ PGA
ACT–DP16K32A–040P12M	40ns	1.35 SQ PGA
ACT–DP16K32A–045P12M	45ns	1.35 SQ PGA

Part Number Breakdown

ACT– DP 16K 32 A– 035 P12 Q

Aeroflex Circuit Technology

Memory Type
DP = Dual Port

Memory Depth, Locations

Memory Width, Bits

Options
A = Asynchronous

Memory Speed, ns (+5V Vcc)

Screening Level
C = Commercial Temp, 0°C to +70°C
T = Military Temp, -55°C to +125°C
M = Military Temp, -55°C to +125°C, Screened *
Q = MIL-PRF-38534 Compliant/SMD

* **Screened to the individual test methods of MIL-STD-883**

Package Type & Size

Thru-Hole Package
P12 = 1.35"SQ PGA 121 Pins

Specifications subject to change without notice

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