ALPHA SEMICONDUCTOR
Excellence in Analog Power Products

AS OP-10

Dual Matched Instrumentation Operational Amplifier

FEATURES

- Extremely tight matching
- Offset match.....0.18mV Max..
- Channel separation..... 126 dB Min
- Low bias current.....2nA Max
- High R_{IN} .....30MΩMin ..
- Bias current match .....3nA Max
- Low noise.....0.6μV_{pp}Max

APPLICATIONS

- Sampling & Hold Amplifiers
- Integrators
- Medical Instrumentation
- Strain Gauge & Thermocouple
- Precision Absolute Value Circuits

PRODUCT DESCRIPTION

The ALPHA Semiconductor AS OP-10 is a dual-matched instrumentation operational amplifier that offers two independent monolithic high-performance operational amplifiers in a single 14-pin dual-in-line package. Tight matching between channels is provided on the main parameters including offset, tracking of offset vs. temperature, non-inverting bias current and common mode and power supply rejection ratios.

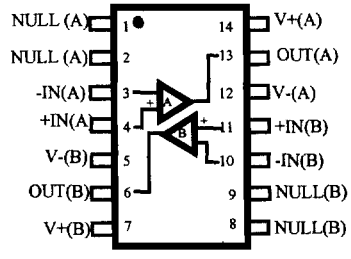
The OP-10 is available in several different grades. The AS OP-10 is available in hermetically sealed 14 pin dual-in-line package. The operating temperature is 0°C to 70°C and -55°C to +125°C.

ORDERING INFORMATION

Plastic DIP 14-PIN	TA=25°C V_{os} Max (mv)	Oper. Temp. Range
OP10EY	0.5	COM
OP10CY	0.5	COM

PIN CONNECTIONS

14-Pin EPOXY DIP



Top View

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Internal Power Dissipation (Note 1) 500mW
Differential Input Voltage ..... ±30V
Input Voltage (Note 2) ..... ±22V
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range
Y Package ..... -65 to +150°C
Operating Temperature Range
OP10A, OP10 ..... -55 to +125°C
OP10E, OP10C ..... 0 to +70°C
Dice Junction Temperature(Tj) ..... -65 to +150°C
Lead Temperature (Soldering, 60 Sec.) ..... 300°C

NOTES:
1. See Table for maximum ambient temperature rating and derating factor.
2. Absolute maximum ratings apply to both DICE and packaged parts unless otherwise noted.
3. For Supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin Plastic DIP	106°C	11.3 mW/°C

ELECTRICAL CHARACTERISTICS at V_S=±15V, Ta=25°C, unless otherwise specified.

Parameter	Symbol	Conditions	OP-10 Min.	OP-10 Typ.	OP-10 Max.	Units
Input Offset Voltage	V_{os}			0.2	0.5	mV
Long-Term Input Offset Voltage Stability	V_{OS}/Time	(Note 1)		0.25	1.0	$\mu V/M_o$
Input Offset Current	I_{os}			1.0	2.8	nA
Input Bias Current	I_B			±1	±3	nA
Input Noise Voltage (Note 2)	e_{npp}	0.1Hz to10Hz		0.35	0.6	μV_{p-p}
Input Noise Voltage Density (Note 2)	e_n	f_o=10Hz		10.3	18.0	nV/√Hz
Input Noise Voltage Density (Note 2)	e_n	f_o=100Hz		10.0	13.0	nV/√Hz
Input Noise Voltage Density (Note 2)	e_n	f_o=1000Hz		9.6		nV/√Hz
Input Noise Current (Note 2)	$i_{np\ p}$	0.1 Hz to 10Hz		14	30	pA_{p-p}
Input Noise Current Density (Note 2)	i_n	f_o=10Hz		0.32	0.80	pA/√Hz
Input Noise Current Density (Note 2)	i_n	f_o=100 Hz		0.14	0.23	pA/√Hz
Input Noise Current Density (Note 2)	i_n	f_o=1000Hz		0.12	0.17	pA/√Hz
Input Resistance-Differential-Mode	R_{in}	(Note 3)	20	60		MΩ
Input Resistance-Common Mode	R_{inCM}			200		GΩ
Input Voltage Range	IVR		±13	±14		V
Common-Mode Rejection Ratio	CMRR	V_{CM}=±13.0	110	126		dB
Power Supply Rejection Ratio	PSRR	V_S=±3V to ±18		4	10	μV/V
Large-Signal Voltage Gain	AV_O	R_l ≥2kΩ, V_o=±10V	200	500		V/mV
Large-Signal Voltage Gain	AV_O	R_l≥2kΩ, V_o=±0.5V Vs=±3V(Note 3)	200	150	500	V/mV
Output Voltage Swing	V_o	Rl ≥ 10kW	±12.5	±13.0		V
Output Voltage Swing	V_o	Rl≥2kΩ	±12.0	±12.8		V
Output Voltage Swing	V_o	Rl ≥1kΩ	±10.5	±12.0		V
Slewing Rate	SR	Rl ≥2kΩ		0.17		V/μs
Closed-Loop Bandwidth	BW	A_{vcl}=+1.0(Note 1)		0.6		MHz
Open-Loop Output Resistance	R_o	V_o=0, Io=0		60		Ω
Power Consumption	P_d	Each Amplifier		90	120	mW
Power Consumption	P_d	V_s=±3V, No load		4	6	mW
Offset Adjustment Range		R_p=20kΩ		±4		mV
Input Capacitance	Cin			8		pF

Notes:
1. Long term input offset voltage stability refers to the averaged trend line of Vos Vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in Vos during the first 30 operating days is typically. 2.5 mV.
2. Sample tested
3. Guaranteed by design.

INDIVIDUAL AMPLIFIER CHARACTERISTICS at V_S=±15V, Ta=25°C, unless otherwise specified.

Parameter	Symbol	Conditions	OP-10E			OP-10C			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage	V_{os}			0.2	0.5		0.2	0.5	mV
Long-Term Input Offset Voltage Stability	V_{OS}/Time	(Note 1)		0.3	1.5		0.5		$\mu V/M_o$
Input Offset Current	I_{os}			1.2	3.8		1.8	6.0	nA
Input Bias Current	I_B			±1.2	±4.0		±1.8	±7.0	nA
Input Noise Voltage (Note 2)	e_{npp}	0.1Hz to10Hz		0.35	0.6		0.38	0.65	μV_{p-p}
Input Noise Voltage Density (Note 2)	e_n	f_o=10Hz		10.3	18.0		10.3	20.0	nV/√Hz
Input Noise Voltage Density (Note 2)	e_n	f_o=100Hz		10.0	13.0		10.2	13.5	nV/√Hz
Input Noise Voltage Density (Note 2)	e_n	f_o=1000Hz		9.6	11.0		9.8	11.5	nV/√Hz
Input Noise Current (Note 2)	$i_{np\,p}$	0.1 Hz to 10Hz		14	30		15	35	pA_{p-p}
Input Noise Current Density (Note 2)	i_n	f_o=10Hz		0.32	0.80		0.35	0.90	pA/√Hz
Input Noise Current Density (Note 2)	i_n	f_o=100 Hz		0.14	0.23		0.15	0.27	pA/√Hz
Input Noise Current Density (Note 2)	i_n	f_o=1000Hz		0.12	0.17		0.13	0.18	pA/√Hz
Input Resistance-Differential-Mode	R_{in}	(Note 3)	15	50		8	33		MΩ
Input Resistance-Common Mode	R_{inCM}			160			120		GΩ
Input Voltage Range	IVR		±13	±14		±13	±14		V
Common-Mode Rejection Ratio	CMRR	V_{CM}=±13.0	106	123		100	120		dB
Power Supply Rejection Ratio	PSRR	V_S=±3V to ±18		4	20		10	32	μV/V
Large-Signal Voltage Gain	AV_O	R_l≥2kΩ, V_o=±10V	200	500		120	400		V/mV
Large-Signal Voltage Gain	AV_O	R_l≥2kΩ, V_o=±0.5V Vs=±3V(Note 3)	150	500		100	400		V/mV
Output Voltage Swing	V_o	Rl≥10kΩ	±12.5	±13.0		±12.0	±13.0		V
Output Voltage Swing	V_o	Rl≥2kΩ	±12.0	±12.8		±11.5	±12.8		V
Output Voltage Swing	V_o	Rl≥1kΩ	±10.5	±12.0			±12.0		V
Slewing Rate	SR	Rl≥2kΩ		0.17			0.17		V/μs
Closed-Loop Bandwidth	BW	A_{vcl}=+1.0(Note 1)		0.6			0.6		MHz
Open-Loop Output Resistance	R_o	V_o=0, Io=0		60			60		Ω
Power Consumption	P_d	Each Amplifier		90	120		95	150	mW
Power Consumption	P_d	V_s=±3V, No load		4	6		4	8	mW
Offset Adjustment Range		R_p=20kΩ		±4			±4		mV
Input Capacitance	Cin			8			8		pF

ELECTRICAL AMPLIFIER CHARACTERISTICS at V_S=±15V, -55°C≤Ta≤+125°C, unless otherwise specified.

Parameter	Symbol	Conditions	OP-10 Min.	OP-10 Typ.	OP-10 Max.	Units
Input Offset Voltage	V_{os}			0.3	0.7	mV
Average Input Offset Voltage Drift Without External Trim With External Trim	 TCV_{os} TCV_{os}	 (Note 1) Rp=20Ω (note 3)		 0.7 0.3	 2.0 1.0	µV/°C µV/°C
Input Offset Current	I_{os}			1.8	5.6	nA
Average Input Offset Current Drift	TCI_{os}	Note 2		8	50	pA/°C
Input Bias Current	I_B			±2	±6	nA
Average Input Bias Current Drift	TCI_B	Note 2		13	50	pA/°C
Input Voltage Range	IVR		±13.0	±13.5		V
Common-Mode Rejection Ratio	CMRR	V_{CM} ±13.0 V	106	123		dB
Power Supply Rejection Ratio	PSRR	V_s=±3V to ±18V		5	20	µV/V
Large-Signal Voltage Gain	A_{vo}	R_L≥2Ω, V_o= ±10V	150	400		V/mV
Output Voltage Swing	V_o	R_L≥2Ω	±12	±12.6		V

MATCHING CHARACTERISTICS at V_S=±15V, Ta=+25°C, Unless otherwise specified.

Parameter	Symbol	Conditions	OP-10 Min.	OP-10 Typ.	OP-10 Max.	Units
Input Offset Voltage	V_{os}			0.12	0.5	mV
Average Noninverting Bias Current	I_B^+			±1.3	±4.5	nA
Noninverting Offset Current	I_{OS}^+			1.1	4.5	nA
Inverting Offset Current	I_{OS}^+			1.1	4.5	nA
Common-Mode Rejection Ratio Match	CMRR	V_{CM}=±13V	106	120		dB
Power Supply Rejection Ratio Match	PSRR	V_S=3V to ±18		4	20	µV/V
Channel Separation	CS	(Note 2)	126	140		dB

MATCHING CHARACTERISTICS at V_S=±15V, -55°C≤Ta≤+125°C, unless otherwise noted.

Parameter	Symbol	Conditions	OP-10 Min.	OP-10 Typ.	OP-10 Max.	Units
Input Offset Voltage Match	V_{os}			0.2	0.9	mV
Input Offset Voltage Tracking Drift Without External Trim With External Trim	 TCV_{os} TCV_{os}	 (Note 2) Rp=20Ω (note 3), Channel A only		 0.9 0.4	 2.5 1.2	µV/°C µV/°C
Average Noninverting Bias Current	I_B^+			±2.4	±8.0	nA
Average Drift of Noninverting Bias Current	TCI_B^+	Note 2		15		pA/°C
Noninverting Offset Current	I_{OS}^+			2.4	90	nA
Average Drift of Noninverting Offset Current	TCI_{OS}	Note 2		18		pA/°C
Inverting Offset Current	I_{OS}			2.4	90	nA
Common-Mode Rejection Ratio Match	CMRR	V_{CM}=±13V	103	117		dB
Power Supply Rejection Ratio Match	PSRR	V_s=±3V to +18		7	32	µV/V

Notes:

1. Long term input offset voltage stability refers to the averaged trend line of Vos Vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in Vos during the first 30 operating days is typically. 2.5 mV.
2. Sample tested
3. Guaranteed by design.

INDIVIDUAL CHARACTERISTICS at V_S=±15V, 0°C≤Ta≤+70°C, unless otherwise specified.

Parameter	Symbol	Conditions	OP-10E Min.	OP-10E Typ.	OP-10E Max.	OP-10C Min.	OP-10C Typ.	OP-10C Max.	Units
Input Offset Voltage	V_{os}			0.25	0.6		0.35	1.6	mV
Average Input Offset Voltage Drift Without External Trim With External Trim	 TCV_{os} TCV_{os}	 (Note 1) Rp=20Ω (note 3)		 0.7 0.3	 2.0 1.0		 1.2 0.4	 4.5 1.5	µV/°C µV/°C
Input Offset Current	I_{os}			1.4	5.3		2.0	8.0	nA
Average Input Offset Current Drift	TCI_{os}	Note 2		8	50		12	50	pA/°C
Input Bias Current	I_B			±1.5	±5.5		±2.2	±9.0	nA
Average Input Bias Current Drift	TCI_B	Note 2		13	50		18	50	pA/°C
Input Voltage Range	IVR		±13.0	±13.5		±13.0	±13.5		V
Common-Mode Rejection Ratio	CMRR	V_{CM} ±13.0 V	103	123		97	120		dB
Power Supply Rejection Ratio	PSRR	V_s=±3V to ±18V		7	32		10	51	µV/V
Large-Signal Voltage Gain	A_{VO}	R_l≥2Ω, V_o= ±10V	100	400		100	400		V/mV
Output Voltage Swing	V_o	R_l≥2Ω	±12.0	±12.6		±11.0	±12.6		V

Notes:

1. *Long term input offset voltage stability refers to the averaged trend line of Vos* Vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in Vos during the first 30 operating days are typically. 2.5 mV.
2. *Sample tested*
3. Guaranteed by design.

MATCHING CHARACTERISTICS at V_S=±15V, Ta=+25°C, Unless otherwise specified.

Parameter	Symbol	Conditions	OP-10E Min.	OP-10E Typ.	OP-10E Max.	OP-10C Min.	OP-10C Typ.	OP-10C Max.	Units
Input Offset Voltage Match	V_{os}			0.12	0.5		0.3		mV
Average Noninverting Bias Current	I_B^+			±1.3	±4.5		±2.0		nA
Noninverting Offset Current	I_{OS}^+			1.1	4.5		1.8		nA
Inverting Offset Current	I_{OS}^+			1.1	4.5		1.8		nA
Common-Mode Rejection Ratio Match	CMRR	V_{CM}=±13V	106	120			117		dB
Power Supply Rejection Ratio Match	PSRR	V_S=3V to ±18		4	20		5		µV/V
Channel Separation	CS	(Note 1)	126	140		126	137		dB

MATCHING CHARACTERISTICS at V_S=±15V, 0°C≤Ta≤+70°C, unless otherwise specified.

Parameter	Symbol	Conditions	OP-10E Min.	OP-10E Typ.	OP-10E Max.	OP-10C Min.	OP-10C Typ.	OP-10C Max.	Units
Input Offset Voltage Match	V_{os}			0.18	0.7		0.4		mV
Input Offset Voltage Tracking Drift Without External Trim With External Trim	 TCV_{os} TCV_{os}	 (Note 1) Rp=20Ω(note 3), Channel A only		 0.9 0.3	 2.3 0.9		 1.3 0.6		µV/°C µV/°C
Average Noninverting Bias Current	I_B^+			±2.0	±6.0		±2.8		nA
Average Drift of Noninverting Bias Current	TCI_B^+	Note 1		12	40		18		pA/°C
Noninverting Offset Current	I_{OS}^+			2.0	6.0		2.8		nA
Average Drift of Noninverting Offset Current	TCI_{OS}	Note 1		15	50		20		pA/°C
Input Offset Current	I_{OS-}			2.0	6.0		2.8		nA
Common-Mode Rejection Ratio Match	CMRR	V_{CM}=±13V	103	117			114		dB
Power Supply Rejection Ratio Match	PSRR	V_s=±3V to +18		6	32			8	µV/V

Notes:

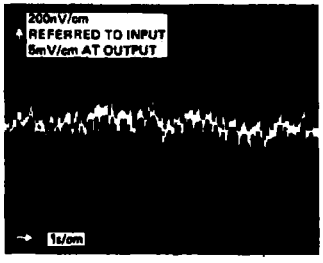
1. Sample tested
2. 2. Guaranteed by design.

OFFSET NULLING CIRCUIT

BURN-IN CIRCUIT

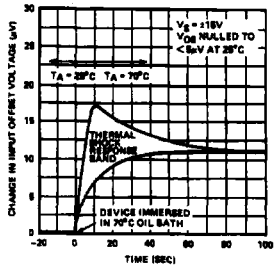
TYPICAL PERFORMANCE

OP-10 LOW FREQUENCY NOISE

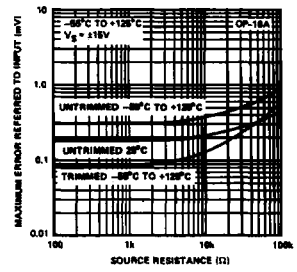


TYPICAL PERFORMANCE

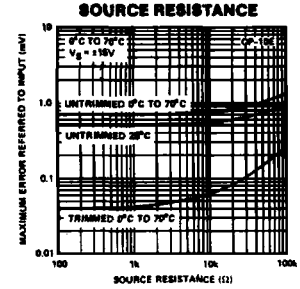
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



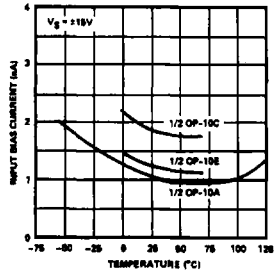
MATCHING CHARACTERISTIC MAXIMUM INPUT ERROR vs SOURCE RESISTANCE



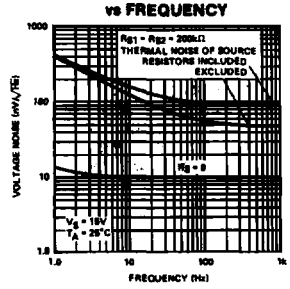
MATCHING CHARACTERISTIC MAXIMUM INPUT ERROR vs SOURCE RESISTANCE



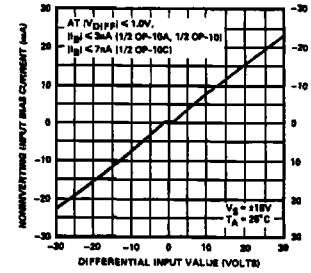
INPUT BIAS CURRENT vs TEMPERATURE



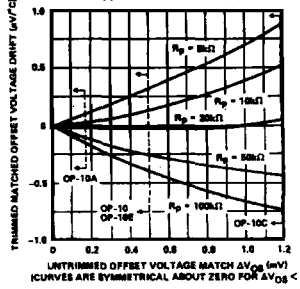
VOLTAGE NOISE DENSITY vs FREQUENCY



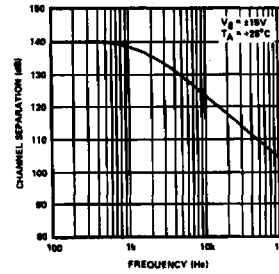
INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE



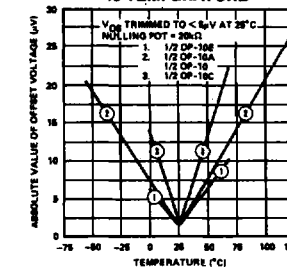
MATCHING CHARACTERISTICS TRIMMED MATCHED OFFSET VOLTAGE DRIFT AS A FUNCTION OF TRIMMING POT (R_P) SIZE AND ΔV_{OS}



MATCHING CHARACTERISTICS CHANNEL SEPARATION vs FREQUENCY

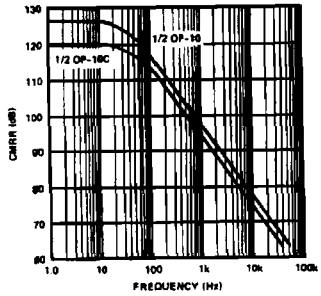


TRIMMED OFFSET VOLTAGE vs TEMPERATURE

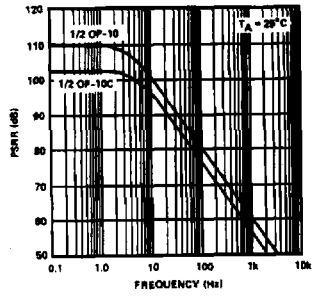


TYPICAL PERFORMANCE

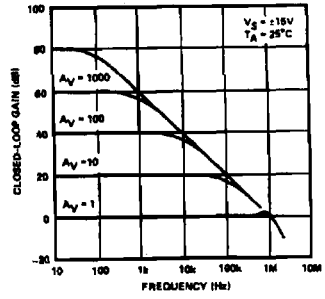
CMRR vs FREQUENCY



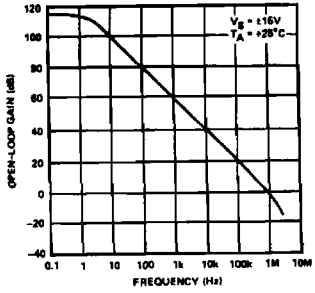
PSRR vs FREQUENCY



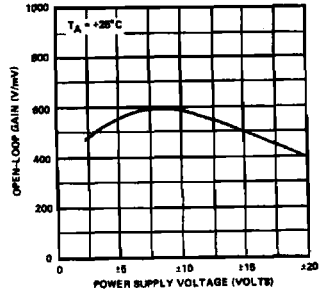
CLOSED-LOOP GAIN vs FREQUENCY



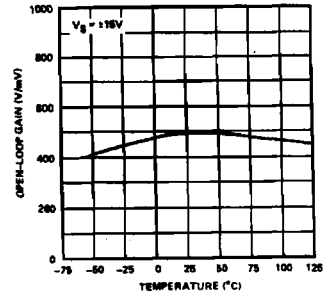
OPEN-LOOP GAIN vs FREQUENCY



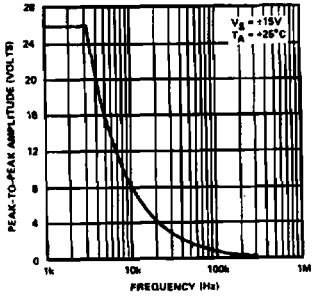
OPEN-LOOP GAIN vs POWER SUPPLY VOLTAGE



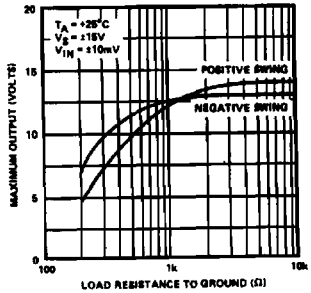
OPEN-LOOP GAIN vs TEMPERATURE



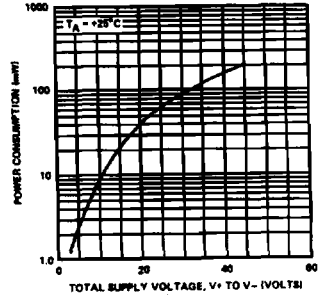
MAXIMUM OUTPUT SWING vs FREQUENCY



MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



POWER CONSUMPTION vs POWER SUPPLY



APPLICATION INFORMATION

DUAL MATCHED OP-AMP ADVANTAGES

Dual matched operational amplifiers provide a powerful tool in solving some difficult circuit design problems. Circuits include true instrumentation amplifiers, high common-mode rejection DC amplifiers, extremely low drift, low DC drift active filters, dual tracking voltage references and many other demanding applications. These designs all require good matching between two operational amplifiers.

The circuit below shows the how the errors can be reduced through these advantages. If the resistors are matched, then the gain of each side will be identical. If the offset voltage of each amplifier is matched, then the net differential voltage at the amplifiers output will be zero. The impedance of each input, both common-mode and differential-mode, are extremely high, an important feature not possible with single operational amplifier circuits.

POWER SUPPLIES

The positive supply terminals are completely independent and may be powered by separate supplies if desired. However, this method would sacrifice the advantages of power supply rejection ratio matching. The negative supply terminals are both connected to the common substrate and must be tied to the same voltage.

OFFSET TRIMMING

Each amplifier has its own offset voltage trimming. The performance over temperature is done by trimming one side to match the offset of the other side.

The AS OP-10 provides the lowest drift when trimmed with 20kΩ potentiometer. This value provides about ±4mV of adjustment range.